Backplane Ethernet Study Group

Market Drivers and Cost Considerations in Support of 40 inch average grade FR4 backplane links at 10Gb/s per lane

Bill Hoppin
Business Development, Synopsys
bhoppin@synopsys.com

Orlando, FL March 2004

Contributors and Supporters

System Vendors	
Kevin Cai	SUN
Joel Goergen	Force10 Networks
Hassan-Ali Mudhafar	Alcatel
Bert Simonovich	Nortel Networks
Bryan Parlor	Nortel Networks
Tad Hofmiester	Ciena
Steve West	Turin Networks

Technology Vendors	
Bill Hoppin	Synopsys, formerly Accelerant Networks
Ted Rado	Analogix
Greg Sheets	Agere
John Stonick	Synopsys, formerly Accelerant Networks
Mike McConnel	Keyeye
Kewei Yang	Analogix
John D'Ambrosia	Tyco
Jimmy Sheffield	Tyco
Bob Noseworthy	UNH
Neal Buren	Agilent

"The contributions to this document are those of the individual contributors who support multi-level signaling standardization for certain applications. They do not necessarily reflect the support from their respective companies over competing technology solutions for other applications."

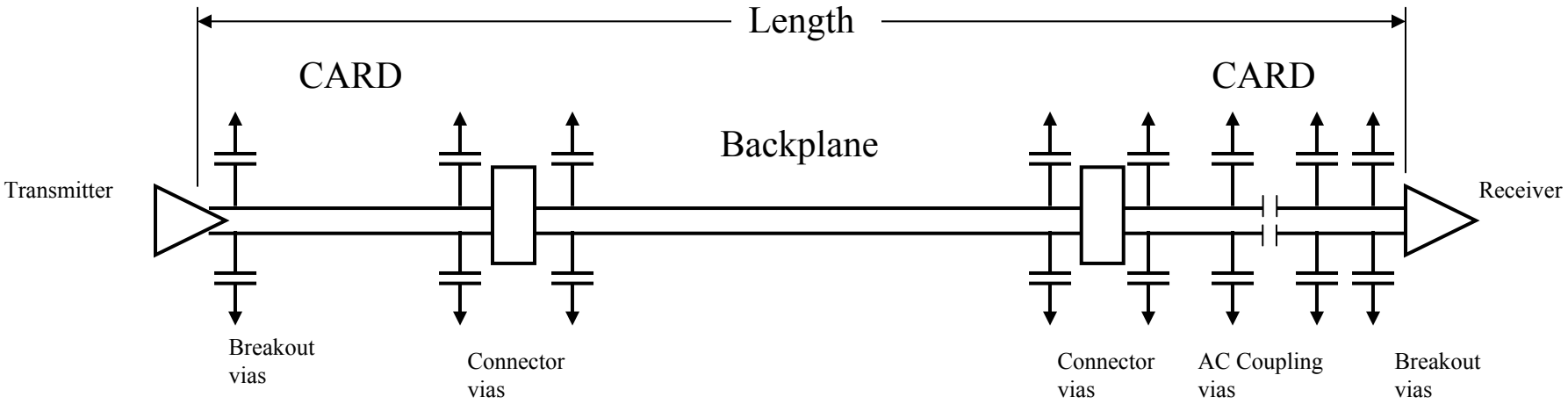
Outline

40 inches FR4 and 2 connectors at 10Gb/s serial per lane

- Currently adopted objectives are appropriate because :
  - Market potential is installed base systems and cost optimized new systems
  - Represents realistic range of line card and backplane applications
  - Accounts for manufacturing and environmental variation
  - Economic feasibility by enabling cost effectiveness at the system level
    - Backplane material, connectors and via structure considerations
- Currently adopted objectives are feasible because :
  - 10G measured results continue to build technical confidence
  - 10G power reasonable today, and coming down
  - 10G silicon complexity/cost following well understood economic curves
- Summary

Legacy system considerations

- Systems shipping today
- Need to work with installed base hardware and high speed mode within the same shelf – do not want to replace all cards for upgrades
  - Speed of links is a function of faceplate capacity, real estate and power dissipation the rack can support
  - Systems that support these constraints upgrade candidates for 10G links
- Length up to 1M (40 inches) See fig below typical channel definition



Legacy system considerations

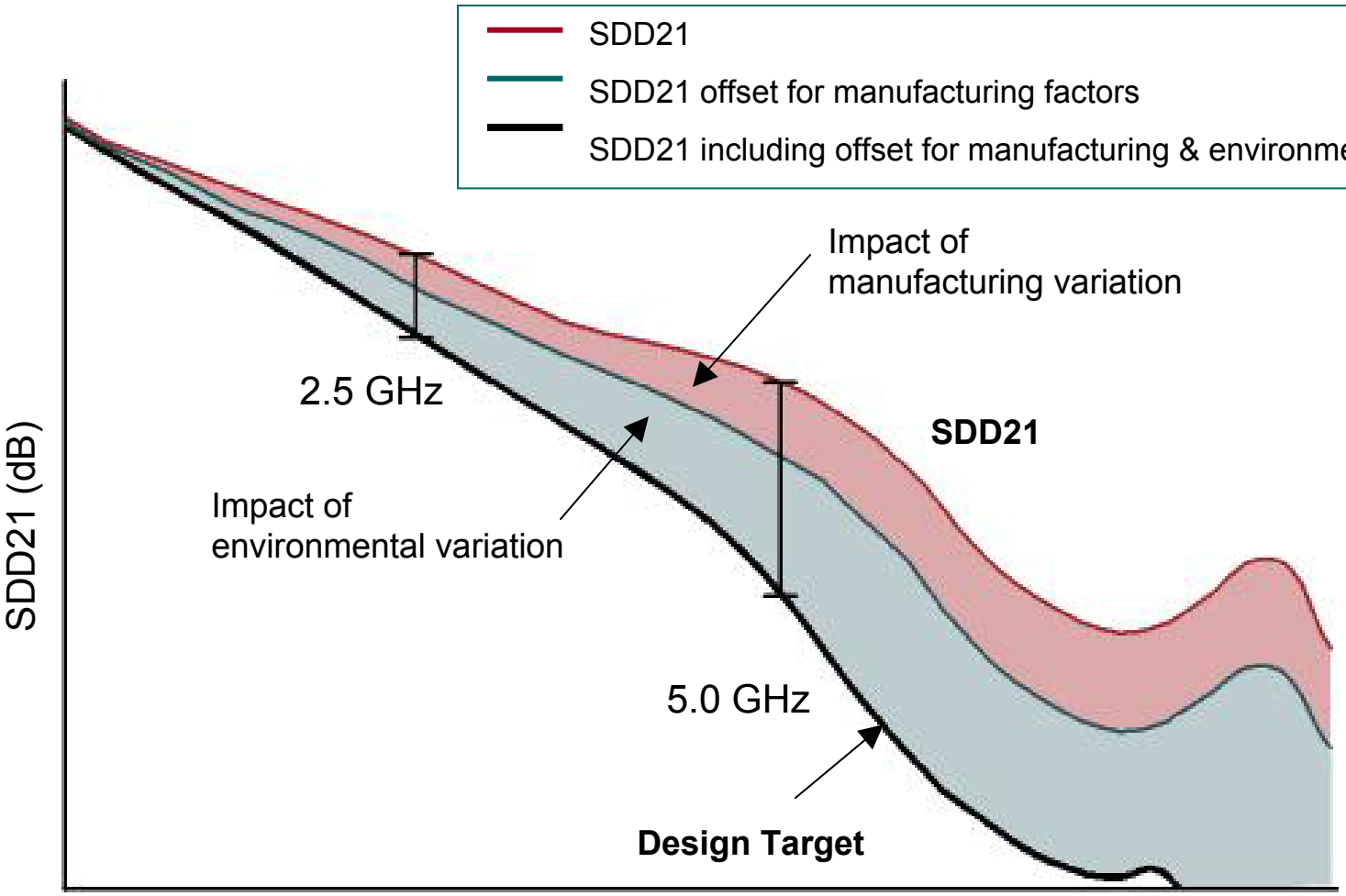
- A legacy upgrade electrical challenge
  - To upgrade an in-service legacy system for a 10G multi-rate switch card you must have the ability to load legacy and 10G backplane port cards in any slot
  - Standard must allow for backplane transceiver CDR solutions to operate from 1G to 10G data rates
    - Note: Traditional CDR solutions do not do this today. MLS solutions do, with less risk as the required baud range is 1-5G vs. 1-10G

- System Impact
  - Any switch fabric that needs a CDR to extract data and clock (usually Layer2 and above), needs to accept both legacy 1G and 10G data at the port inputs
  - Otherwise the pads must be switched to an appropriate CDR for the rate which is highly undesirable

Cost optimized new system considerations

- New systems in development today are the legacy systems of tomorrow
- COST, POWER, REAL ESTATE are king
  - Expensive material or connectors for infrastructure to support future 10G are not acceptable to many, and imply expensive qualification and risk for system vendors
    - Medium grade FR4 (ISOLA FR406) or equivalent preferred, especially line cards
    - Nelco-13 or equivalent for backplane is acceptable and qualified in systems
  - Low power, highly integrated solutions are preferred
- ATCA as a starting ref application for channel PCB trace lengths
  - Length based on ATCA approximately 31 inches (assuming 5" per line cards) for a mesh in 19" rack
- The 40 inch objective is an appropriate channel relative to ATCA as it:
  - Accounts for manufacturing and environmental guard band
  - Supports the need for mezzanine card capability –additional connectors and vias in channel model

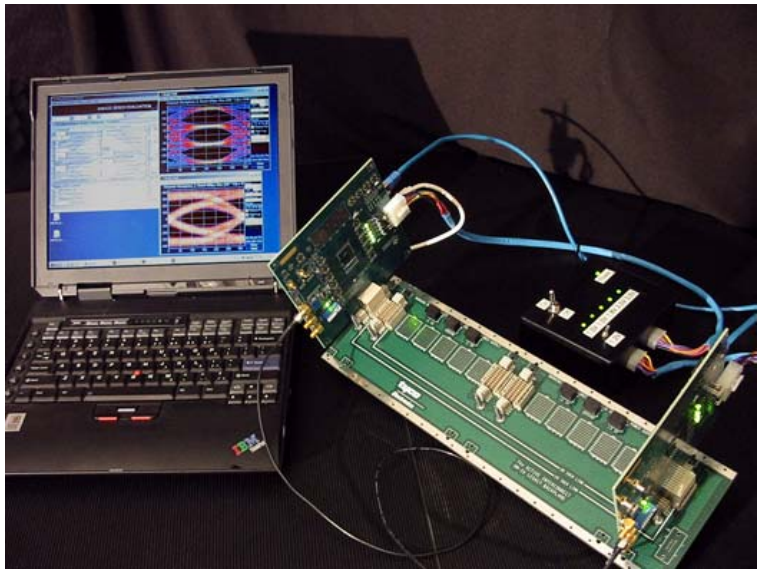
Guard Banding SDD21 for margin



At higher speeds, manufacturing & environmental variations have a significant, and often overlooked, impact on end performance of the total interconnect system

10G Measured Feasibility Data

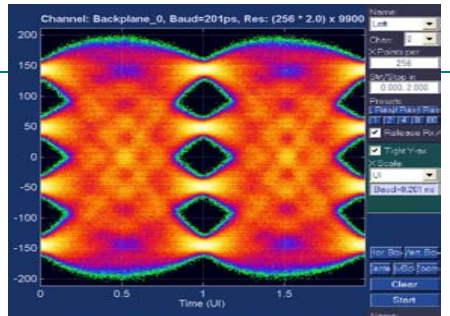
- 6 backplane configurations
  - 4000-6, 4000-13, 4000-13SI, 6000, 6000SI, and ISOLA 620
  - 4.75 mil wide traces (4 mil on 4000-6 variants)
- 3 Lengths
  - 8”, 22” and 36” lengths
- 3 types of HM-Zd signal routing (4 FEXT, 4 NEXT)
  - QuadRoute Tx to Tx, Rx to Rx
  - QuadRoute Tx to Rx, Rx to Tx
  - Non QuadRoute



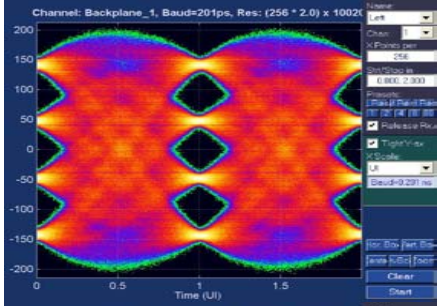
	Pair A/B	Pair C/D	Pair E/F	Pair G/H
Column 5	Tx_0	Tx_1	Tx_2	Tx_3
Column 6	Rx_0	Rx_1	Rx_2	Rx_3

10G measurements with FEXT/NEXT 36” backplane

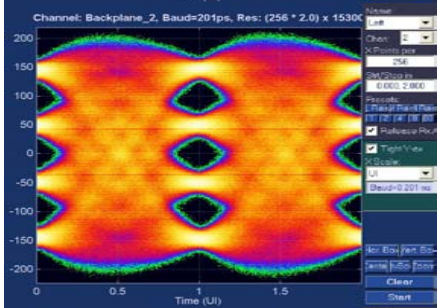
1 C0



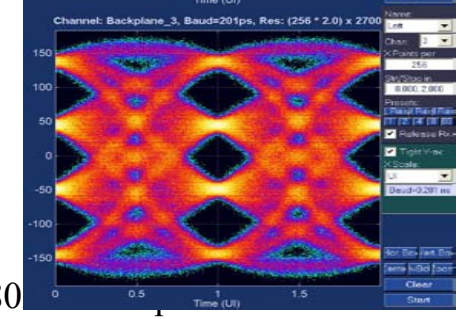
1 C1



1 C2



1 C3



5G PAM4 .13u device running at 10G

All 8 pairs active on QuadRoute FR4 4000-13SI, full crosstalk conditions (4 FEXT, 4 NEXT)

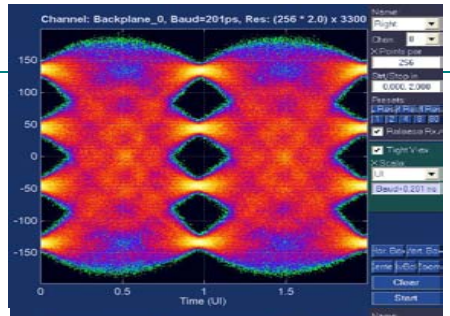
All devices tested to BER 10^-12 using 2^31 PRBS Pattern over 36 inches

8” and 22” link conditions across all 6 materials passed BER 10^-12 using 2^31 PRBS Pattern

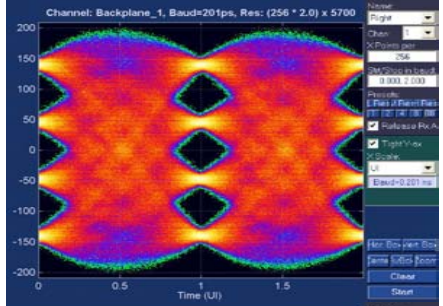
Out of 336 links tested, 34 36” link configurations did not pass and will be the subject of future simulation work on a mutually agreed to channel model with purpose built 10G designs

* Data courtesy of Tyco electronics, with support from Synopsys (formerly Accelerant Networks)

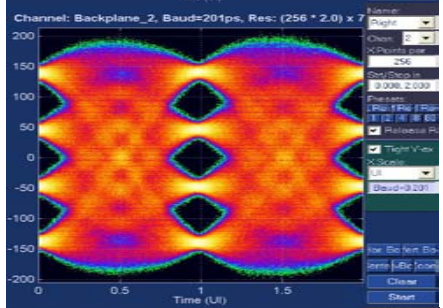
2 C0



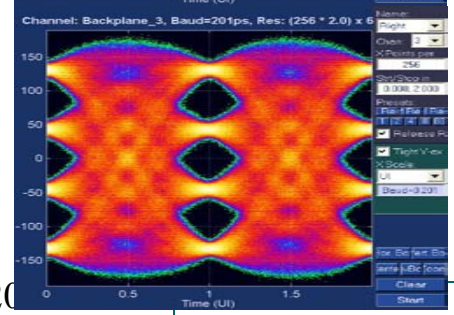
2 C1



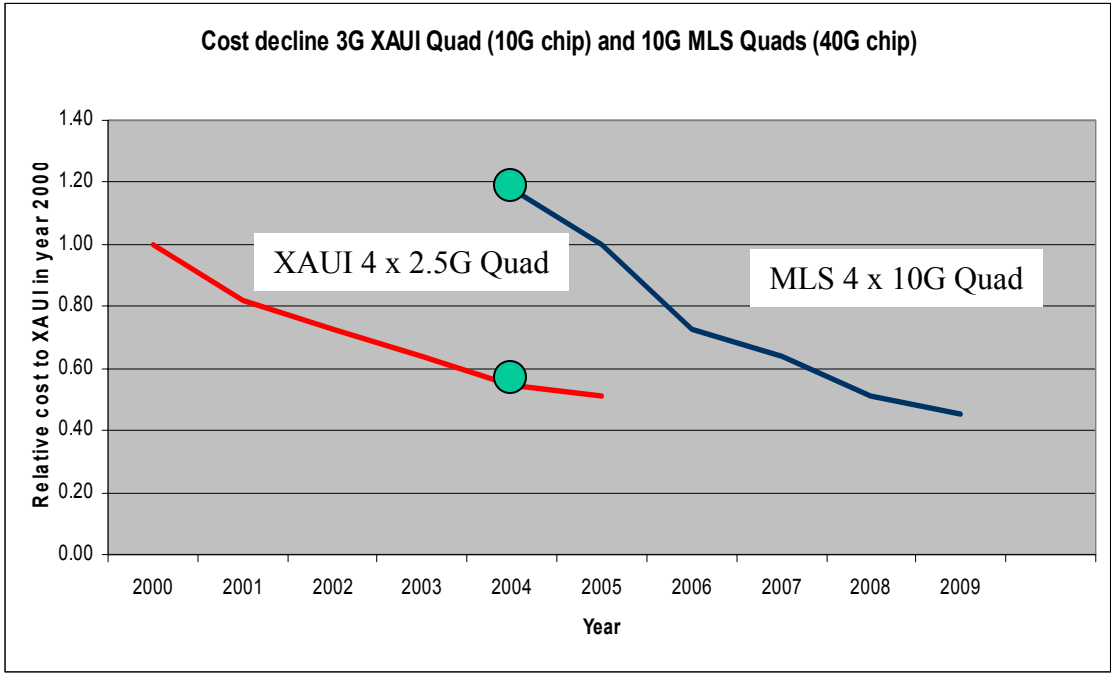
2 C2



2 C3

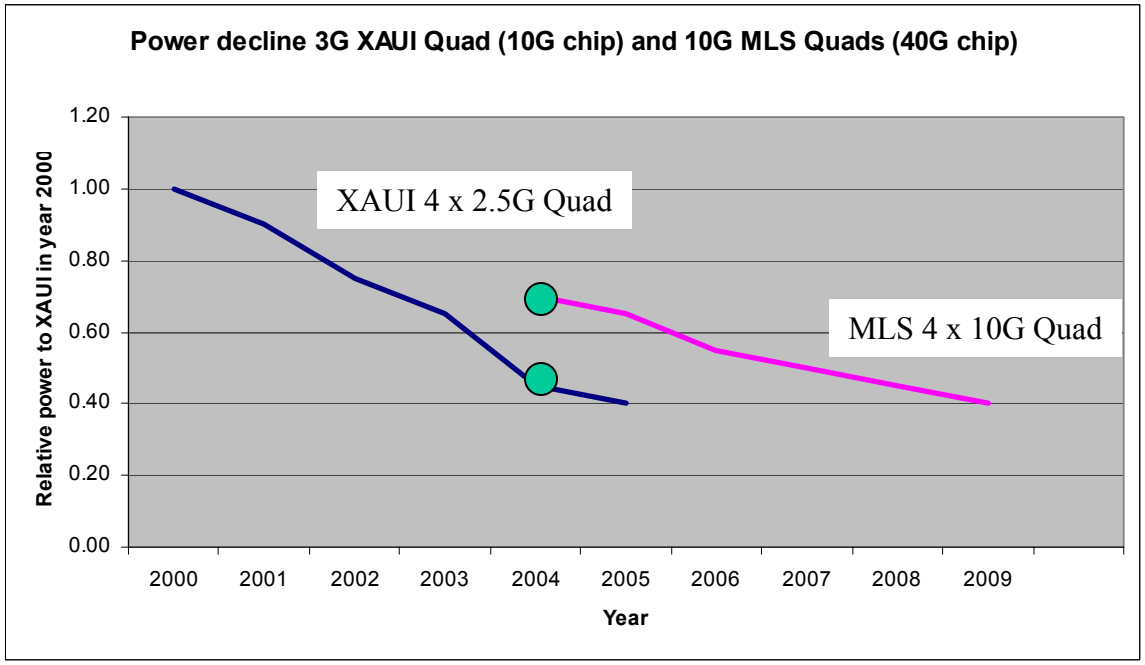


Silicon complexity and cost



- MLS does not represent significant increase in complexity or die size
  - Will follow a similar cost decline to XAUI
  - By 2007 will approach same cost as XAUI today, integration is important

Power Considerations



- MLS does not represent significant increase in power
  - Will follow a similar power decline to XAUI
  - By 2007 will approach same power as XAUI today

Future work

- Feasibility data so far is from .13u 5G part run at 10G
  - Margin will be gained with 10G purpose built designs
  - Performance gains quantified through simulation work on agreed to channel model
- Process road maps and customers support 1.8V supplies
  - Per FSA, the number of Gate Oxide options is increasing, not decreasing
    - 90nm is the first technology to support Triple Oxides
  - 1.8V customer power supplies and devices available through 45nm
- Test vendors desire to align and support standards efforts
- Address need for > 10e-15 BER from some system vendors

5 criteria

- Broad market potential – proven!
- Compatibility (non-issue)
- Distinct identity – proven!
- Technical feasibility – proven!
- Economic feasibility – proven!

Summary

- The current objectives are the right ones
  - Broad market = potential legacy and cost optimized new designs
  - Technical feasibility = data continues to support objectives
  - Economic feasibility = cost, power, and integration concerns are being addressed

- Propose to quantify objectives in a representative channel model
- Future work will match purpose built 10G solutions to channel model