Reference receiver proposal for CAUI-4 chip to chip

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Background: COM noise budget

- COM models total receiver noise as a combination of:
 - Channel-induced noise (unequalized ISI, crosstalk)
 - TX jitter
 - Assumed maximum values for BUJ and RJ
 - Converted to noise using cursor slopes
 - TX noise, attenuated by the thru channel
 - Assumed Gaussian; currently SNDR=29 dB
 - Represents internal xtalk, supply noise, etc.
 - System noise
 - Taken as 5.2e-8 V²/GHz at the RX filter input
 - Represents thermal noise, EMI, etc.

Often ignored in simulations

COM experiment

- Channel: 15 dB Meg6 LowSR (Rich Mellitz), THRU + 3 NEXT (small)
- TX: 12 mm package model from annex 93A; min amplitude
- RX: 3 scenarios
 - A: "CAUI-4 reference receiver"
 - Ideal termination
 - CTLE as in annex 93A (in D1.1 of 83D it is TBD)
 - Not technically feasible
 - B: "Realistic receiver"
 - 12 or 30 mm RX package + die cap + 55 Ω term (as in D2.2 of 802.3bj)
 - CTLE as in annex 93A
 - Technically feasible
 - C: "Improved realistic receiver"
 - Same as B, but RX has an additional 1-tap DFE
 - Also technically feasible

In all cases, 2 packages assumed for remote part, 12 or 30 mm

Does RX termination matter at all?

Here are the two package models used in 100GBASE-KR4 (concatenated to measured s-parameters)



Effect of RX termination (TX always includes 12 mm package)



Ideal termination

12 mm RX package

30 mm RX package

Scenario A results



This (or something similar) is currently suggested as a reference receiver for RX interference compliance...

- Very minor ISI effect seems to have lots of margin
- Unrealistic no package is transparent
- Those of us who don't have a good package may use other means to compensate... (e.g. DFE?)





Scenario B results



This is "real life" for this channel, assuming DFE is not allowed

- Signal very attenuated
- ISI still dominant in noise budget
- Margin seems too low





Scenario C results

Suggest changing minimum COM for CAUI-4 to 2 dB – then both package assumptions provide healthy margin



If we assume one DFE tap, results improve considerably

- This is a realistic scenario!
- Those of us who don't have a 1-tap DFE may use other means to compensate... (e.g. a good package?)





DFE implications

- Cost and power impact
 - 1-tap DFE can be designed with negligible area
 - Estimated power delta: <1 pJ/bit; likely <<10% of device power
- Error propagation
 - Results above have a small tap weight (0.35)
 - With BER<1e-15, even with a higher tap value, probability of having a burst is negligible (compared to having a single error)
- MTTFPA
 - CAUI-4 data is 64b/66b encoded no transcoding
 - Probability of having two bursts of length >1 in a single frame, with BER<1e-15, is even more negligible
 - Crude calculation: even if every bit error creates such a burst, MTTFPA is >10¹⁷ years
 - Doesn't seem to be an issue

Proposal

- Use Annex 93A for channel specification of CAUI-4 chip-to-chip (Annex 83D)
- Invoke using exact same parameters as Clause 93, except for
 - BER <1e-15
 - 1-tap DFE, with maximum value of 0.75