Annex 83D

(normative)

Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83D–1 shows an example relationship of the CAUI-4 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

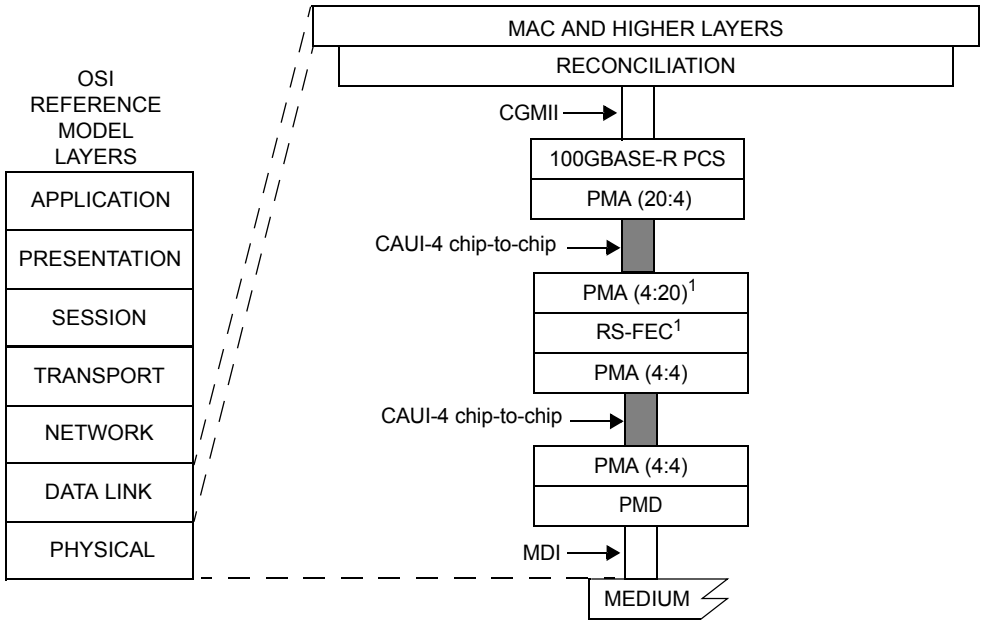

Figure 83D–1—Example CAUI-4 chip-to-chip relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

The CAUI-4 bidirectional link is described in terms of a CAUI-4 transmitter, a CAUI-4 channel, and a CAUI-4 receiver. Figure 83D–2 depicts a typical CAUI-4 application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the informative differential insertion loss budget associated with the chip-to-chip application. The CAUI-4 chip-to-chip interface comprises independent data paths in each direction. Each data path contains four differential lanes which are AC coupled. The nominal signaling rate for each lane is 25.78125 GBd. The CAUI-4 transmitter on each end of the link is adjusted to an appropriate setting

based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an ~~approximate setting with the~~ appropriate setting. The adaptive or adjustable receiver ~~performing~~ performs the remainder of the equalization~~. Operation and control of this receiver is outside the scope of this standard~~.

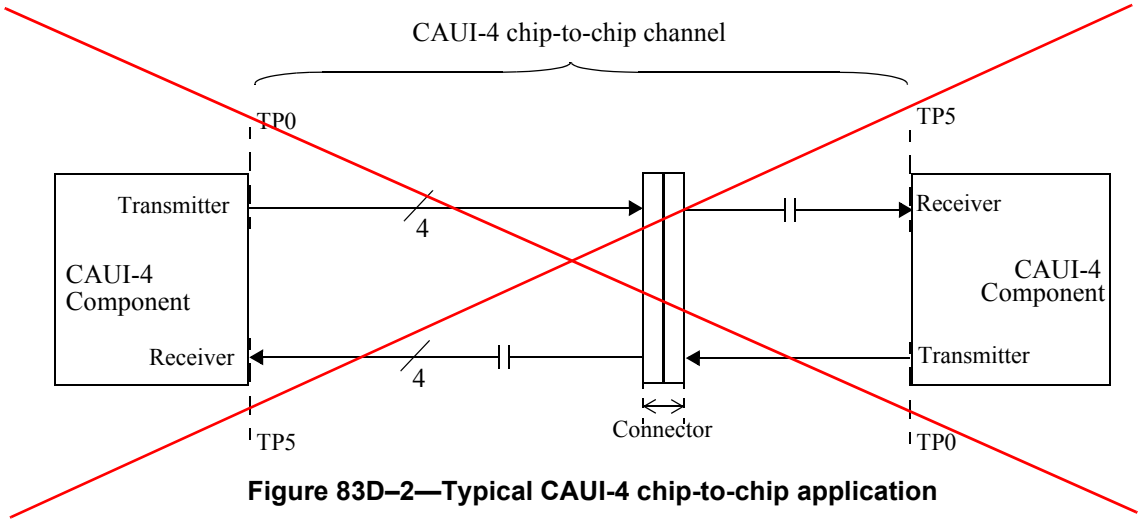

Figure 83D–2—Typical CAUI-4 chip-to-chip application

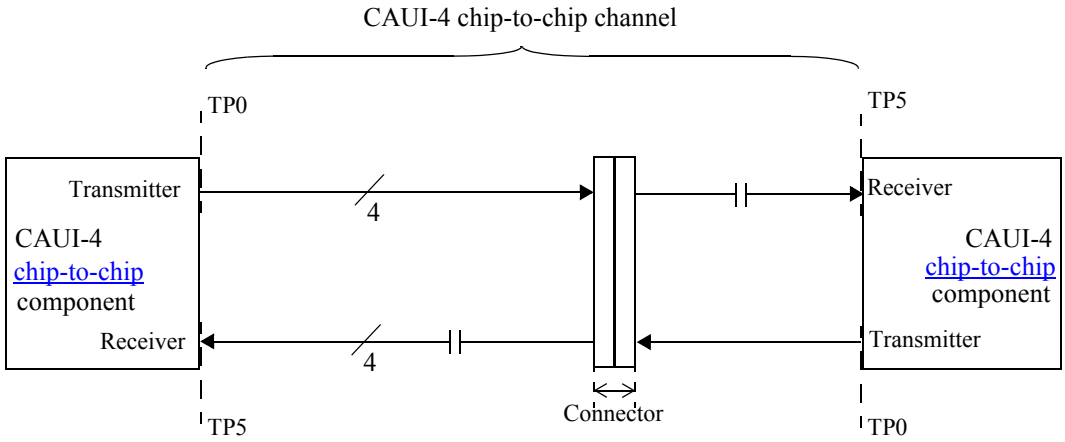

Figure 83D–2—Typical CAUI-4 chip-to-chip application

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower than Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

$$Insertion\_loss(f) \le \begin{cases} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 12.89 \le f < 25.78 \end{cases} \quad \text{(dB)} \qquad \text{(83D–1)}$$

where

f	is the frequency in GHz
Insertion_loss(f)	is the informative CAUI-4 chip-to-chip insertion loss

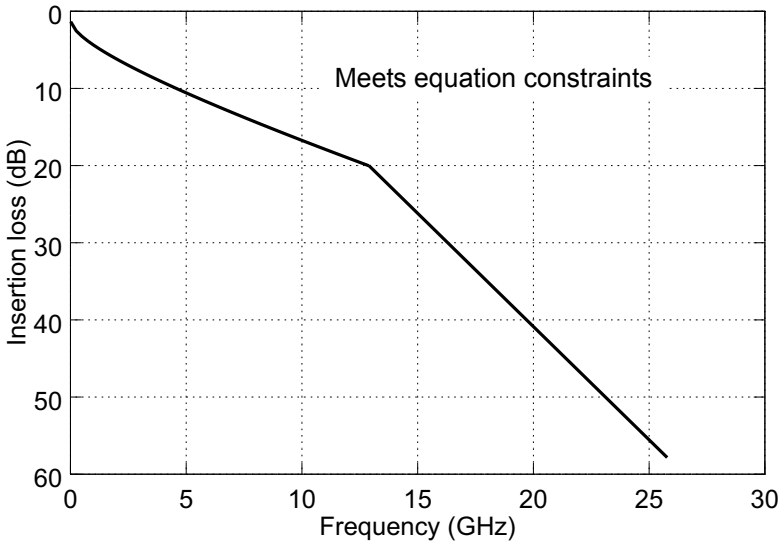

Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss

83D.2 CAUI-4 chip-to-chip compliance point definition

The electrical characteristics for the CAUI-4 chip-to-chip interface are defined at compliance points for the transmitter (TP0a) and receiver (TP5a) respectively. The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93-5 and 93.8.1.1 respectively. The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93-10 and 93.8.2.1 respectively.

83D.3 CAUI-4 chip-to-chip electrical characteristics

83D.3.1 CAUI-4 transmitter characteristics

A CAUI-4 chip-to-chip transmitter shall meet the specifications defined in Table 83D–1 if measured at TP0a. While the CAUI-4 chip-to-chip transmitter requirements are similar to those in Clause 93, they differ in that they do not assume transmitter training or a back-channel communications path. Also, the transmit output waveform is not manipulated via a PMD control function (see 93.7.12).

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

83D.3.1.1 Transmitter equalization settings

The CAUI-4 chip-to-chip transmitter includes programmable equalization to compensate for the frequency-dependent loss of the channel and to facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 83D–4. The transmitter output equalization is characterized using the linear fit method described in 93.8.1.5.1 where the state of the CAUI-4 transmit output is manipulated via management. ~~The pre-cursor tap value c(−1) and the post-cursor tap value c(1)~~

Table 83D–1—CAUI-4 transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	93.8.1.2	25.78125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
~~Common~~AC common-mode ~~AC~~ output voltage (max, RMS)	93.8.1.3	12	mV
Differential output return loss (min)	93.8.1.4	Equation (93-3)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93-4)	dB
Output waveform[a] Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 93.8.1.5.2 93.8.1.5.2 93.8.1.5.2 83D.3.1.1 83D.3.1.1	 0.6 0.4 0.71 x v_f Table 83D–2 Table 83D–3	 V V V — —
Signal-to-noise-and-distortion ratio (min)	93.8.1.6	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak[b] Effective total uncorrelated jitter, peak-to-peak[bc]	92.8.3.~~9~~8	 0.035 0.1 0.26	 UI UI UI

[a]The state of the transmit equalizer is controlled by management interface.
[b]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.9.2 except that the range for fitting $CDFL_i$ and $CDFR_i$, as defined in 92.8.3.~~9~~8.2 c), shall be from 10^{-6} to 10^{-4} ~~to 2.5×10^{-3}~~
[c]Effective total uncorrelated jitter, peak-to-peak is specified to a 10^{-15} probability

~~are controlled independently of each other. The pre-cursor equalization ratio R_{pre} for each pre-cursor tap setting is shown in Table 83D–2 where R_{pre} is defined to be (c(0)–(c(–1))/(c(0)+c(–1)) and the post-cursor tap setting c(1) is 0. The post-cursor equalization ratio R_{pst} for each post-cursor tap setting is shown in Table 83D–3 where R_{pst} is defined to be (c(0)–c(1))/(c(0)+c(1)) and the pre-cursor tap setting c(–1) is 0.~~

The variable *Local_eq_cm1* controls the weight of the pre-cursor tap c(–1). The valid values of *Local_eq_cm1* and their effect are specified in Table 83D–2. The variable *Local_eq_c1* controls the weight of the post-cursor tap c(1). The valid values of *Local_eq_c1* and their effect are specified in Table 83D–3. *Local_eq_cm1* and *Local_eq_c1* are independent of each other and independent on each lane. Each successive step in *Local_eq_cm1* and *Local_eq_c1* value results in a monotonic change in transmitter equalization.

If a Clause 45 MDIO is implemented, ~~the c(–1) and c(1) coefficients~~ *Local_eq_cm1* and *Local_eq_c1* for each lane (0 through 3) and direction (transmit and receive) are accessible through registers 1.180 through 1.187 (see 45.2.1.92b through 45.2.1.92e).

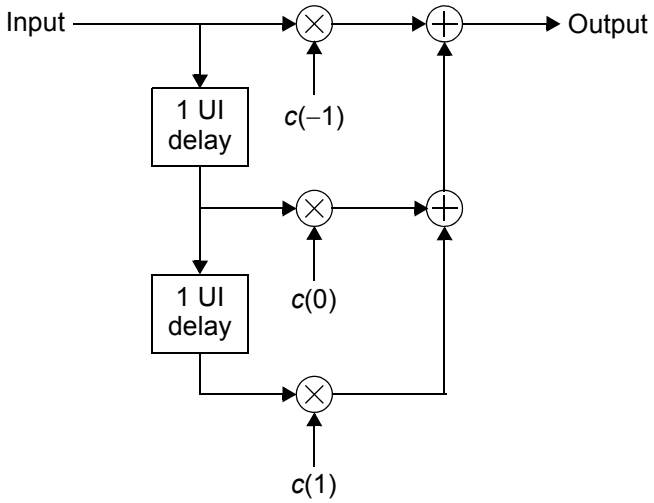

Figure 83D–4—Transmit equalizer functional model

Table 83D–2—~~Pre-cursor equalization~~

~~Pre-cursor equalization setting~~	~~Value~~
~~R_{pre} at tap setting 0~~	~~1 ±12.5%~~
~~R_{pre} at tap setting 1~~	~~1.11 ±12.5%~~
~~R_{pre} at tap setting 2~~	~~1.25 ±12.5%~~
~~R_{pre} at tap setting 3~~	~~1.43 ±12.5%~~

Table 83D–2—Pre-cursor equalization

Local_eq_cm1 value	$\frac{c(-1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04

Table 83D–3—~~Post-cursor equalization~~

~~Post-cursor equalization setting~~	~~Value~~
~~R_{pst} at tap setting 0~~	~~1 ±12.5%~~
~~R_{pst} at tap setting 1~~	~~1.11 ±12.5%~~
~~R_{pst} at tap setting 2~~	~~1.25 ±12.5%~~
~~R_{pst} at tap setting 3~~	~~1.43 ±12.5%~~
~~R_{pst} at tap setting 4~~	~~1.67 ±12.5%~~
~~R_{pst} at tap setting 5~~	~~2 ±12.5%~~

.

Table 83D–3—Post-cursor equalization

Local_eq_c1 value	$\frac{c(1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04
4	–0.2 ±0.04
5	–0.25 ±0.04

83D.3.2 Optional EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-4 shutdown.

If the EEE capability includes CAUI-4 shutdown (see 78.5.2) then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction CAUI-4 transmitter is disabled as specified below. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction CAUI-4 transmitter is disabled as specified below.

For EEE capability with CAUI-4 shutdown, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction.

Furthermore, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction CAUI-4 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction CAUI-4 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in this section.

83D.3.3 CAUI-4 receiver characteristics

A CAUI-4 chip-to-chip receiver shall meet the specifications defined in Table 83D–4 if measured at TP5a.

Table 83D–4—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.2.2	Equation (93-3)	dB
Differential to common mode input return loss	93.8.2.2	Equation (93-5)	dB
Interference tolerance	83D.3.3.1	Table 83D–5	—
~~Jitter tolerance[a]~~	~~93.8.2.4~~	~~Table 93-7~~	~~—~~

[a]~~When referencing 93.8.2.4 the following modifications are required: Test transmitter shown in Figure 93-12 meets 83D.3.1 specifications, test channel meets the requirements of the interference tolerance test channel using Test 2 values from Table 83D–5, bit error ratio better than 10^{-15} for the receiver jitter tolerance test.~~

83D.3.3.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 83D–5. The interference tolerance test uses the method described in Annex 93C as specified by 93.8.2.3, with the following exceptions:

a) The parameters in Table 83D–5 replace the parameters in Table 93-6.

b) The transmitter taps are set via management (see 83D.3.1.1) to the ~~optimal transmitter equalizer~~ settings ~~described in 83D.3.1.1~~that provide the lowest BER.

c) Sinusoidal jitter is added to the test transmitter by modulating the clock source.

83D.3.3.2 Transmitter equalization feedback (optional)

Transmitter equalization feedback is an optional capability for a CAUI-4 chip-to-chip receiver. If implemented, it shall operate as described in this subclause.

Transmitter equalization feedback is generated for each lane (0 through 3) and direction (transmit and receive) independently. The variables that control transmitter equalization feedback are specific for each lane and direction.

A CAUI-4 chip-to-chip receiver may generate a request to change the transmit equalization coefficients of the remote transmitter to new values by setting the *Request_flag* variable to 1. The variables *Request_eq_cm1* and *Request_eq_c1* indicate the request values of *Local_eq_cm1* and *Local_eq_c1*, respec-

Table 83D–5—Receiver interference tolerance parameters

Parameter	Test 1 values			Test 2 values			Units
	Min	Max	Target	Min	Max	Target	
Bit error ratio[ab]	—	10^{-15}		—	10^{-15}		—
Applied pk-pk sinusoidal jitter	Table 88-13			Table 88-13			
Insertion loss at 12.89 GHz[c]	19.5~~—~~	20.5~~20~~		9.5~~—~~	10.5~~10~~		dB
Coefficients of fitted insertion loss[d] a_0 a_1 a_2 a_4	 –1 0 0 0	 2 2.937 1.599 0.03		 –1 0 0 0	 1 0.817 0.801 0.01		 dB dB/GHz$^{1/2}$ dB/GHz dB/GHz^2
~~RSS_DFE4~~RSS_DFE2[e]	0.05	—		0.025	—		—
COM including effects of broad-band noise	—	~~—2~~	2	—	~~—2~~	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3
[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard
[c]Measured between TPt and TP5 (see Figure 93C-4)
[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz
[e]RSS_DFE2 is equivalent to RSS_DFE4 described in 93A.2 except that n_1=2 and n_2=5.

tively, in the remote transmitter (see Table 83D–2 and Table 83D–3). The requested setting may be generated from the remote CAUI-4 chip-to-chip transmitter's equalization setting, which is stored in variables *Remote_eq_cm1* and *Remote_eq_c1*, and from information internal to the receiver, in an implementation specific manner.

When a CAUI-4 chip-to-chip receiver does not request a change of the remote transmitter's transmit equalization setting, it sets the *Request_flag* variable to 0. A CAUI-4 chip-to-chip receiver that does not implement transmitter equalization feedback always sets *Requests_flag* to 0.

If a Clause 45 MDIO is implemented, the variables *Request_flag, Requested_eq_cm1, Requested_eq_c1, Remote_eq_cm1* and *Remote_eq_c1* for each lane and direction are accessible through registers 1.180 through 1.187 (see 45.2.1.92b through 45.2.1.92e).

83D.3.4 Global energy detect function for optional EEE operation

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and CAUI-4 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the CAUI-4 for the ingress direction SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input ~~detects~~ that corresponds to an ALERT signal driven from the CAUI-4 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is ~~applied to the channel~~ received.

83D.4 CAUI-4 chip-to-chip channel characteristics

The Channel Operating Margin (COM), computed using the procedure in Annex 93A and the parameters in Table 83D–6, shall be greater than or equal to 2 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization coefficients.

Table 83D–6—Channel Operating Margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended board capacitance	 C_d z_p z_p C_b	 2.5×10^{-4} 12 30 1.8×10^{-4}	 nF mm mm nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	~~Table 83D–7~~ –12 0 1	dB
Continuous time filter, zero frequency	f_z	~~Table 83D–7~~ $f_b/4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	~~Table 83D–7~~ $f_b/4$ f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 Av A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB

Table 83D–6—Channel Operating Margin parameters *(continued)*

Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	0.3	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2×10^{-48}	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—

Table 83D–7—Reference CTLE coefficients

g_{DC}	f_{p1}	f_{p2}	f_z
-1	18.6	14.1	9.385
-2	18.6	14.1	8.937
-3	15.6	14.1	8.018
-4	15.6	14.1	7.861
-5	15.6	14.1	7.75
-6	15.6	14.1	7.67
-7	15.6	14.1	7.609
-8	15.6	14.1	7.566
-9	15.6	14.1	7.531
-10	15.6	14.1	7.503
-11	15.6	14.1	7.483
-12	15.6	14.1	7.466

83D.5 Example usage of the optional transmitter equalization feedback

83D.5.1 Overview

If implemented, transmitter equalization feedback from a CAUI-4 chip-to-chip receiver may be used to tune the equalization settings of the transmitter at the other end of the CAUI-4 chip-to-chip link to the values

requested by the receiver. An example of a possible transmitter equalization tuning process using transmitter equalization feedback is provided in this subclause.

In this example, two components, A and B, are connected by a CAUI-4 chip-to-chip link, such that A is closest to the PCS and B is closest to the PMD. Clause 45 MDIO is implemented by both components, with component A at device address 11 and component B at device address 10. Transmitter equalization feedback is implemented by either component A, component B, or both. One Station Management (STA) controls both components.

Figure 83D–5 depicts the components of the CAUI-4 chip-to-chip link and the registers used during the tuning procedure.

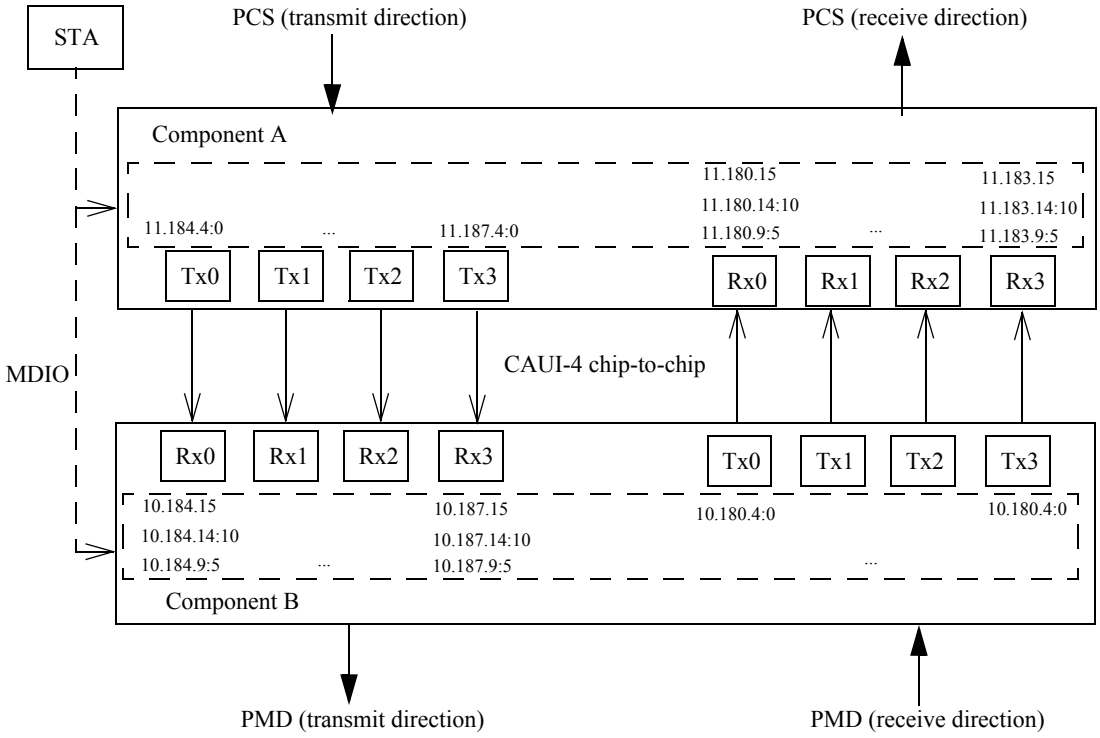

Figure 83D–5—Example transmitter equalization feedback components and registers

The STA performs the procedures described in 83D.5.2 and 83D.5.3 to tune lane 0 equalization settings in both sides of the CAUI-4 chip-to-chip link. When these procedures are completed, the STA uses similar procedures to tune equalization settings in lanes 1 through 3. When all lanes are tuned, the STA may repeat the process with another pair of components connected by CAUI-4 chip-to-chip.

Note—Using non-optimal transmitter equalization settings (or changing them) during the tuning procedure may interrupt data communication. The CAUI-4 bit error ratio is assumed to meet the requirements of 83D.3.3.1 upon completion of the tuning process.

83D.5.2 Tuning equalization settings on lane 0 in the transmit direction

1) Read *Local_eq_cm1* (11.184.1:0) and *Local_eq_c1* (11.184.4:2) from component A.

2) Write *Local_eq_cm1* and *Local_eq_c1* read from component A to *Remote_eq_cm1* (10.184.6:5) and *Remote_eq_c1* (10.184.9:7), respectively, in component B.
3) Read *Request_flag* (10.184.15), *Requested_eq_cm1* (10.184.11:10) and *Requested_eq_c1* (10.184.14:12) from component B.
4) If *Request_flag* is 0, go to tuning equalization settings on lane 0 in the Receive direction (83D.5.3)
5) If *Request_flag* is 1, write *Requested_eq_cm1* and *Requested_eq_c1* read from component B to *Local_eq_cm1* (11.184.1:0) and *Local_eq_c1* (11.184.4:2), respectively, in component A.
6) Go to step 1.

83D.5.3 Tuning equalization settings on lane 0 in the receive direction

1) Read *Local_eq_cm1* (10.180.1:0) and *Local_eq_c1* (10.180.4:2) from component B.
2) Write *Local_eq_cm1* and *Local_eq_c1* read from component B to *Remote_eq_cm1* (11.180.6:5) and *Remote_eq_c1* (11.180.9:7), respectively, in component A.
3) Read *Request_flag* (11.180.15), *Requested_eq_cm1* (11.180.11:10) and *Requested_eq_c1* (11.180.14:12) from component A.
4) If *Request_flag* is 0, proceed to tuning lane 1.
5) If *Request_flag* is 1, write *Requested_eq_cm1* and *Requested_eq_c1* read from component A to *Local_eq_cm1* (10.180.1:0) and *Local_eq_c1* (10.180.4:2), respectively, in component B.
6) Go to step 1.

83D.6 Protocol implementation conformance statement (PICS) proforma for Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[8]

83D.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83D.6.2 Identification

83D.6.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83D.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bm-201x, Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

83D.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83D.1	Four independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	83D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*LPI	Support for CAUI-4 shutdown	83D.3.2		O	Yes [ ] No [ ]

83D.6.4 PICS proforma tables for chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.6.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	83D.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	83D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	83D.3.1	less than our equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	83D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode ~~output~~output voltage	83D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	83D.3.1	Meets Equation (93-3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	83D.3.1	Meets Equation (93-4) constraints	M	Yes [ ]
TC8	Output ~~wave form~~waveform	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Amplitude and swing for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ]
TC11	Transmit disable for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ]

83D.6.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	93.8.2.2	Meets Equation (93-3) constraints	M	Yes [ ]
RC2	Differential to common mode input return loss	93.8.2.2	Meets Equation (93-5) constraints	M	Yes [ ]
RC3	Interference tolerance	83D.3.3.1	Satisfy requirements in Table 83D–5	M	Yes [ ]
RC4	Jitter Tolerance	93.8.2.4	Satisfy requirements in Table 93-7	M	Yes [ ]
RC5	Signal detect for CAUI-4 shutdown	83D.3.4		LPI:M	Yes [ ]

83D.6.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	83D.4	Greater than or equal to 2 dB	CHAN:M	Yes [ ]