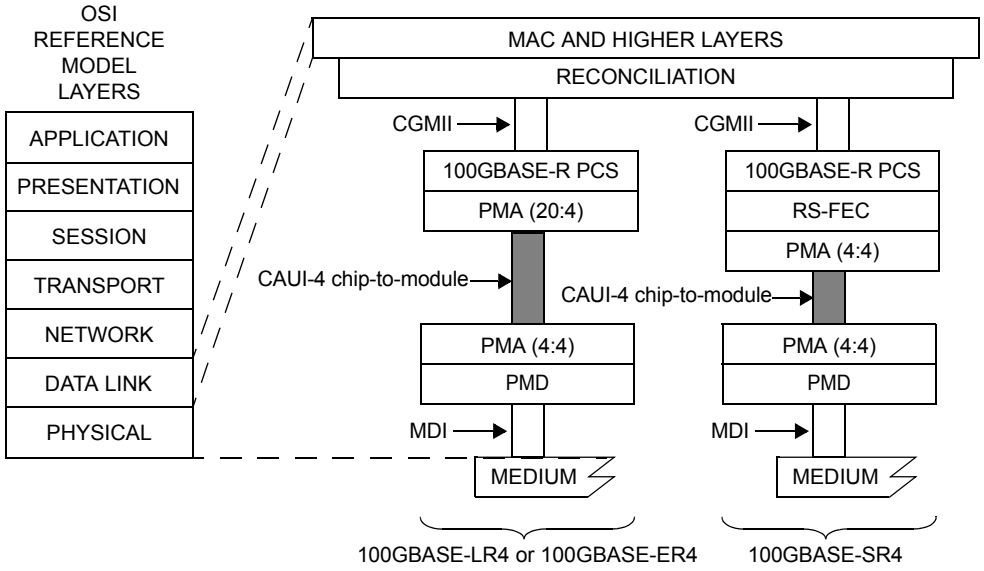
Annex 83E

(normative)

Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83E–1 shows the relationship of the CAUI-4 chip-to-module interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with pluggable module interfaces.



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83E–1—Example CAUI-4 chip-to-module relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

The CAUI-4 link is described in terms of a host CAUI-4 component, a CAUI-4 channel with associated insertion loss, and a module CAUI-4 component. Figure 83E–2 and Equation (83E–1) depict a typical CAUI-4 application, and summarize the differential insertion loss budget associated with the chip-to-module application which is shown in Figure 83E–3. The CAUI-4 chip-to-module interface comprises independent data paths in each direction. Each data path contains four differential lanes which are AC coupled within the module. The nominal signaling rate for each lane is 25.78125 GBd. The chip-to-module interface is defined

using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [Bx1].

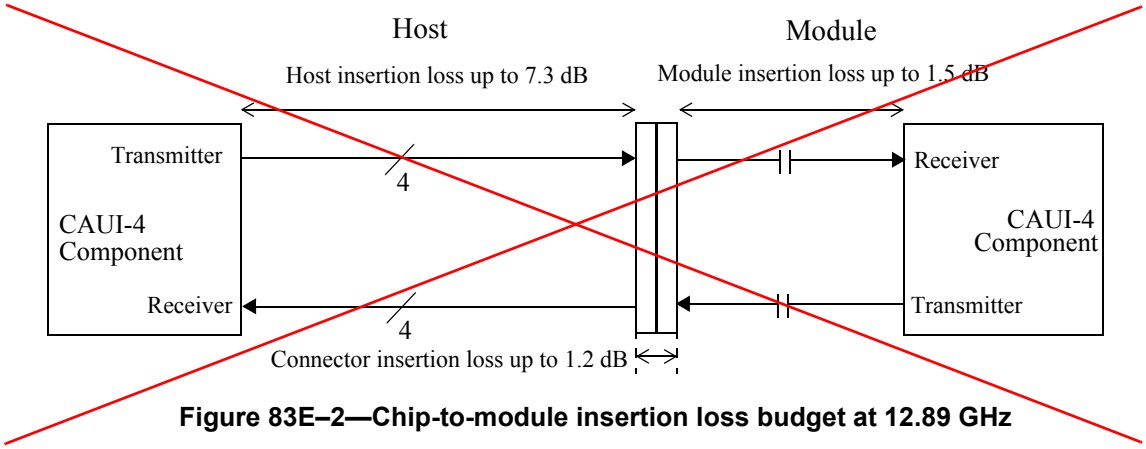


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

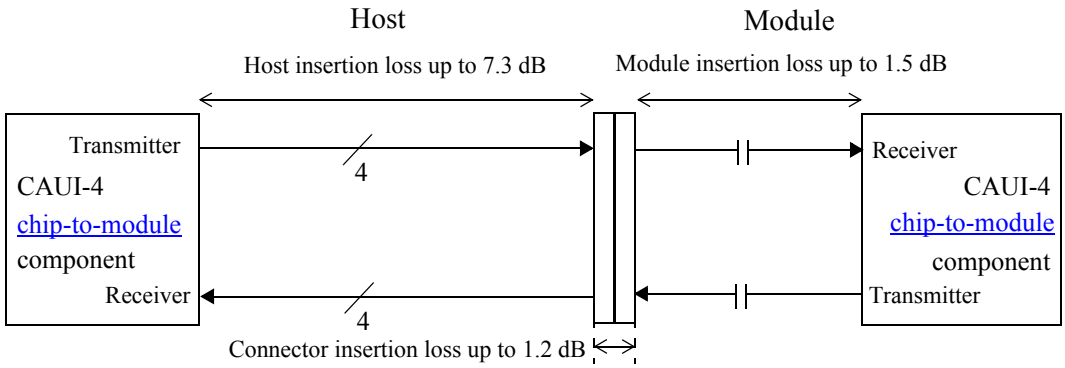


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f < 18.75 \end{cases} \quad \text{(dB)} \qquad \text{(83E–1)}$$

where

f	is the frequency in GHz
Insertion_loss(f)	is the CAUI-4 chip-to-module insertion loss

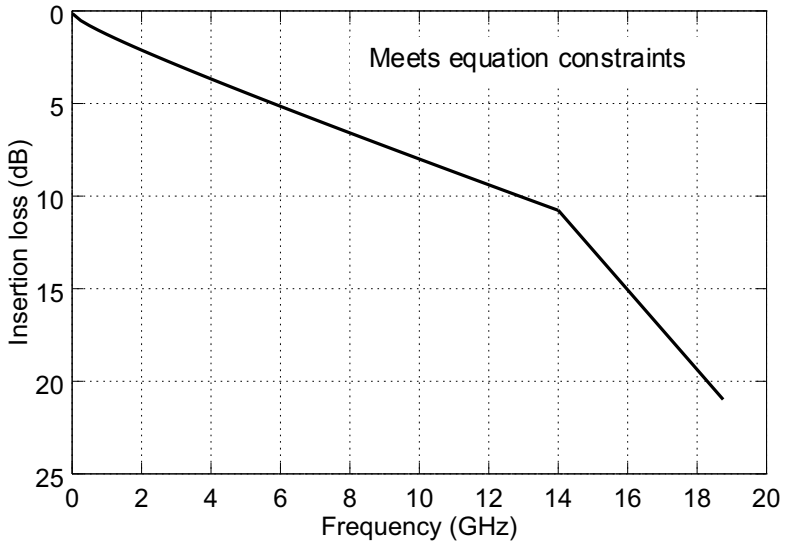


Figure 83E–3—CAUI-4 chip-to-module channel insertion loss

83E.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-15}.

83E.2 CAUI-4 chip-to-module compliance point definitions

The electrical characteristics for the CAUI-4 chip-to-module interface are defined at compliance points for the Host and Module respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 83E–4 depicts the location of compliance points when measuring Host CAUI-4 compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. Similarly, the input of the HCB at TP4a is used to verify the host input compliance.

Figure 83E–5 depicts the location of compliance points when measuring Module CAUI-4 compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. Similarly, the input of the MCB at TP1 is used to verify the module input compliance. Additional details on

the requirements for the MCB and HCB are given in 83E.4.1

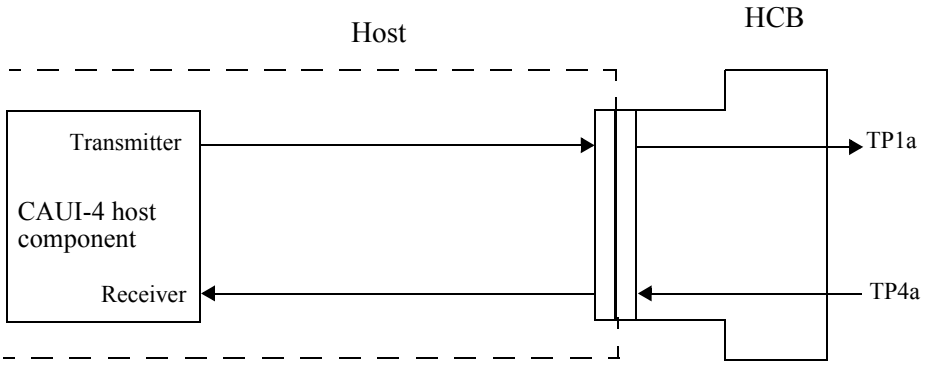


Figure 83E–4—Host CAUI-4 Compliance Points

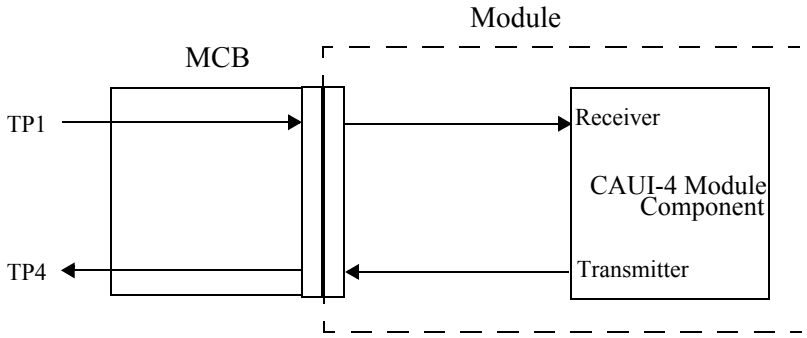


Figure 83E–5—Module CAUI-4 Compliance Points

83E.3 CAUI-4 chip-to-module electrical characteristics

83E.3.1 CAUI-4 host output characteristics

A CAUI-4 host output shall meet the specifications defined in Table 83E–1 if measured at TP1a.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

83E.3.1.1 Signaling rate and range

The CAUI-4 signaling rate is 25.78125 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 38.787879 ps.

Table 83E–1—CAUI-4 host output characteristics (at TP1a)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
DC common-mode output voltage (max)	83E.3.1.2	2.8	V
DC common-mode output voltage (min)	83E.3.1.2	–0.3	V
Single-ended output voltage (max)	83E.3.1.2	3.3	V
Single-ended output voltage (min)	83E.3.1.2	–0.4	V
AC c~~C~~ommon-mode ~~AC~~ output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	83E.3.1.2	 35 900	mV
Eye width (min)	83E.3.1.6	0.46	UI
Eye height A, differential (min)	83E.3.1.6	95	mV
Eye height B, differential (min)	83E.3.1.6	80	mV
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	10	ps

83E.3.1.2 Signal levels

The peak-to-peak differential voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 83E–6.

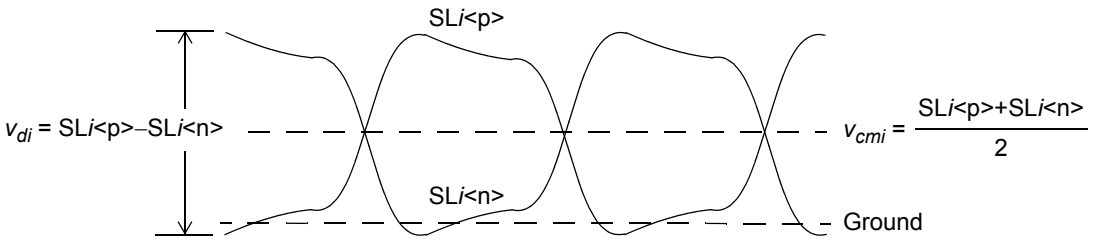


Figure 83E–6—Voltage definitions

The peak-to-peak differential output voltage is less than or equal to 900 mV. The peak-to-peak differential output voltage is less than or equal to 35 mV when the transmitter is disabled.

The DC common-mode output voltage ~~is between −0.3 V~~ and ~~2.8 V with respect to signal ground. The~~ AC common-mode output voltage ~~is less than or equal to 17.5 mV RMS~~ are defined with respect to signal ground.

83E.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (83E–2) and illustrated in Figure 83E–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(83E–2)}$$

where

f is the frequency in GHz
RLd is the CAUI-4 chip-to-module host output differential return loss

Common to differential output conversion return loss, in dB, of the output is shown in Equation (83E–3) and illustrated in Figure 83E–8

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(83E–3)}$$

where

f is the frequency in GHz
RLdc is the CAUI-4 chip-to-module output common to differential mode conversion return loss

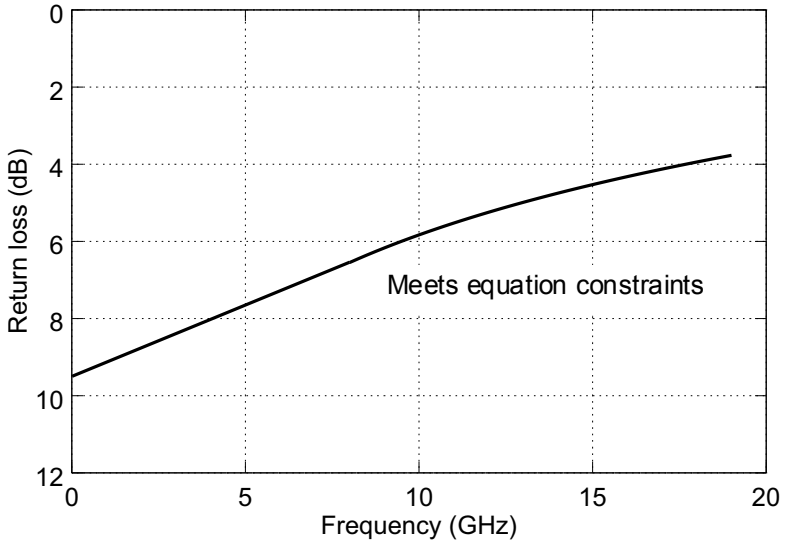


Figure 83E–7—Output differential return loss

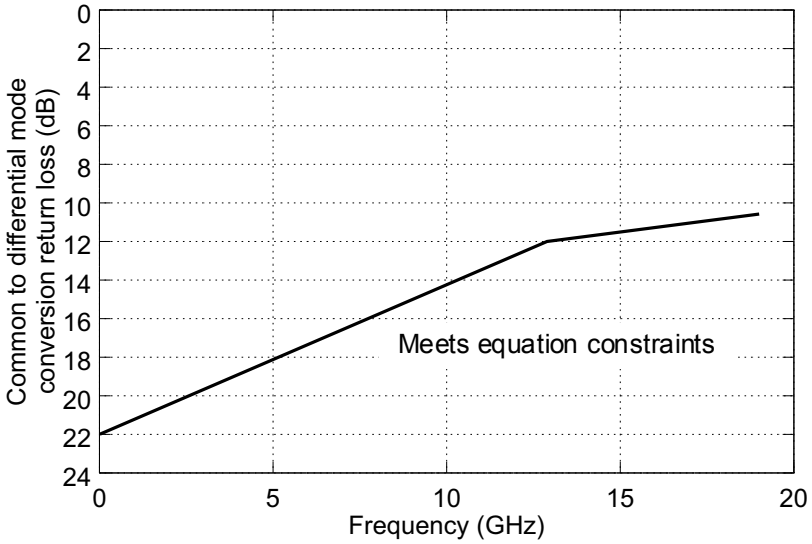


Figure 83E–8—Output common to differential mode conversion return loss

83E.3.1.4 Differential termination mismatch

Differential termination mismatch is defined in 86A.5.3.2.

83E.3.1.5 Transition time

The transition times (rise and fall times) are defined in 86A.5.3.3.

83E.3.1.6 Host output eye width and eye height

Host output eye width is greater than 0.46 UI. Host output eye height is greater than 95 mV. Figure 83E–9 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 83E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.1.6.1. The recommended CTLE peaking value (which is also used for host output eye measurements) is provided to the module via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and target transition time of ~~19~~12 ps.

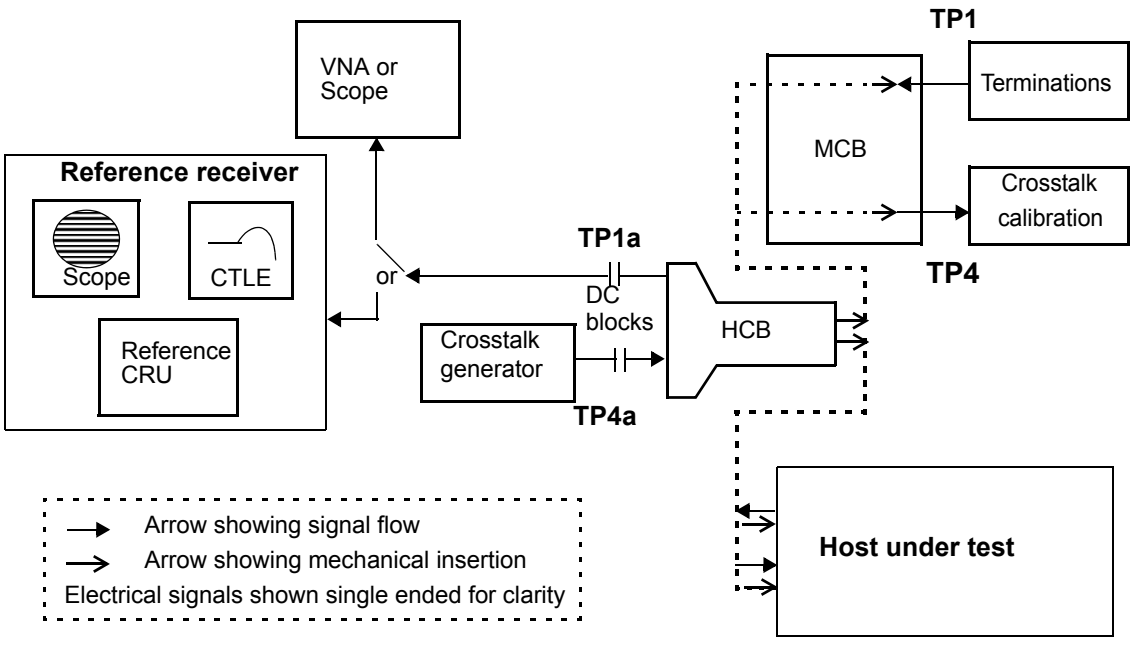


Figure 83E–9—Example host output test configuration

83E.3.1.6.1 Reference receiver for host output eye width and eye height evaluation

The reference receiver is used to measure host eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4) with coefficients given in Table 83E–2 and illustrated in Figure 83E–10. The equalizer may be implemented in software, however the measured signal is not averaged.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{\mathrm{j}2\pi f + Z_1}{(\mathrm{j}2\pi f + P_1)(\mathrm{j}2\pi f + P_2)} \quad (83E\text{–}4)$$

where

$H(f)$	is the CTLE transfer function
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
j	is the square root of –1
f	is the frequency in GHz

Table 83E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

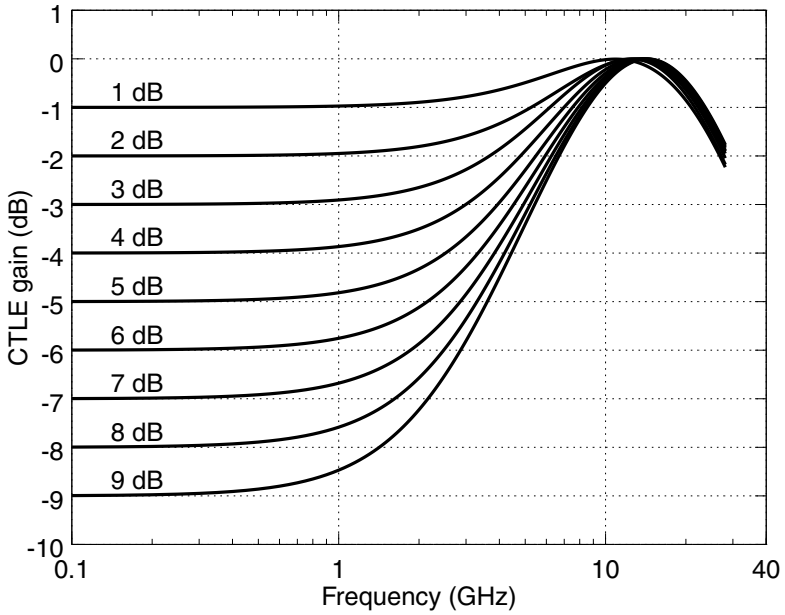


Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic

83E.3.2 CAUI-4 module output characteristics

A CAUI-4 module output shall meet the specifications defined in Table 83E–3 if measured at TP4. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Table 83E–3—CAUI-4 module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
~~Common~~AC common-mode ~~AC~~ output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential output voltage (max)	83E.3.1.2	900	mV
Eye width (min)	83E.3.2.1	0.57	UI
Eye height, differential (min)	83E.3.2.1	228	mV
Vertical eye closure (max)	83E.4.2.1	5.5	dB
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB

Table 83E–3—CAUI-4 module output characteristics (at TP4) *(continued)*

Parameter	Reference	Value	Units
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	~~9.5~~12	ps
DC common mode voltage (min)[a]	83E.3.1.2	–350	mV
DC common mode voltage (max)[a]	83E.3.1.2	2850	mV

[a]DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

83E.3.2.1 Module output eye width and eye height

Module output eye width is greater than 0.57 UI. Module output eye height is greater than 228 mV. Figure 83E–11 depicts an example module output eye width and eye height test configuration. Module output eye width and eye height are measured at TP4 using compliance boards defined in 83E.2. The module output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.2.1.1. Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

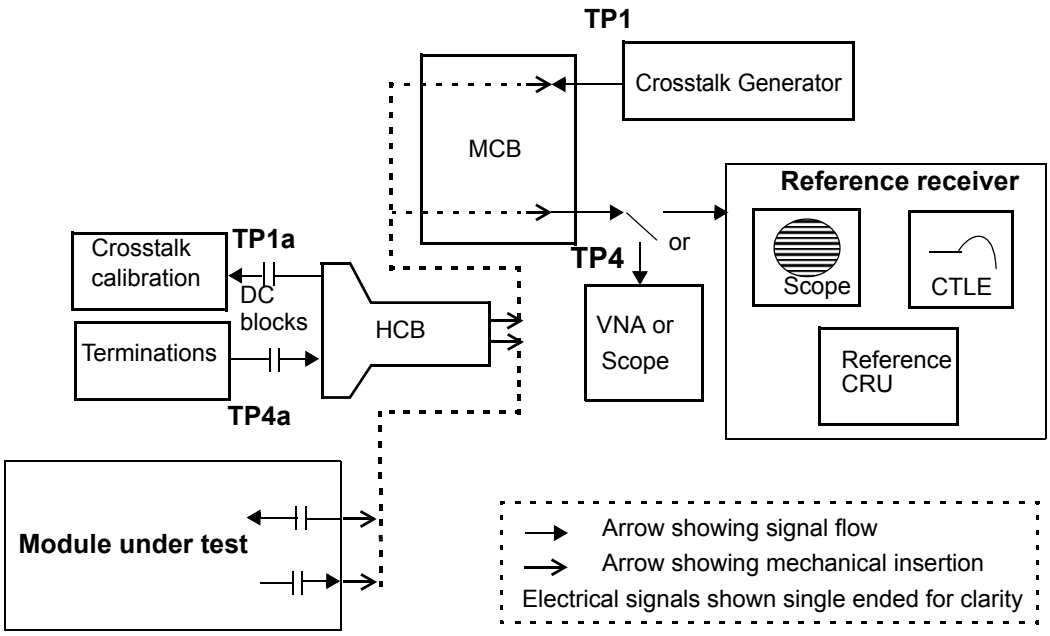


Figure 83E–11—Example module output test configuration

83E.3.2.1.1 Reference receiver for module output eye width and eye height evaluation

A reference receiver is used to measure module eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4) with coefficients given in the first two rows of Table 83E–2. The equalizer may be implemented in software, however the measured signal is not averaged. Either of the two equalizer settings may be used to meet the output eye width and eye height requirement.

83E.3.3 CAUI-4 host input characteristics

A CAUI-4 host input shall meet the specifications defined in Table 83E–4 if measured at the appropriate test point.

Table 83E–4—CAUI-4 host input characteristics

Parameter	Reference	Test point	Value	Units
~~Bit error ratio (max)~~[a]	~~83E.3.3.1~~	~~TP4a~~	~~10^{-15}~~	
Signaling rate, per lane (range)	83E.3.1.1	TP4a	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP4	900	mV
Differential input return loss (min)	83E.3.3.2	TP4a	Equation (83E–5)	dB
Differential to common mode input return loss (min)	83E.3.3.2	TP4a	Equation (83E–6)	dB
Host stressed input test[b]	83E.3.3.3	TP4	See 83E.3.3.3	
Differential termination mismatch (max)	83E.3.1.4	TP4a	10	%
Common-mode voltage[c] Min Max	83E.3.1.2	TP4a	 –0.3 2.8	V

[a] ~~Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard.~~
[b] Meets BER specified in 83E.1.1.
[c] Generated by host, referred to host ground.

83E.3.3.1 ~~Input bit error ratio~~

~~The CAUI-4 chip-to-module host input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.3.3.~~

83E.3.3.2 Input return loss

The differential input return loss, in dB, of the input is shown in Equation (83E–5) and illustrated in Figure 83E–12. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \quad \text{(dB)} \qquad \text{(83E–5)}$$

where

f is the frequency in GHz
RLd is the CAUI-4 chip-to-module input differential return loss

Differential to common mode input return loss, in dB, of the input is shown in Equation (83E–6) and illustrated in Figure 83E–13.

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \quad \text{(dB)} \qquad \text{(83E–6)}$$

where

f is the frequency in GHz
$RLcd$ is the CAUI-4 chip-to-module input differential to common mode input return loss

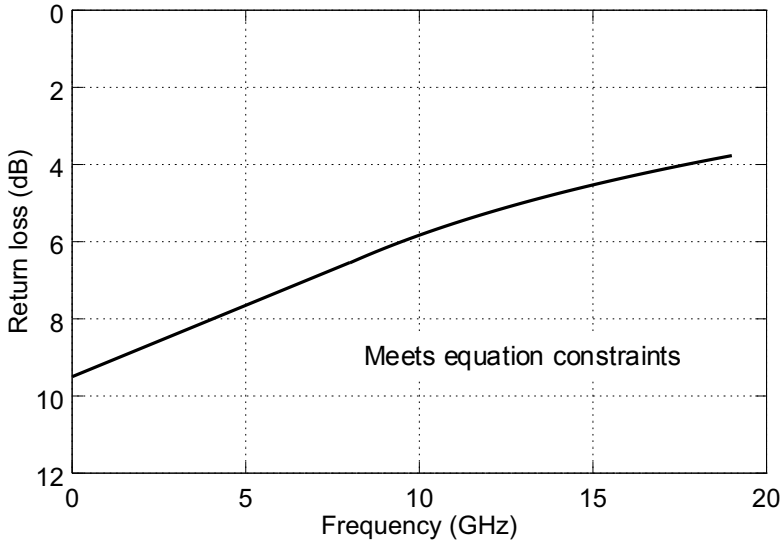


Figure 83E–12—Differential input return loss

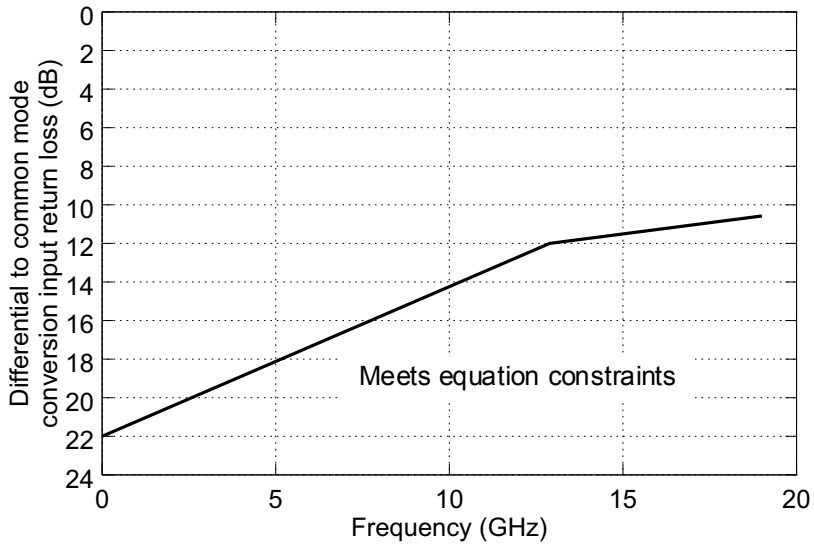


Figure 83E–13—Differential to common mode conversion input return loss

83E.3.3.3 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 83E.3.3.3.1. The input shall satisfy the input tolerance defined in Table 83E–5.

Table 83E–5—Host stressed input parameters

Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye height	228 mV

83E.3.3.3.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 83E–14. The stress signal is applied at TP4a, and is calibrated at TP4. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9, see Table 86-11 and Table 68-6). The reference receiver includes a selectable software CTLE given by Equation (83E–4) and the first two rows of Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern. The amount of applied peak-to-peak sinusoidal jitter used for the host stressed input test is given in Table 83E–5. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and ~~PRBS11~~PRBS9. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 GBd).

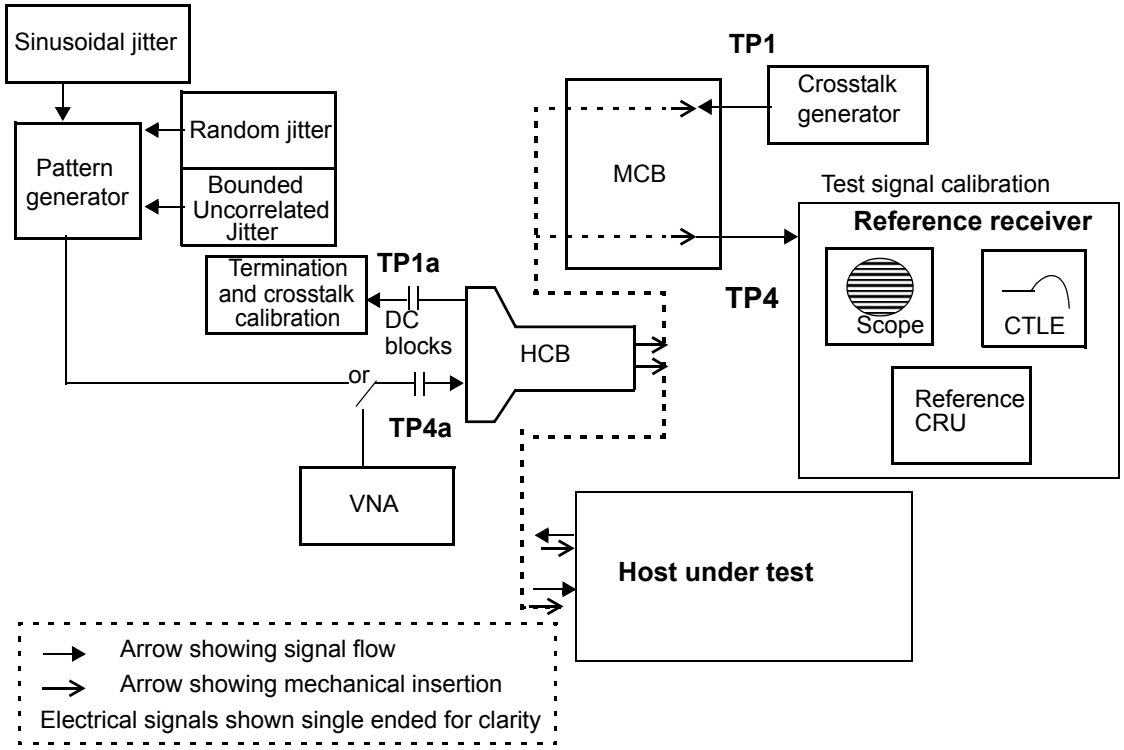


Figure 83E–14—Example host stressed input test

The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–6~~. The target pattern generator 20% to 80% transition in the host stressed input test is 9.5 ps~~.

Table 83E–6—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total jitter at BER of 10^{-15}
[b]Random jitter at BER of 10^{-15}
[c]As defined in 92.8.3.10.1

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP1a. The crosstalk signal is calibrated with Pattern 4~~ (PRBS9, see Table 86-11)~~. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the stressed input test. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least

31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

~~Eye height and eye width are then measured at TP4 using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude is adjusted to result in the eye height and eye width given in Table 83E–5 using the reference receiver.~~

Eye height and eye width, extrapolated to a probability of 10^{-15}, are then measured at TP4 based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the receiver's differential pk-pk input voltage tolerance specification as shown in Table 83E–4) to result in the eye height and eye width given in Table 83E–5 using the reference receiver with the setting of the CTLE which maximizes the product of eye height and eye width.

A host input test signal should have a vertical eye closure in the range of 4.5 dB to 5.5 dB with a target value of 5 dB.

The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the HCB into the host under test.

83E.3.4 CAUI-4 module input characteristics

A CAUI-4 module input shall meet the specifications defined in Table 83E–7 if measured at the appropriate test point.

Table 83E–7—CAUI-4 module input characteristics

Parameter	Reference	Test point	Value	Units
~~Bit error ratio (max)[a]~~	~~83E.3.4.1~~	~~TP1~~	~~10^{-15}~~	
Signaling rate per lane (range)	83E.3.1.1	TP1	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP1a	900	mV
Differential input return loss (min)	83E.3.3.2	TP1	Equation (83E–5)	dB
Differential to common mode input return loss (min)	83E.3.3.2	TP1	Equation (83E–6)	dB
Differential termination mismatch (max)	83E.3.1.4	TP1	10	%
Module stressed input test[b]	83E.3.4.2	TP1a	See 83E.3.4.2	
Single-ended voltage tolerance range (min)	83E.3.1.2	TP1a	–0.4 to 3.3	V
~~Single-ended voltage tolerance (max)~~	~~83E.3.1.2~~	~~TP1a~~	~~3.3~~	~~V~~
DC common mode voltage (min)[c]	83E.3.1.2	TP1	–350	mV
DC common mode voltage (max)[c]	83E.3.1.2	TP1	2850	mV

[a] ~~Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard.~~

[b] Meets BER specified in 83E.1.1.

[c] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

83E.3.4.1 ~~Input bit error ratio~~

~~The CAUI-4 module input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.4.2.~~

83E.3.4.2 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 83E.3.4.2.1. The input shall satisfy the input tolerance defined in Table 83E–8.

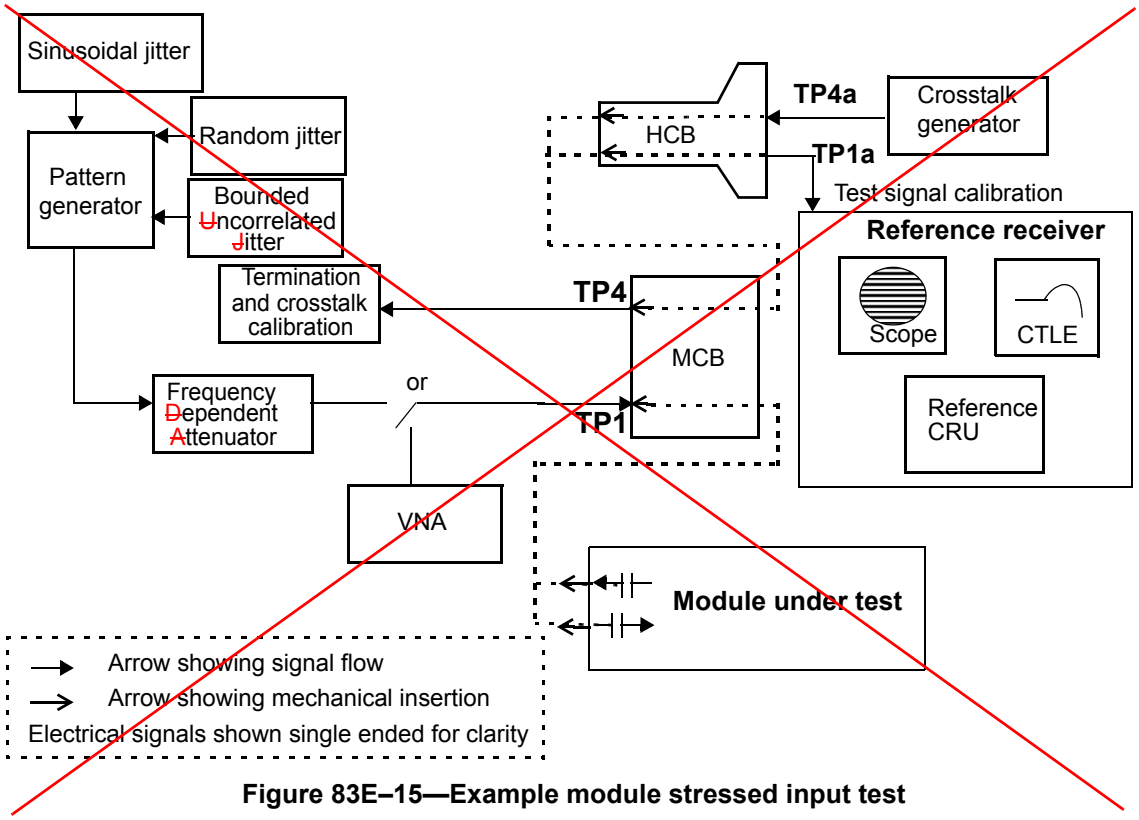


Figure 83E–15—Example module stressed input test

Table 83E–8—Module stressed input parameters

Parameter	Value
Eye width	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye height	95 mV

83E.3.4.2.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 83E–15. The stress signal is applied at TP1, and is calibrated at TP1a. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 ~~(PRBS9, see Table 86-11)~~. The reference receiver includes a selectable software CTLE given by Equation (83E–4) and Table 83E–2. The stressed signal is generated by

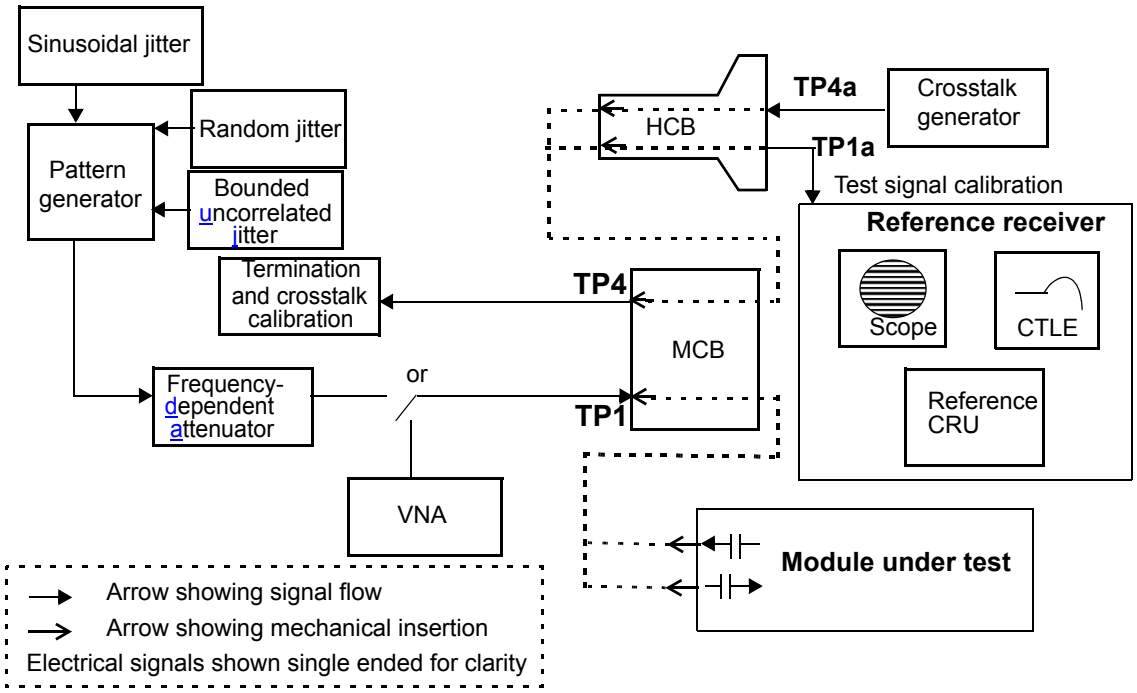


Figure 83E–15—Example module stressed input test

adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel, and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 83E–8. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and ~~PRBS11~~PRBS9. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–9. The target pattern generator 20% to 80% transition time in the module stressed input test is 9.5 ps. The return loss of the test system as measured at TP1 meets the specification given in Equation (83E–2).

Table 83E–9—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total jitter at BER of 10^{-15}
[b]Random jitter at BER of 10^{-15}
[c]As defined in 92.8.3.10.1

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP4. The crosstalk signal is calibrated with Pattern 4 ~~(PRBS9, see Table 86-11)~~. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the stressed input test. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes being active during the stressed input test.

Two levels of frequency dependent attenuation are used for the module stressed input test: high loss, and low loss. For the high loss case, frequency dependent attenuation is added such that from the output of the pattern generator to TP1a is ~~10.25~~13.8 dB loss at 12.89 GHz. The 13.8 dB loss represents 10.25 dB channel loss with an additional allowance for host transmitter package loss. Eye height and eye width, extrapolated to a probability of 10^{-15}, are then measured at TP1a ~~using the setting of the software CTLE which maximizes the product of eye height and eye width~~ based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the receiver's differential pk-pk input voltage tolerance specification as shown in Table 83E–7) to result in the eye height and eye width given in Table 83E–8 using the reference receiver with the setting of the CTLE which maximizes the product of eye height and eye width. For the low loss case, discrete frequency dependent attenuation is removed such that from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width ~~are then measured~~ at TP1a ~~using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude~~ are then adjusted ~~to result~~ in the ~~eye height and eye width given in Table 83E–8 using~~ same way as described for the ~~reference receiver~~ high loss case. In both the low loss and high loss cases, the module under test is provided with the reference CTLE setting used to meet eye width and eye height requirements via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). The module under test ~~is evaluated with~~ shall meet the BER requirement as described in Table 83E–7 using three *Recommended_CTLE_value* values for both the high loss test and low loss test. These are: a) the CTLE setting used to meet eye width and eye height requirements, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2. Modules may optionally elect not to use the *Recommended_CTLE_value.*

The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the module into the MCB.

83E.4 CAUI-4 measurement methodology

This subclause describes common measurement tools and methodologies to be used for the CAUI-4 chip-to-module interface. Details of HCB and MCB characteristics are given in 83E.4.1 and details of the eye diagram measurement methodology are given in 83E.4.2.

83E.4.1 HCB / MCB characteristics

HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture. The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture.

83E.4.2 Eye width and eye height measurement method

Eye diagrams in CAUI-4 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a select-

able continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is Pattern 4 ~~(PRBS9, see Table 86-11)~~. The following procedure should be used to obtain eye height and eye width parameters:

1) Capture Pattern 4 using a clock recovery unit with a corner frequency of 10 MHz and slope of 20 dB/decade and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.

2) Apply the reference receiver including the appropriate CTLE to the captured signal. For modules, any single CTLE setting as described in 83E.3.2.1.1 which meets both eye width and eye height requirements is acceptable. For host compliance, the CTLE peaking in the reference receiver shall be set to ~~one of~~ three values. These are: a) the recommended CTLE peaking value provided by the host, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2. ~~Any of~~ A compliant host passes both the ~~three CTLE settings that meets both~~ eye width and eye height A limit specified in Table 83E–1 using at least one of the settings, and passes eye height B ~~defined~~ in Table 83E–1 ~~is acceptable.~~at all of the two or three settings.

3) Use the differential equalized signal from step 2 to construct the CDF of the jitter zero crossing for both the left edge (CDFL) and right edge (CDFR), as a distance from the center of the eye. Calculate the eye width (EW6) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits. For a pattern with 50% transition density the maximum value for the CDFL and CDFR will be 0.5. The CDFL and CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.

4) Leveraging the Dual-Dirac jitter model described in 48B.1.1, estimate the random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield the random jitter on the left edge (RJL) and the random jitter on the right edge (RJR) respectively. The eye width is then given by Equation (83E–7)

$$EW15 = EW6 - 3.19 \times (RJR + RJL) \quad \text{(83E–7)}$$

where

$EW15$	is the eye width extrapolated to 10^{-15} probability
$EW6$	is the eye width at 10^{-6} probability
RJL	is the RMS value of the jitter estimated from CDFL
RJR	is the RMS value of the jitter estimated from the CDFR

5) Use the differential equalized signal from step 2 to construct the CDF of the signal voltage in the central 5% of the eye, for both logic 1 (CDF1) and logic 0 (CDF0), as a distance from the center of the eye. Calculate the eye height (EH6) as the difference in voltage between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the voltage at the top and bottom of the eye normalized by the total number of sampled bits. For a well balanced number of ones and zeros the maximum value for CDF0 and CDF1 will be 0.5.

6) Apply the Dual-Dirac and tail fitting techniques to CDF1 and CDF0 to estimate the noise at the middle of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} and 10^{-6} of CDF1 and CDF0 to yield relative noise one (RN1) and relative noise zero (RN0). The eye height is then given by Equation (83E–8)

$$EH15 = EH6 - 3.19 \times (RN0 + RN1) \quad \text{(83E–8)}$$

where

$EH15$	is the eye height extrapolated to 10^{-15} probability
$EH6$	is the eye height at 10^{-6} probability
$RN1$	is the RMS value of the noise estimated from CDF1
$RN0$	is the RMS value of the noise estimated from CDF0

83E.4.2.1 Vertical eye closure

Vertical eye closure is calculated using Equation (83E–9)

$$VEC = 20\log\left(\frac{AV}{EH15}\right) \quad \text{(83E–9)}$$

where

VEC	is vertical eye closure in dB
AV	is the eye amplitude of the equalized waveform. Eye amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye
$EH15$	is given in equation Equation (83E–8)

83E.5 Protocol implementation conformance statement (PICS) proforma for Annex 83E, Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[9]

83E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83E, Chip-to-module four-lane 100 Gb/s Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83E.5.2 Identification

83E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bm-201x, Annex 83E, Chip-to-module four-lane 100 Gb/s Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

Date of Statement	

[9]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

83E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83E.1	Four independent data paths in each direction	M	Yes [ ]
BER	Meets CAUI-4 BER requirement	83E.1.1	10^{-15}	M	Yes [ ]
ADR	Adaptive receiver	83E.3.4.2.1	Module CAUI-4 receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

83E.5.4 PICS proforma tables for chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	83E.3.1.2	less than our equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	~~83E.3.1.2~~ 83E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode ~~output~~output voltage	~~83E.3.1.2~~ 83E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	83E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	83E.3.1.6	0.46 UI	M	Yes [ ]
TH12	Eye height	83E.3.1.6	95 mV	M	Yes [ ]
TH13	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3 or valid 100GBASE-R signal	M	Yes [ ]

83E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode ~~output~~output voltage	83E.3.1.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	83E.3.1.4	Less than 10%	M	Yes [ ]
TM8	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TM9	Eye width	83E.3.1.6	0.57 UI	M	Yes [ ]
TM10	Eye height	83E.3.1.6	228 mV	M	Yes [ ]
TM11	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3 or valid 100GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	83E.4.2.1	5.5 dB (max)	M	Yes [ ]

83E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	CAUI-4 host input characteristics	83E.3.3	Table 83E–4	M	Yes [ ]
~~RH1~~	~~BER~~	~~83E.3.3.1~~	~~10^{-15}~~	~~M~~	~~Yes [ ]~~
~~RH2~~	~~Differential input return loss~~	~~83E.3.3.2~~	~~Equation (83E–5)~~	~~M~~	~~Yes [ ]~~
~~RM3~~	~~Reference impedance for input return loss~~	~~83E.3.3.2~~	~~100 Ω.~~	~~M~~	~~Yes [ ]~~
~~RH4~~	~~Differential to common mode input return loss~~	~~83E.3.3.2~~	~~Equation (83E–6)~~	~~M~~	~~Yes [ ]~~
~~RH5~~	~~Stressed input test~~	~~83E.3.3.3~~	~~Satisfy requirements in Table 83E–5~~	~~M~~	~~Yes [ ]~~

83E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	CAUI-4 module input characteristics	83E.3.4	Table 83E–7	M	Yes [ ]
~~RM1~~	~~BER~~	~~83E.3.3.1~~	~~10^{-15}~~	~~M~~	~~Yes [ ]~~
~~RM2~~	~~Differential input return loss~~	~~83E.3.3.2~~	~~Equation (83E–5)~~	~~M~~	~~Yes [ ]~~
~~RM3~~	~~Reference impedance for input return loss~~	~~83E.3.3.2~~	~~100 Ω.~~	~~M~~	~~Yes [ ]~~
~~RM4~~	~~Differential to common mode input return loss~~	~~83E.3.3.2~~	~~Equation (83E–6)~~	~~M~~	~~Yes [ ]~~
~~RM5~~	~~Stressed input test~~	~~83E.3.4.2~~	~~Satisfy requirements in Table 83E–8~~	~~M~~	~~Yes [ ]~~