Channel Characteristics (83D.4)

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Channel in D1.1

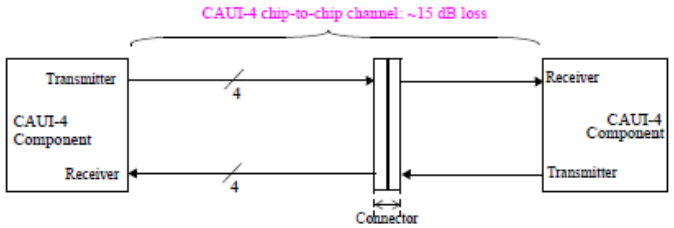

Figure 83D–2—Chip-to-chip insertion loss budget at 12.89 GHz

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower due to the channel ILD, return loss, and crosstalk.

EDITORS NOTE: Insertion_loss equation is TBC

$$Insertion\_loss(f) \le \begin{cases} 1.614(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.614(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad \text{(83D–1)}$$

where

f is the frequency in GHz

$Insertion\_loss(f)$ is the informative CAUI-4 chip-to-chip insertion loss

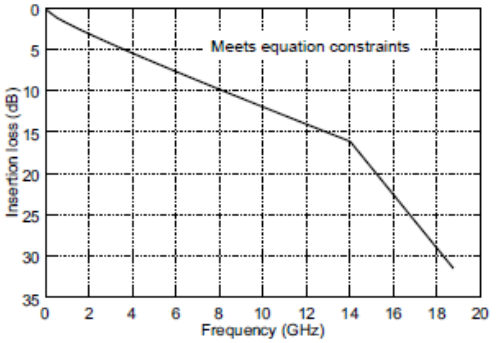

Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss

83D.4 CAUI-4 chip-to-chip channel characteristics

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 83D–5 shall be greater than or equal to TBD. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization settings.

Table 83D–5—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_d z_p C_b	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_b	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 TBD TBD TBD	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 TBD TBD TBD	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 TBD TBD TBD	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	TBD	UI
Dual-Dirac jitter, peak	A_{DD}	TBD	UI
One-sided noise spectral density	η_0	TBD	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—

Channel in D1.1 Continued

$$RLd(f) \geq \begin{cases} 15 & 0.05 \leq f \leq 6.4 \\ 15 - 15\log_{10}\left(\frac{4f}{25.78}\right) & 6.4 < f \leq 19 \end{cases} \text{ (dB)} \qquad \text{(83D–8)}$$

where

f is the frequency in GHz
RLd is the CAUI-4 chip-to-chip differential input return loss

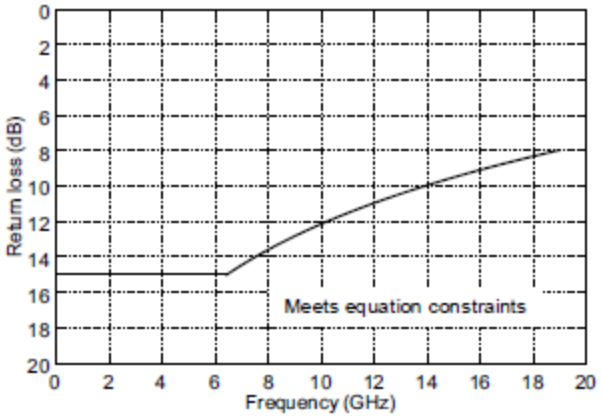

Figure 83D–13—Channel return loss

Channel Update

CAUI-4 chip-to-chip channel

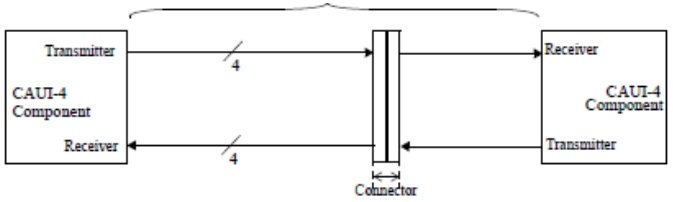

Figure 83D–2—Chip-to-chip insertion loss budget at 12.89 GHz

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower due to the channel ILD, return loss, and crosstalk.

$$Insertion\_loss(f) \le \begin{cases} 1.614(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.614(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad \text{(83D–1)}$$

where

f is the frequency in GHz
$Insertion\_loss(f)$ is the informative CAUI-4 chip-to-chip insertion loss

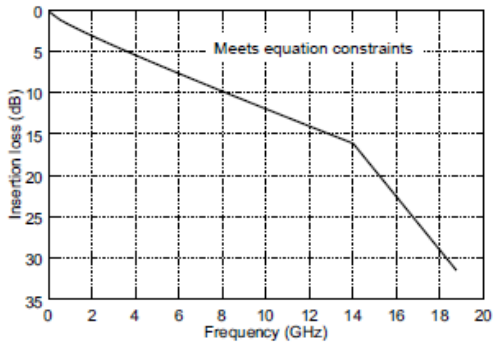

Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss

Channel Update

83D.4 CAUI-4 chip-to-chip channel characteristics

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 83D–5 shall be greater than or equal to 3dB using any combination of discrete transmitter equalizer and continuous time filter settings shown in Table 83D-5. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization settings.

Table 83D–5—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Transmitter package model Single-ended device capacitance Transmission line length Single-ended board capacitance	C_d t z_p t C_b t	2.5×10^{-4} 12 1.8×10^{-4}	nF mm nF
Receiver package model Single-ended device capacitance Transmission line length Single-ended board capacitance	C_d r z_p r C_b r	0 0 0	nF mm nF
Single-ended reference resistance	R_b	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient	$c(-1)$	0 -0.032 -0.058	— — —
Transmitter equalizer, post-cursor coefficient	$c(1)$	0 -0.041 -0.074 -0.1	— — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	-15 -1 1	dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	A_v A_f A_n	0.4 0.4 0.6	V V V
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—