45. Management Data Input/Output (MDIO) Interface

45.2.3 PCS registers

Change the row for 3.220 through 3.399 of Table 45-99 (as modified by IEEE Std P802.3bj-201x) and insert three new rows immediately below the changed row as follows:

Table 45–99—PCS registers

Register address	Register name	Subclause
3.220 through 3.~~399~~299	Reserved	
3.300	Multi-lane BIP mismatch status	45.2.3.45a
3.301 through 3.305	Multi-lane BIP mismatch counter, 1-lane through 5-lane	45.2.3.45b
3.306 through 3.399	Reserved	

Insert 45.2.3.45a, 5.2.3.45b, and 45.2.3.45c after 45.2.3.45 as follows:

45.2.3.45a Multi-lane BIP mismatch status register (Register 3.300)

The assignment of bits in the multi-lane BIP mismatch status register is shown in Table 45–139a. If the multi-lane PCS described in Clause 82 implements the optional multi-lane BIP mismatch handling (see 82.2.14.3), this register reflects the values of the hi_bip_mismatch and group_bip_mismatch_count variables.

Table 45–139a—Multi-lane BIP mismatch status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.300.15:6	Reserved	Value always zero, writes ignored	RO
3.300.5	High BIP mismatch	1 = more than two markers with mismatched BIP in the last alignment marker group 0 = up to two markers with mismatched BIP in the last alignment marker group	RO/LH
3.300.4:0	Group BIP mismatch count	The number of markers with mismatched BIP in the last alignment marker group	RO

[a]RO = Read only, LH = Latching high

45.2.3.45b Multi-lane BIP mismatch counter, 1-lane register (Register 3.301)

The assignment of bits in the multi-lane BIP mismatch counter, 1-lane register is shown in Table 45–139b. If the multi-lane PCS described in Clause 82 implements the optional multi-lane BIP mismatch handling (see 82.2.14.3), this register reflects the value of the group_bip_mismatch_counter<1> variable. When this register is read or upon PCS reset, the group_bip_mismatch_counter<1> variable shall be set to zero.

Table 45–139b—Multi-lane BIP mismatch counter, 1-lane register bit definitions

Bit(s)	Name	Description	R/W[a]
3.301.15:0	Multi-lane mismatch counter, 1-lane	Cumulative number of 1-lane BIP mismatches in an alignment marker group	RO/NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.45c Multi-lane BIP mismatch counter, 2-lane through 5-lane registers (Registers 1.302 through 1.305)

The behavior of the multi-lane BIP mismatch counter, 2-lane through 5-lane registers is identical to that described for the 1-lane register in 45.2.3.45b. If the optional multi-lane BIP mismatch handling (see 82.2.14.3) is implemented, then multi-lane mismatches of each number of lanes are counted and shown in register bits 15:0 in the corresponding register. Mismatches of 2, 3, and 4 lanes are shown in registers 3.302, 3.303 and 3.304, respectively. Mismatches of 5 or more lanes are shown in register 3.305.

82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.2 Physical Coding Sublayer (PCS)

Change the text of 82.2.6 as follows:

82.2.6 Block distribution

Once the data is encoded and scrambled, it is distributed to multiple PCS lanes, 66-bit blocks at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. This allows the PCS to support multiple physical lanes in the PMD and XLAUI or CAUI-n interfaces (see Annex 83A, ~~and~~ Annex 83B, Annex 83D, and Annex 83E). The 40GBASE-R PCS distributes the 66-bit blocks to 4 PCS lanes, and the 100GBASE-R PCS distributes the blocks to 20 PCS lanes. The distribution process is shown in Figure 82–6.

Change the title and text of 82.2.14 and insert additional subclause headings as follows:

82.2.14 Alignment marker ~~removal~~ handling

82.2.14.1 Lane multiplexing and marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks. ~~and the~~ The alignment markers ~~are~~ form groups of adjacent blocks within this stream. These alignment marker groups are deleted from the data stream. The difference in rate from the deleted alignment markers is compensated for by inserting idle control characters by a function in the Receive process. Note that ~~an~~ alignment marker groups appear at regular intervals and at known locations and are ~~is~~ always deleted ~~when a given PCS Lane is in am_lock=true~~ even if individual alignment markers do ~~it does~~ not match the expected alignment marker value (due to ~~a~~ bit errors for example). Repeated alignment marker errors will result in am_lock being set to false for a given PCS Lane, but until that happens it is sufficient to delete the block in the alignment marker position.

82.2.14.2 BIP check

~~As part of the alignment marker removal process~~When a group of alignment markers is removed, the BIP_3 field value of each marker is compared to the calculated BIP value for ~~each~~ the corresponding PCS lane. The result of this comparison is reflected in the am_bip_mismatch<*x*> variables.

The cumulative number of BIP mismatches in each lane is stored in the bip_error_counter<*x*> counters. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.200 through 3.219) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1081344.

82.2.14.3 Multi-lane BIP mismatch handling

Multi-lane BIP mismatch handling is required for a 100GBASE-R PCS when the optional CAUI-4 PMA service interface physical instantiation is implemented. It is optional for a 100GBASE-R PCS without CAUI-4, and for a 40GBASE-R PCS.

If implemented, multi-lane BIP mismatch handling shall be as described in this subclause (82.2.14.3).

The purpose of multi-lane BIP mismatch handling is to provide an assessment of the rates of correlated error events in a multi-lane link. These rates can be used to estimate the mean time to false packet acceptance (MTTFPA).

When a group of alignment markers is removed, the number of markers with mismatched BIP in an alignment marker group is calculated and stored in the group_bip_mismatch_count variable. If group_bip_mismatch_count is greater than two, the variable hi_bip_mismatch is set to 1, otherwise it is set to 0. The variable group_bip_mismatch_count retains its value between alignment marker groups and the variable hi_bip_mismatch latches high until reset by being read.

If group_bip_mismatch_count equals *i*, where *i* is between 1 and 5, the counter group_bip_mismatch_counter<*i*> is incremented by 1. If group_bip_mismatch_count is larger than 5, group_bip_mismatch_counter<5> is incremented by 1. Any such increment is performed only once per alignment marker group, so that the group_bip_mismatch_counter<*i*> counters store the cumulative numbers of multi-lane BIP mismatch events.

If both multi-lane BIP mismatch handling and Clause 45 MDIO are implemented, then the multi-lane BIP mismatch counters (registers 3.301 through 3.305) reflect the values of each of the group_bip_mismatch_counter<*i*> counters. If multi-lane BIP mismatch handling is implemented but a Clause 45 MDIO is not implemented, then a vendor-specific equivalent implementation of the counters shall be provided instead.

82.2.18 Detailed functions and state diagrams

82.2.18.2 State variables

82.2.18.2.2 Variables

Change the definition for PCS_status in 82.2.18.2.2 as follows:

PCS_status
: A Boolean variable, ~~that is true~~ If multi-lane BIP mismatch handling is implemented, asserted when align_status is true, hi_bip_mismatch is false and hi_ber is false. If multi-lane BIP mismatch handling not is implemented, asserted when align_status is true and hi_ber is false.

Insert a new variable definition for am_bip_mismatch<x> in the appropriate place in 82.2.18.2.2 (as modified by IEEE Std 802.3bj-201x) as follows:

am_bip_mismatch<*x*>
: A Boolean variable that is asserted during BIP check if the lane *x* alignment marker BIP_3 field value is not equal to the calculated BIP value for PCS lane *x*, where *x* = 0:3 for 40GBASE-R and *x* = 0:19 for 100GBASE-R. It is de-asserted if the BIP_3 field value is equal to the calculated BIP value, or if the processed block is not an alignment marker.

Insert the following new text and variables at the end of the existing subclause 82.2.18.2.2 (as modified by IEEE Std 802.3bj-201x):

The following variables are used only for the optional multi-lane BIP mismatch handling capability.

group_bip_mismatch_count

This variable holds the number of markers with mismatched BIP in the most recent alignment marker group.

hi_bip_mismatch

This Boolean variable is assigned when an alignment marker group is checked. Asserted if group_bip_mismatch_count is larger than two, and de-asserted otherwise. This variable retains its value between alignment marker groups.

82.2.18.2.4 Counters

Insert a new counter definition for bip_error_counter<x> in the appropriate place in 82.2.18.2.4 (as modified by IEEE Std 802.3bj-201x) as follows:

bip_error_counter<*x*>

16-bit counters which hold the accumulated number of am_bip_mismatch<*x*> occurrences, where *x* = 0:3 for 40GBASE-R and *x* = 0:19 for 100GBASE-R. If a Clause 45 MDIO is implemented, these counters are reflected in registers 3.200 through 3.219. They are cleared on reading and saturated on overflow.

Insert the following new text and counters at the end of the existing subclause 82.2.18.2.4 (as modified by IEEE Std 802.3bj-201x):

The following counters are used only for the optional multi-lane BIP mismatch handling capability.

group_bip_mismatch_counter<*x*>

These 16-bit counters count the number of group BIP errors of various lengths. group_bip_mismatch_counter<*i*> is incremented by one when an alignment marker group with exactly *i* mismatched BIP fields is encountered, where *x* = 1:4 for 40GBASE-R and *x* = 1:5 for 100GBASE-R. If a Clause 45 MDIO is implemented, these counters are reflected in registers 3.301 through 3.305. They are cleared on reading and saturated on overflow.