CAUI-4 Sinusoidal Jitter Specification: Additional requirements?

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Current CAUI-4 Sinusoidal Jitter spec.

Table 88–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	$5 \times 10^5 / f$
10 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

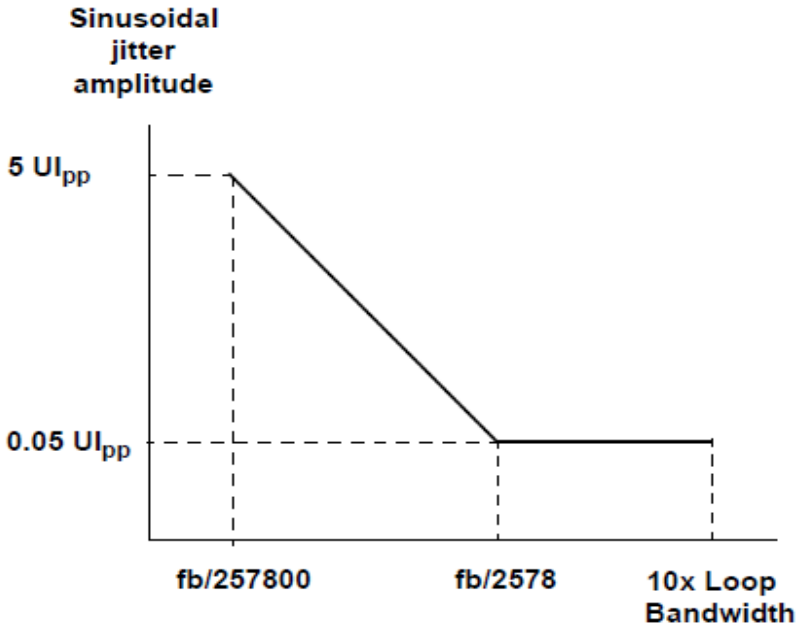


Figure 13-12. Host input and Module input Sinusoidal Jitter

CAUI-4 Sinusoidal Jitter (SJ) Handling

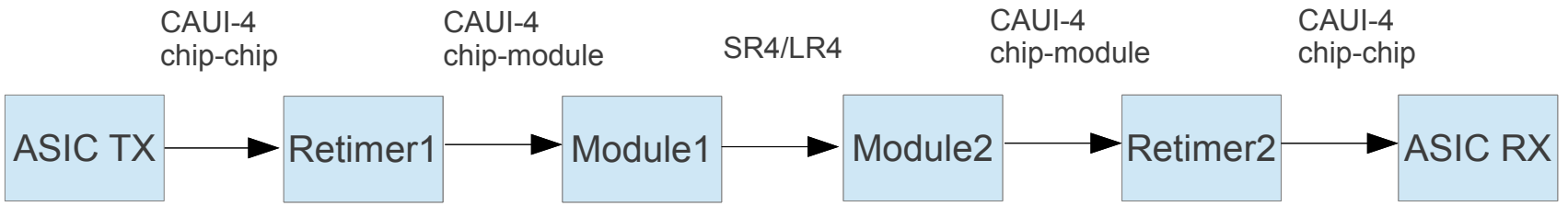
1. For a complete spec., an RX SJ tolerance spec. should be paired with a TX SJ generation spec.

Currently most specifications including CAUI-4 do not directly specify TX SJ. It is therefore possible for a compliant TX to exceed the RX SJ tolerance spec.

2. For applications with multiple interconnect segments, devices need to be specified to be either SJ transparent or SJ terminating

CAUI-4 chip-chip and chip-module specifications, do not specify SJ handling

End-to-End Topology

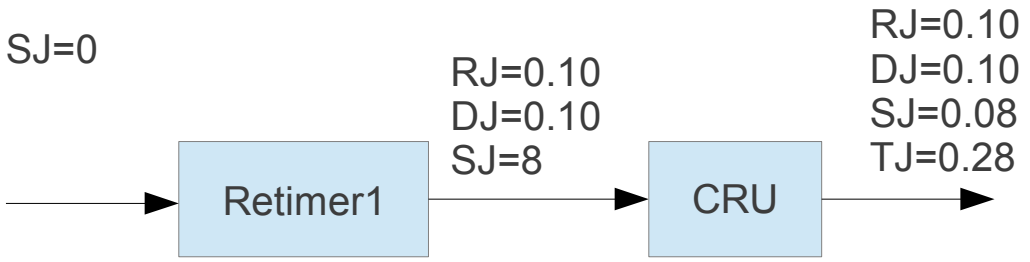


With SJ transparent devices, SJ accumulates at every device between ASIC TX and ASIC RX.

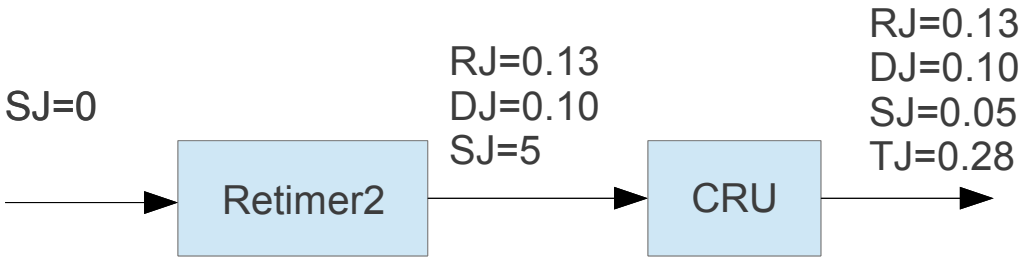
Sinusoidal Jitter Accumulation

Assume SJ Frequency is Fb/257800 =100KHz

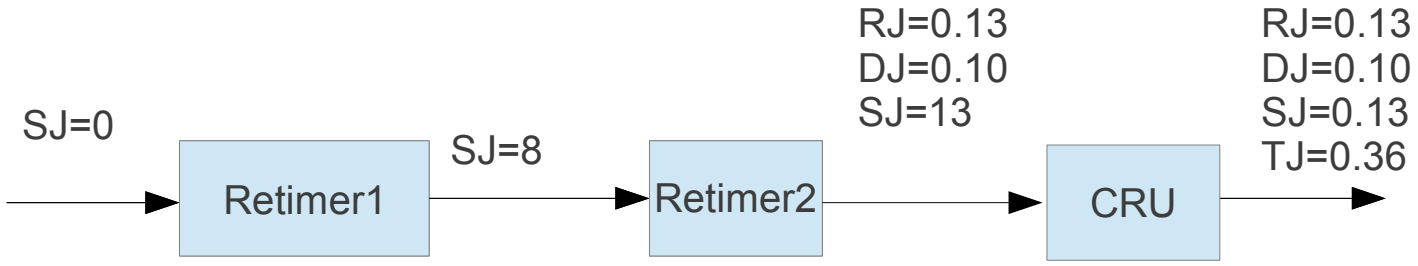
All jitter in UIpp



Compliant TX exceeds RX SJ Tolerance limit



Compliant



Compliant devices cascaded result in non-compliant output

Impact on system power filter design

Power supply ripple can be a major contributor to SJ.

Assuming full SJ budget allocated to power supply ripple:

At Fb/25780=1 MHz ripple frequency, current SJ limit is 0.5UIpp = ~20 ps

For 1V supply, ripple of +/-0.5% = 10mVpp

If TX and RX equally contribute to SJ, ~10 ps each

Power noise to jitter conversion should then be better than 10/10 = ~1ps/mV

Power filters take up real estate

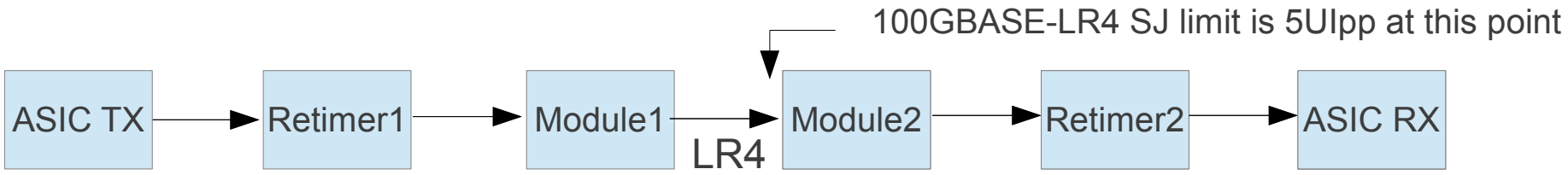
With lower voltages and higher current, IR drop increasingly challenging

CAUI-4 SJ spec. can impact power filter design cost/complexity

Possible changes / solutions

1a. If devices can be SJ transparent

i) Limit additive TX SJ to 1.5UIpp (@ fb/257800) for all TX in topology
(accumulation limited by 100GBASE-LR4 SJ spec.)



(All devices must have better than 300fs/mV, power noise to jitter conversion)

ii) To simplify, require all CAUI-4 RX in the topology tolerate 7.5UIpp (@ fb/257800)

OR

1b. Specify that devices will be SJ terminating

Limit TX SJ generation to 5UIpp (@ fb/257800)

2. To avoid ambiguity, extend SJ mask 5UIpp requirement down to DC

Possible changes / solutions (continued)

3. Align 100GBASE-SR4 SJ spec. with CAUI-4 requirements

Table 95–7—100GBASE-SR4 receive characteristics

Conditions of receiver jitter tolerance test:		
Jitter frequency and peak-to-peak amplitude	(190, 5)	kHz, UI
Jitter frequency and peak-to-peak amplitude	(940, 1)	kHz, UI