CAUI-4 Ad hoc

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Agenda

- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-to-module discussion
- Chip-to-chip discussion

Mechanism for host to provide recommended CTLE value

83E.3.1.6 Host output jitter and eye height

Host output eye width is greater than 0.46 UI. Host output eye height is greater than 95 mV. Figure 83E–9 depicts an example host output jitter and eye height test configuration. Host output jitter and eye height are measured at TP1a using compliance boards defined in 83E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.1.6.1. The recommended CTLE peaking value is provided to the module via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.88c). Eye contour measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are defined in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and transition time of 9.5 ps.

Module input compliance test

~~Frequency dependent attenuation is added such that from the output of the limiter to TP1a is 10.25 dB loss at 12.89 GHz. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and variable gain are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver.~~

Two levels of frequency dependent attenuation are used for the module stressed input test: High Loss, and Low Loss. For the High Loss case, frequency dependent attenuation is added such that from the output of the limiter to TP1a is 10.25 dB loss at 12.89 GHz. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and variable gain are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. For the Low Loss case, discrete frequency dependent attenuation is removed such that from the output of the limiter to TP1a is comprised of the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and variable gain are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. In both the Low Loss and High Loss cases, the module under test is provided with the reference CTLE setting used to meet eye width and eye height requirements via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.88c). The module under test is evaluated with three *Recommended_CTLE_value* values for both the High Loss test and Low Loss Test. These are: a) the CTLE setting used to meet eye width and eye height requirements, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2.

Host output compliance test

83E.4.2 Host / Module eye contour measurement method

Eye diagrams in CAUI-4 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is Pattern 4 (PRBS9) as defined in Table 86-11. The follow procedure should be used to obtain eye height and eye width parameters:

1) Capture Pattern 4 using a clock recovery unit with 3 dB tracking bandwidth of 10 MHz and maximum peaking of 0.1 dB and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.

2) ~~Apply respective reference receiver CTLE to captured signal. Any single CTLE setting which meets both eye width and eye height requirements is acceptable.~~

3) Apply respective reference receiver CTLE to captured signal. For modules, any single CTLE setting as described in 83E.3.2.1.1 which meets both eye width and eye height requirements is acceptable. For host compliance, the CTLE peaking in the reference receiver shall be set to one of three values. These are: a) the recommended CTLE peaking value provided by the host, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2. Any of the three CTLE settings that meets both eye width and eye height defined in Table 83E–1 is acceptable.

4) Use the differential equalized signal from step 2 to construct the CDF of the jitter zero crossing for both the left edge (CDFL) and right edge (CDFR), as a distance from the center of the eye. Calculate the eye width (EW6) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits. For a pattern with 50% transition density the maximum value for the CDFL and CDFR will be 0.5. The CDFL and CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.

MDIO

45.2.1 PMA/PMD registers

Change the identified reserved row in Table 45-3 (as modified by IEEE Std P802.3bj-201x) and insert a new row for register 1.169 immediately below the changed row as follows:

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.167 through 1.~~169~~168	Reserved	
1.169	CAUI-4 chip-to-module recommended CTLE	45.2.1.88c

Insert 45.2.1.88c after 45.2.1.88b (as inserted by IEEE Std P802.3bj-201x) as follows:

45.2.1.88c CAUI-4 chip-to-module recommended CTLE register (Register 1.169)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–67c. The value stored in this register corresponds to the CTLE peaking value (see 83E.3.1.6.1) recommended by the host (and used in the evaluation of host output compliance). The module may optionally use this information to adjust its CTLE setting.

Table 45–67c—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.169.15:6	Reserved	Value always 0, writes ignored	RO
1.169.5:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	RO
1.169.0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read only

Reference CTLE

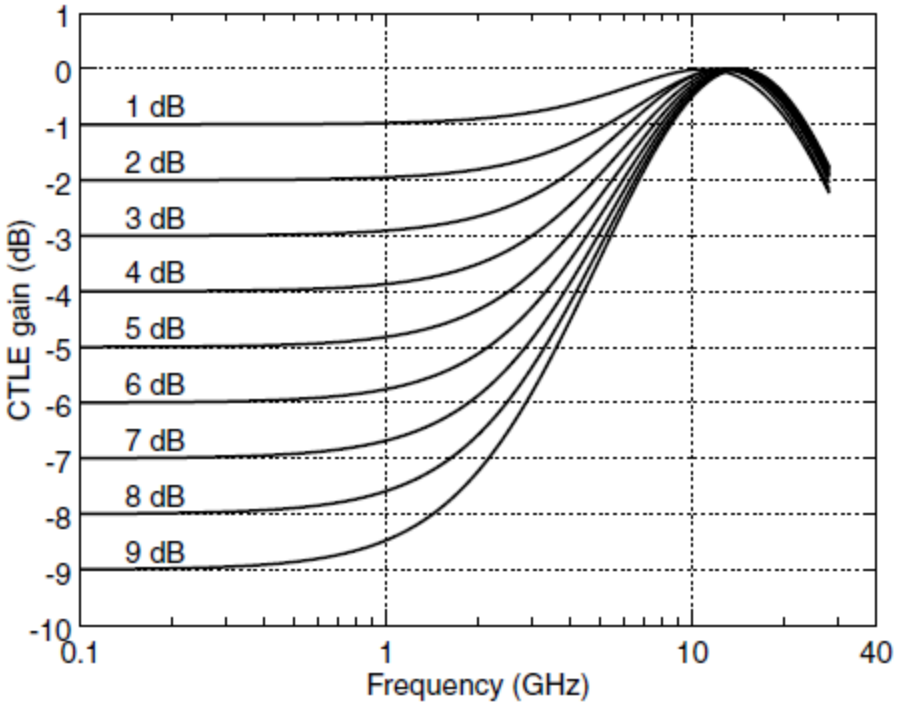

Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic