CAUI-4 Ad hoc

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20dB Informative channel update

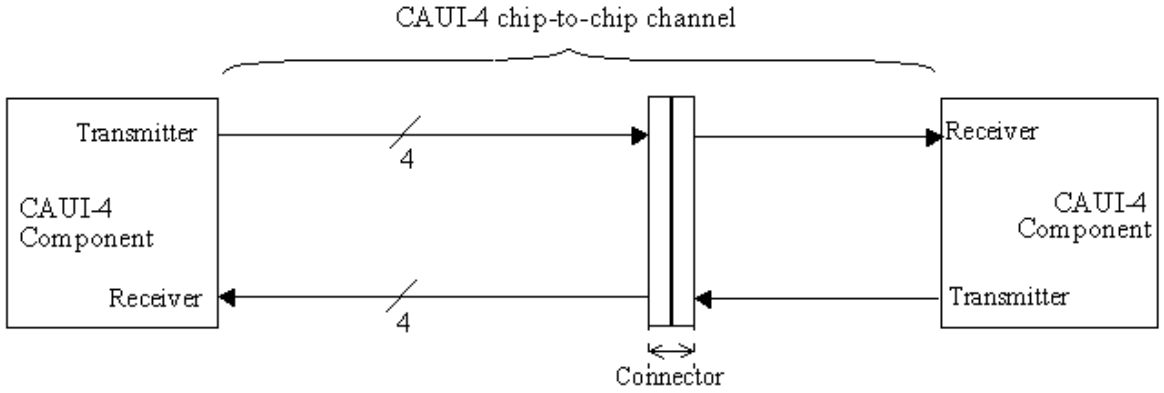

Figure 83D–2—Typical CAUI-4 chip-to-chip application§

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower due to the channel ILD, return loss, and crosstalk.¶

$$Insertion\_loss(f) \le \begin{cases} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 14 \le f < 25.78 \end{cases} \text{ (dB)} \quad \text{(83D–1)}$$

where¶

f	is the frequency in GHz¶
$Insertion\_loss(f)$	is the informative CAUI-4 chip-to-chip insertion loss¶

Updated Insertion Loss Figure

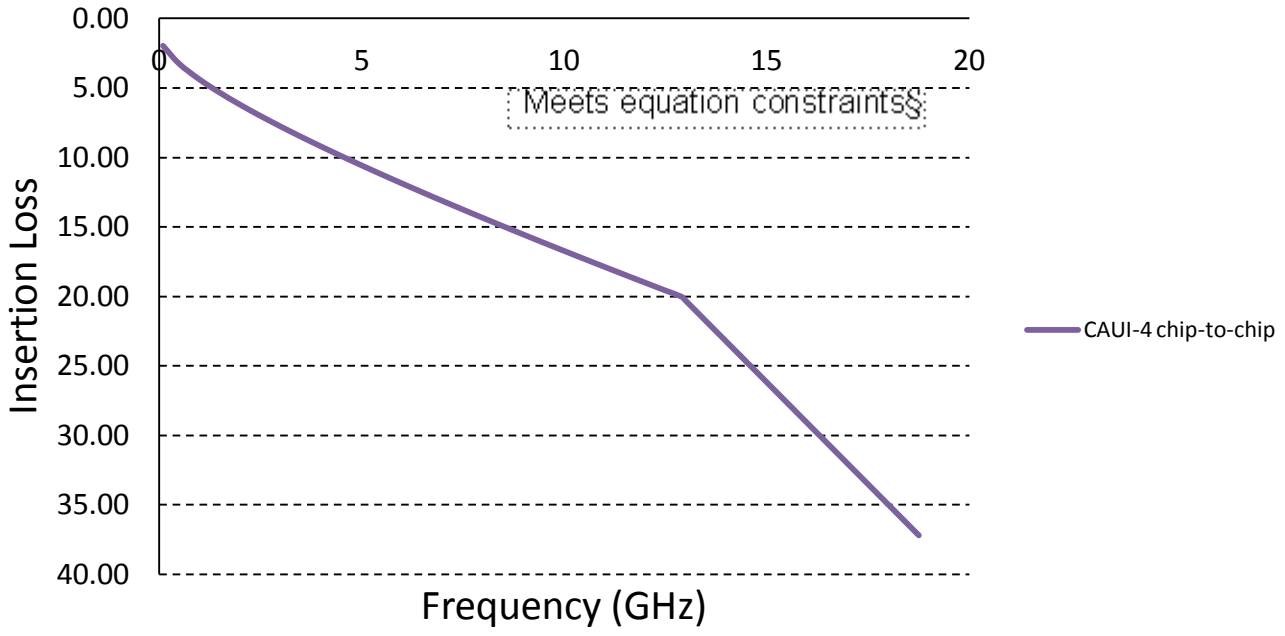

Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss§

83D.2 CAUI-4 chip-to-chip compliance point definition¶

Transmitter

- Current approach: Eye mask and defined pre/post transmit equalization

or

- With addition of DFE, implementation can be more similar to CL93
  - Output waveform
  - Output jitter definition

Transmitter

- CAUI-4 does not use PMD control function (93.7.12)
  - Define to use management interface to control transmitter

83D.3 CAUI-4 chip-to-chip electrical characteristics¶

83D.3.1 CAUI-4 transmitter characteristics¶

A CAUI-4 chip-to-chip transmitter shall meet the specifications defined in Table 83D–1 when measured at TP0a. While the CAUI-4 chip-to-chip transmitter interface is similar to Clause 93, it differs by not assuming transmitter training. The transmit output wave form is not manipulated via PMD control function defined in 93.7.12. Also the CAUI-4 transmitter does not assume a back-channel communications path.¶

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.¶

Transmitter

Table 83D–1—TCAUI-4 transmitter characteristics at TP1a§

Parameter§	Subclause Reference§	Value§	Units§
Signaling rate per lane (range)§	93.8.1.2§	25.78125 ±100 ppm§	GBd§
Differential peak-to-peak output voltage (max)¶ Transmitter disabled¶ Transmitter enabled§	93.8.1.3§	¶ 30¶ 1200§	mV§
Common-mode voltage (max)§	93.8.1.3§	1.9§	V§
Common-mode voltage (min)§	93.8.1.3§	0§	V§
Common-mode AC output voltage (max, RMS)§	93.8.1.3§	12§	mV§
Differential output return loss (min)§	93.8.1.4§	Equation (93-3)§	dB§
Common-mode output return loss (min)§	93.8.1.4§	Equation (93-4)§	dB§
Output waveform[a]¶ Steady state voltage v_f (max)¶ Steady state voltage v_f (min)¶ Linear fit pulse peak (min)¶ Normalized coefficient step size (min)¶ Normalized coefficient step size (max)¶ Pre-cursor full scale range (min)¶ Post-cursor full scale range (min)§	93.8.1.5§	¶ 0.6¶ 0.4¶ 0.71 x v_{f1} 0.0083¶ 0.05¶ 1.54¶ 4§	¶ V¶ V¶ V¶ -¶ -¶ -¶ -§
Signal-to-noise-and-distortion ratio (min)§	93.8.1.6§	27§	§
Output Jitter (max)¶ Even-odd jitter¶ Effective bounded uncorrelated jitter, peak-to-peak¶ Effective random jitter, RMS§	93.8.1.7§	¶ 0.035¶ 0.1¶ ¶ 0.01§	¶ UI¶ UI¶ ¶ UI§

[a]State of the transmit equalizer is controlled by management interface.§

-Leave unchanged
- Change step size and range, or
-Keep D2.0 fixed settings

Interference Tolerance

Table 93–6—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Test 3 values		Test 4 values		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
RS-FEC symbol error ratio[a]	—	10^{-11}	—	10^{-11}	—	10^{-4}	—	10^{-4}	—
Insertion loss at 12.89 GHz[b]	—	16	30	—	—	30	35	—	dB
Coefficients of fitted insertion loss[c]									
a_0	–0.9	0.9	–0.9	0.9	–0.9	0.9	–0.9	0.9	dB
a_1	0	3.3	0	3.3	0	3.3	0	3.3	dB/GHz$^{1/2}$
a_2	0	—	0	—	0	—	0	—	dB/GHz
a_4	0	0.022	0	0.03	0	0.03	0	0.043	dB/GHz^2
RSS_DFE4	0.05	—	0.05	—	0.05	—	0.05	—	—
COM, including effects of broadband noise	—	3	—	3	—	3	—	3	dB

[a]The FEC symbol error ratio is measured in step 11 of the receiver interference tolerance method defined in 93C.2.
[b]Measured between TPt and TP5 (see Figure 93C–4).
[c]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with f_{min} = 0.05 GHz, f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz.

CAUI-4 Chip-Chip	
Min	Max
-	10^{-15}
-	20
-1	2
0	14.914
0	41.228
0	19.728
0.05	-
-	2

COM

Signaling rate§	f_b§	25.78125§	GBd§
Maximum start frequency§	f_{min}§	0.05§	GHz§
Maximum frequency step§	Δf§	0.01§	GHz§
Transmitter package model¶ Single-ended device capacitance¶ Transmission line length¶ Single-ended board capacitance§	¶ $C_{d,t}$¶ $z_{p,t}$¶ $C_{b,t}$§	¶ 2.5 × 10^{-4}¶ 12¶ 1.8 × 10^{-4}§	¶ nF¶ mm¶ nF§
Receiver package model¶ Single-ended device capacitance¶ Transmission line length¶ Single-ended board capacitance§	¶ $C_{d,r}$¶ $z_{p,r}$¶ $C_{b,r}$§	¶ 2.5 × 10^{-4}¶ 12¶ 1.8 × 10^{-4}§	¶ nF¶ mm¶ nF§
Single-ended reference resistance§	$R_{s,t}$§	50§	ohms§
Single-ended termination resistance§	$R_{d,t}$§	55§	ohms§
Receiver 3dB bandwidth§	$f_{r,3}$§	0.75 × f_b§	GHz§
Transmitter equalizer, pre-cursor coefficient¶ §	$c(-1)$, $c(0)$, $c(1)$§	Table 83D–8¶ §	¶ —¶ —¶ —§
Transmitter equalizer, post-cursor coefficient¶ §	$c(-1)$, $c(0)$, $c(1)$§	Table 83D–9¶ §	¶ —¶ —¶ —§
Continuous time filter, DC gain¶ §	$CTLE_{dc}$§	Table 83D–6§	¶ dB¶ dB¶ dB§
Transmitter differential peak output voltage¶ Victim¶ Far-end aggressor¶ Near-end aggressor§	¶ A_v¶ A_{fa}¶ A_{na}§	¶ 0.4¶ 0.4¶ 0.6§	¶ V¶ V¶ V§
Number of signal levels§	L§	2§	—§
Level separation mismatch ratio§	R_{LM}§	1§	§§
Transmitter signal to noise ratio§	SNR_{TX}§	27§	dB§
Number of samples per unit interval§	M§	32§	—§
Decision feedback equalizer (DFE) length§	N_b§	5§	UI§
Normalized DFE coefficient magnitude limit§	δ_{max}§	0.3§	—§
Random jitter, RMS§	σ_{RJ}§	0.01§	UI§

Add Rx Package Model

Keep Tx EQ and CTLE updates(?)

5 tap with max 0.3 limit

Minutes

- Attendees
  - Pete Anslow, Ciena
  - Charles Moore, Avago Technologies
  - Adam Healey, LSI
  - Richard Mellitz, Intel
  - Adee Ran, Intel
  - Matt Brown, Applied Micro
  - Vinu Arumugham, Cisco
  - John Petrilla, Avago
  - Ali Ghiasi, Independent
  - Jonathan King, Finisar
  - Dan Dove, Dove Networking
  - Mike Li, Altera
- Patent policy
- Chip-to-module discussion
  - latchman_01_120913 updates
    - Request comments to be sent to Ryan Latchman prior to the next meeting
    - Comment will be submitted by Ryan Latchman to implement changes outlined in presentation after next meeting
  - Arumugham_00_121013
    - Concern with SJ accumulation and lack of Tx SJ specification
    - Request for simulations which demonstrate the source of SJ discussed in presentation
    - Request for off-line work to build supporters to implement a specific change
- Chip-to-chip discussion
  - Proposed Change to PCS for multi-lane error detection (Adee Ran)
    - Mark expressed concern with bringing down the link
    - Request another specific logic call be organized with interested parties
  - latchman_02_120913
    - Request for additional implementation input on 83D
    - Ryan Latchman to provide implementation text for changes outlined
    - Mike Li, to put together a second low loss receiver interference test (~10dB)
    - Richard Melitz to consider changes to RSS_DFE4
- Next meeting: Dec 16 2013 at 9am PT