Thoughts on the 100GbE Proposed PCS changes

802.3bm

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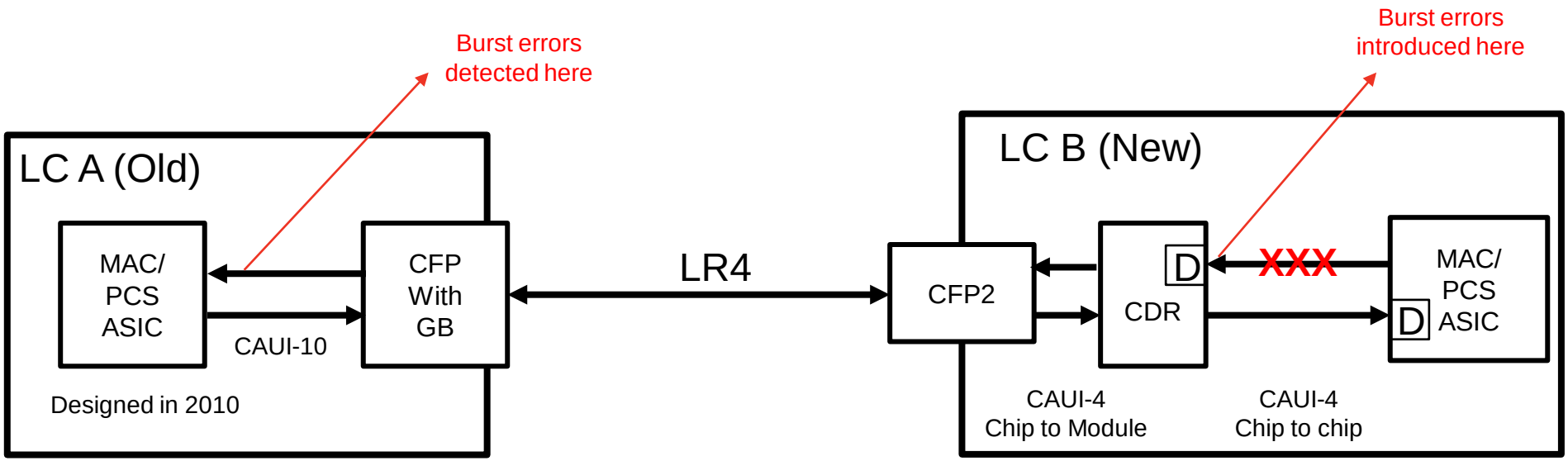
Introduction to the problem

- **Proposal is to signal a problem when 3 or more errors are detected in an Alignment Marker period**
- **As proposed, the PCS status signal, which indicates an operational PCS, would go to non-operational mode for one alignment marker period after receiving a single burst error. This would take down your interface for a single burst error!**
  - Can cause a routing flap
  - The cure is worse than the disease?
  - What does a customer do with the information anyhow? Replace the LC?? But is the LC compliant or not??
- **Even if you don't have a CAUI-4 interface, you would need to support this in case the far end has a CAUI-4 interface! It will not be optional.**
  - This makes the proposal incompatible with current deployed interfaces

Full Span Problem

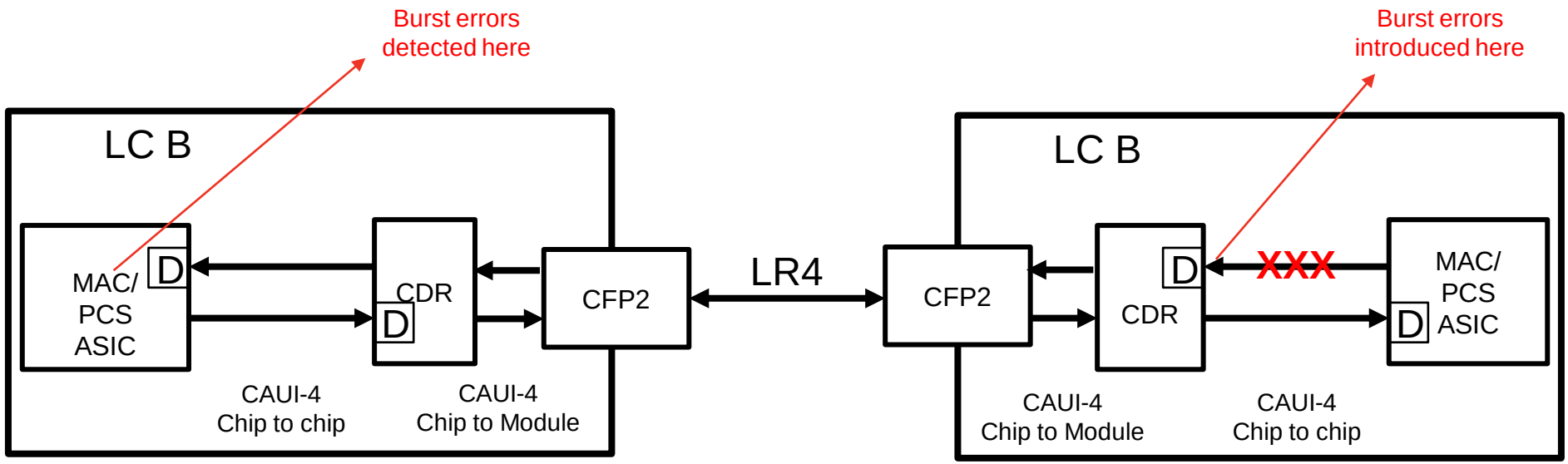
- **Burst errors on the far end CAUI-4 chip to chip must be detected by the near end, so all PCS entities would need to change!**
  - Including equipment already installed in the field !
- **Or you add a requirement that retimers monitor the BIP!**



D DFE based receiver.

Full Span Problem

- **If both sides have a CAUI-4 interface then how would you know which linecard to replace?**
  - Assuming the desired action is to replace a card? That is otherwise compliant but happens to get a burst errors?
  - You cannot put LCs into loopback and reproduce this problem in a reasonable timeframe
- **Or you add a requirement that retimers monitor the BIP!**
  - This would part of the PCS into the PMA



D DFE based receiver.

How to Move Forward?

- **Reduce the budget back to 15dB?**
  - Does it solve the problem, don't believe so because requires extremely clean package (not realistic for large ASICs)
- **Require a retimer or GB to terminate the BIP???**
  - But then what to do with the information?
  - loose end-to-end visibility ?
- **Add in precoding? Or other mechanism?**

- **Limit DFE taps?**
  - Proposal is tap weight < 0.3, proposal is to enforce that setting
- **Decrease the BER?**
  - Better than 10^-18 (3.2 errors per year)
- **Switch to block interleaving for chip to chip interfaces**
- **Ignore the problem since most links will operate with a better BER and MTTFPA won't be an issue?**
- **Change the MTTFPA requirement ?**
  - from AOU to something a little less but still large enough?

Thanks!