CAUI-4 C2C lower latency FEC option

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Current options for CAUI-4 C2C

	CTLE-only	CTLE + 5 Tap DFE	KR4
AN	No	No	Yes
PMD Training	No	No	Yes
RS(514,528) FEC	No	No	Yes
Min latency PCS scrambler to descrambler[1] (ns)	20.8	20.8	~100 (correction on) ~55 (bypass on)
Max Loss Budget (dB)[2]	15	20	35
Area	X	1.6X	3.4X
Power	X	1.6X	3.1X
MTTFPA	Acceptable	???	Acceptable

[1] Excludes common PMA/Channel latencies which are assumed to be the “same”
[2] Under ideal interference conditions.

CTLE + 5 Tap DFE

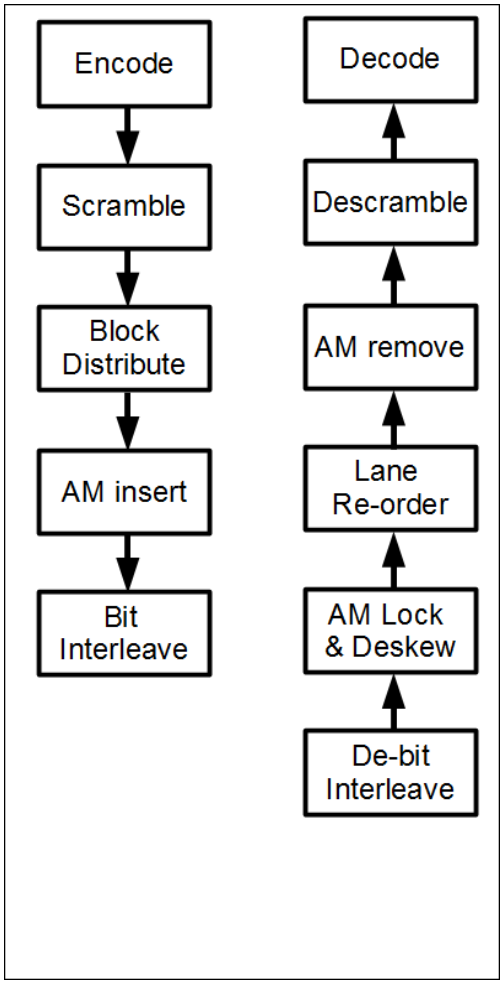
- **Mellitz presentation – COM Simulation used to control the amount of feedback DFE is allowed to supply**
  - Calculating this based on current operating conditions is not a trivial thing to do live insitu. Receiver tuning methods must also have a control knob.
  - How do you ensure that a PHY adheres to the values applied in the COM simulation for the channel. (software applies settings into the system that were used in SI designers COM simulation)
- **Ran presentation – Add another layer of monitoring based on BIP fields to track if probability of MTTFPA is too low.**
  - Monitors errors coming through flap link if too many BIP errors occur
  - False packet can be received and processed and re-transmitted before monitor fires to take link down.

Alternative – Use extremely low latency FEC

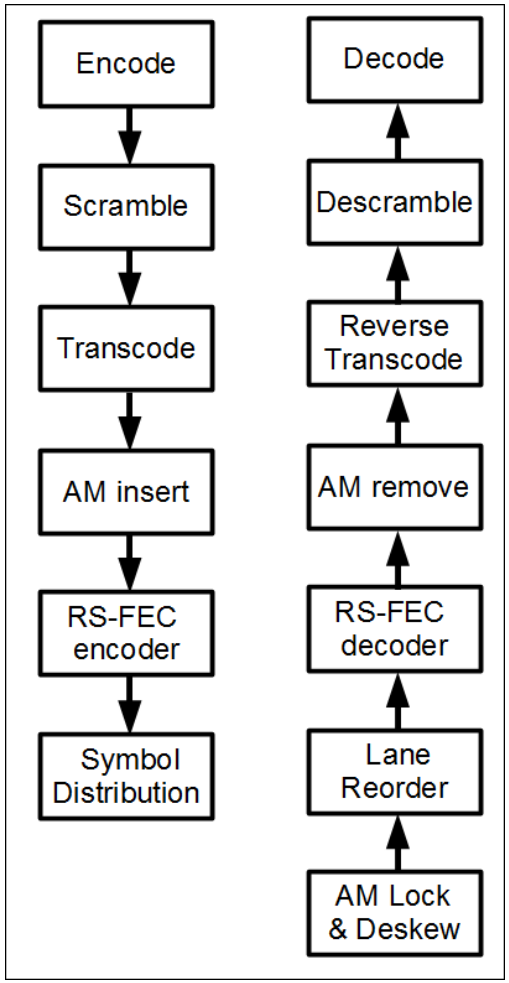
- **Define RS-FEC with codeword based on 5 TC blocks**
  - AMs map into a single FEC codeword, same AM/frame logic as KR4
  - Essentially cutting the KR4 RS-FEC in ¼
- **5 TC blocks provides 35b of parity**
- **Use a symbol size of 8b, providing T=2 (2 corrections)**
  - RS(161,165,m=8,t=2)
- **Latency for codeword reception is 1320b * 39ps / 4 = 12.8ns**
  - Same as bit interleaving
- **Area**
  - ~10% increase compared to bit interleaving logic

Block diagrams for co-located design

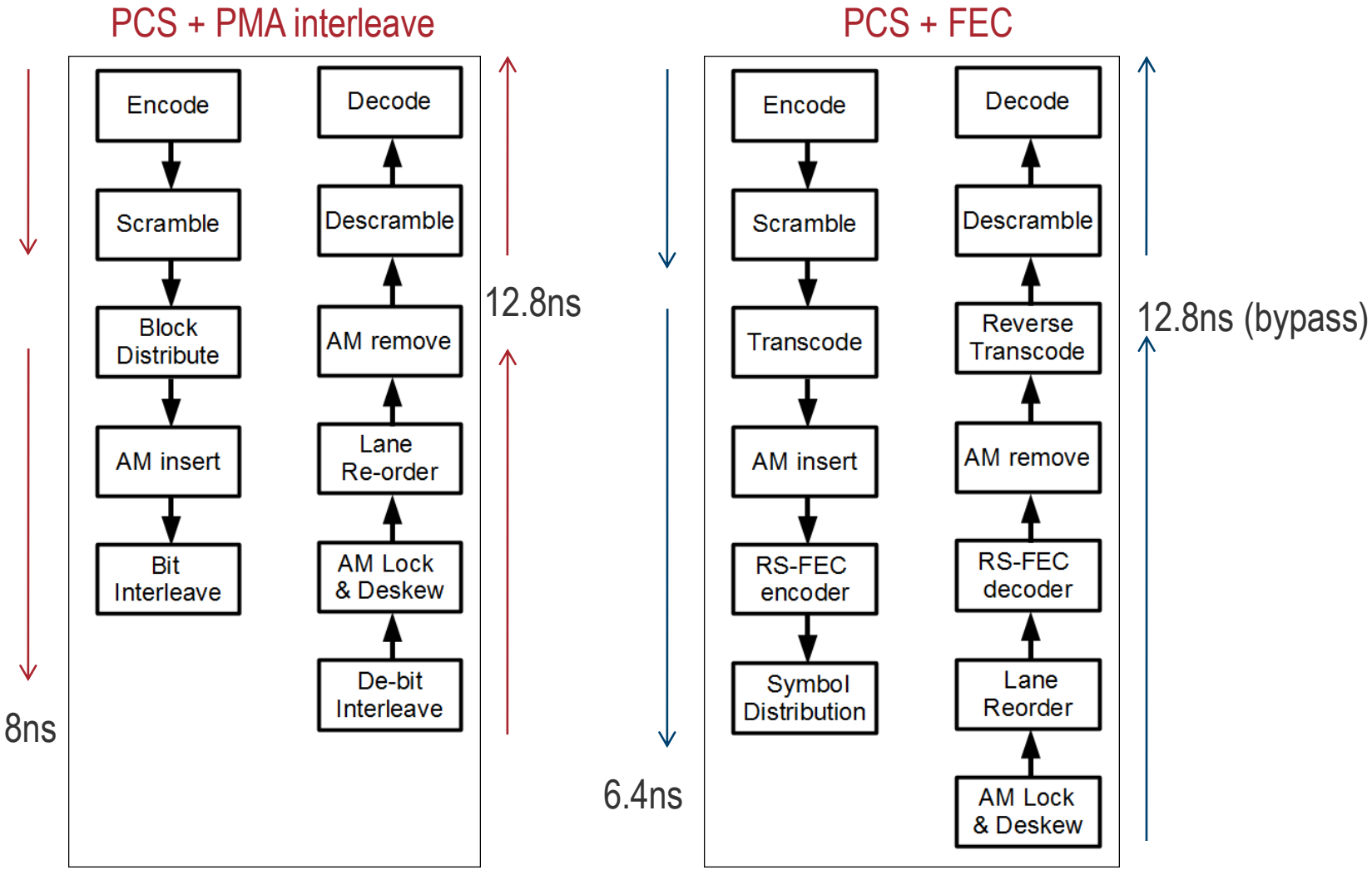
PCS + PMA interleave



PCS + FEC



Block diagrams for co-located design



Adding in RS(161,165) FEC option to proposed options for CAUI-4 C2C

	CTLE-only	CTLE + 5 Tap DFE		KR4
AN	No	No	No	Yes
PMD Training	No	No	No	Yes
RS(514,528,m=10) FEC	No	No	No	Yes
RS(161,165,m=8) FEC	No	No	Yes	No
Latency from PCS scrambler to descrambler[1] (ns)	20.8	20.8	~25 (correction on) ~18 (bypass)	~100 (correction on) ~55 (bypass)
Max Loss Budget (dB)[2]	15	20	20	35
Area	X	1.6X	1.65X	3.4X
Power	X	1.6X	1.6X	3.1X
MTTFPA	Acceptable	???	Acceptable	Acceptable

[1] Excludes common PMA/Channel latencies which are assumed to be the “same”

[2] Under ideal interference conditions.

RS(161,165) v. RS(514,528) performance

BER	Codeword (bits)	t	Corrected BER	codeword (bits)	t	Corrected BER
1.00E-05	1320	2	2.87E-10	5280	7	2.69E-19
1.00E-06	1320	2	2.90E-13	5280	7	2.82E-27
1.00E-07	1320	2	2.90E-16	5280	7	2.84E-35
1.00E-08	1320	2	2.90E-19	5280	7	2.84E-43
1.00E-09	1320	2	2.90E-22	5280	7	2.84E-51
1.00E-10	1320	2	2.90E-25	5280	7	2.84E-59
1.00E-11	1320	2	2.90E-28	5280	7	2.84E-67
1.00E-12	1320	2	2.90E-31	5280	7	2.84E-75
1.00E-13	1320	2	2.90E-34	5280	7	2.84E-83
1.00E-14	1320	2	2.90E-37	5280	7	2.84E-91
1.00E-15	1320	2	2.90E-40	5280	7	2.84E-99