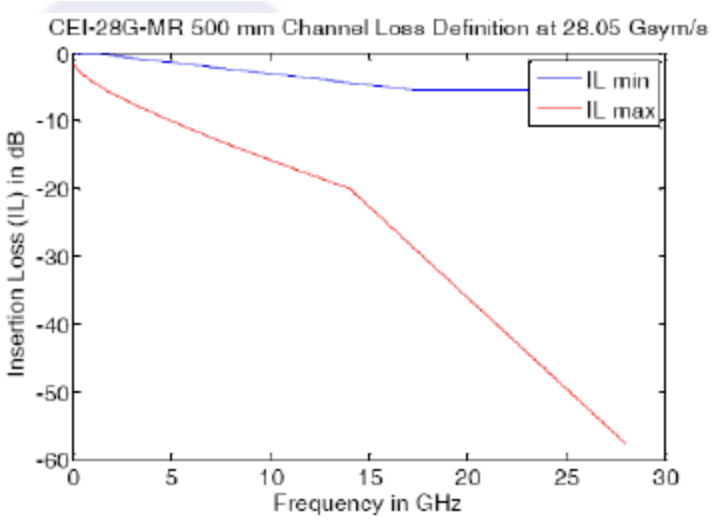
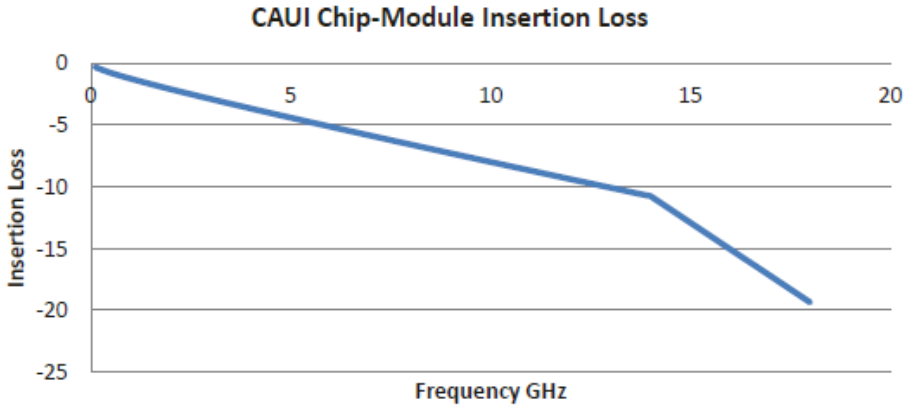
Agenda

- Patent Policy:
  - The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-Chip Discussion
  - Current Status
  - MTTFPA and chip-chip specification
- Chip-Module Draft Baseline
  - Specification BER discussion

Current Status of Chip-Chip

- Foundation for draft baseline: latchman_03_1112_optx.pdf
  - Transmitter
  - Channel
  - Receiver
- Material interest in 20dB link budget (similar to OIF MR)
  - ~10dB more loss than chip-module
    - ~5dB more than extended CTLE based discussions + Tx FIR
  - Most significant potential issue is mean time to false packet acceptance
    - Ability for IEEE CRC to detect corrupted frame





MTTFPA Background

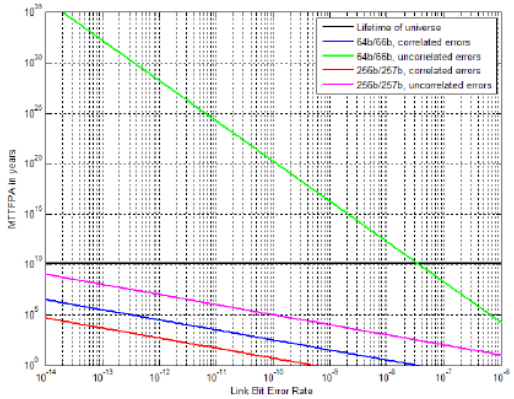
http://www.ieee802.org/3/bj/public/may12/cideciyan_01_0512.pdf

At 1E-15, low probability, the MTTFPA approaches lifetime of the universe for 64/66 data

MTTFPA Estimation – High Correlation Case

- For uncorrelated errors MTTFPA estimation is similar to MTTFPA of 512b/513b transcoding in *Teshima et al. "Bit-Error-Tolerant (512*N)b/(513*N+1)b Code for 40Gb/s and 100Gb/s Ethernet Transport", INFOCOM 2008.*
- Analysis accounts for correlated errors in MAC frame assuming a=0.5
- Basic ethernet frames of length 1518 bytes
- For correlated errors with a=0.5 MTTFPA is very low both for 64b/66b and 256b/257b

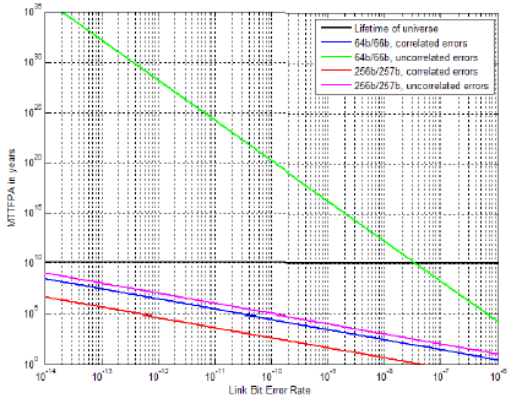
For correlated errors
prob. that burst error continues: a=0.5



MTTFPA Estimation – Low Correlation Case

- Analysis accounts for correlated errors in MAC frame assuming a=0.1
- Basic ethernet frames of length 1518 bytes
- For correlated errors with a=0.1 modest improvement in MTTFPA for 64b/66b and 256b/257b

For correlated errors
prob. that burst error continues: a=0.1



Turning off FEC decoder is not recommended for 256b/257b transcoded and FEC encoded data

Is MTTFPA an issue which modifies chip-chip baseline?

- No
  - Move forward with baseline assuming 20dB loss budget
  - Include a comment on correlated errors (which may apply to base 802.3ba document)
    - Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.
- Yes
  - Choose resolution to issue:
    - Change link budget
      - Would apps requirements be met?
    - Leverage bj as chip-chip
      - No need for new spec
    - Incorporate FEC in chip-chip
      - Reduces value proposition relative to bj
    - Add PCS to multiplex 66bit blocks
      - beyond scope

Chip-Module BER Discussion

- latchman_02_1112_optx.pdf

CAUI-4 Host Transmitter

	CR4 (D1.2, TP2)	VSR (7.2, TP1a)	CAUI-4 Chip-Module Potential
Signaling rate, per lane, Gb/s	25.78125 +/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak output voltage (max) with Tx disabled	35mV		35mV
Common Mode Voltage Range	0 - 1.9V	-0.3V (min) to 2.8V (max)	-0.3V (min) to 2.8V (max)
Differential output return loss (min)	SDD22>= 12-0.5f for 0.01<=f<=8 SDD22>= 5.65-9.71$\log_{10}$(f/14)	SDD22 < -11dB for 0.05<f<fb/7 SDD22 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD22>= 12-0.5f for 0.01<=f<=8 GHz SDD22>= 5.65-9.71$\log_{10}$(f/14) for 8<f<= 25 GHz
Common-mode AC output voltage (max,rms)	30mV	17.5mV	17.5mV
Amplitude peak-to-peak (max)	1200mV	900mV	900mV
Output total jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	0.54UIpp @ 10^{-15} Measured using CTLE	0.52UIpp @ 10^{-12} Measured using reference CTLE
Eye height peak-to-peak (min)		100mVppd @ 10^{-15} Measured using ref CTLE	106mVppd @10^{-12} Measured using ref CTLE

CAUI-4 Module Receiver

	VSR (7.2, TP1)	CAUI-4 Chip-Module Potential
Bit Error Ratio	10^{-15} or better per lane	10^{-12} or better

Straw Poll: Eye Opening Target

- 1E-12
  - A) Use OIF VSR numbers at 1E-12
    - 0.54UIpp@1E-12
    - 100mV @1E-12
  - B) Use extrapolation of OIF numbers to 1E-12
- 1E-15
  - C) Use OIF VSR numbers
    - 0.54UIpp @1E-15
    - 100mV @1E-15

Minutes

Attendees: Jonathan King, Rick Rabinovich, Vinu Arumugham , Dan Dove, Pete Anslow, Tom Palkert, Song Shang, Jeff Maki, Ted Sprague, David Ofelt, Scott Irwin, Galen Fromm, Charles Moore, Wheling Cheng, Piers Dawe, Gary Nicholl, Megha Shanbhag, Andre Szczepanek Greg Lecheminant, Mark Gustlin, Alex Umnov,

- Chip to chip
  - Focused on MTTFPA
    - Discussed further analysis required on probability of burst error based on DFE tap weights
    - Add header error analysis which is not covered in cideciyan_01_0512
  - Options discussed per slide 4
    - majority of interest in looking at how much reach is possible with a Tx FFE and Rx CTLE
    - Care needs to be taken with respect to ICN and ILD
    - Ball park estimate is 15dB channel support
    - Also need to consider proliferation of interfaces in the industry
- Discussed BER definition for eye opening spec
  - BER target for entire link vs CAUI budget (CAUI needs to be better than 1E-12 for link to be 1E-12)
  - What is practiced in industry vs what standard says (1E-12 often not acceptable)
  - Potential for 1E-15 spec to force sub-optimal spec for people that only want 1E-12
  - Straw poll per slide 6
- Straw poll results:
  - A: 4
  - B: 3
  - C:11