CAUI-4 chip-to-module recommended CTLE register

Pete Anslow, Ciena

IEEE P802.3bm Task Force, CAUI-4 Ad Hoc, 14 February 2014

IEEE P802.3bm D2.1 subclause 45.2.1.88c

Insert 45.2.1.88c after 45.2.1.88b (as inserted by IEEE Std 802.3bj-201x) as follows:

45.2.1.88c CAUI-4 chip-to-module recommended CTLE register (Register 1.169)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–67c. The value stored in this register corresponds to the CTLE peaking value (see 83E.3.1.6.1) recommended by the host (and used in the evaluation of host output compliance). The module may optionally use this information to adjust its CTLE setting.

Table 45–67c—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.169.15:6	Reserved	Value always 0, writes ignored	RO
1.169.5:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	RO
1.169.0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read only

Comments

- The recommended CTLE peaking value is a parameter that the host must communicate to the module. This needs to be done by the host writing this value into register 1.169 when a module is plugged in to the host.

  Consequently, bits 1.169.5:1 should be R/W and not RO as shown.

- Clause 45 is generally structured to have a subclause describing each register contents and then a set of subclauses beneath that describing each bit or group of bits. 45.2.1.88c contains both a description of register 1.169 and also a description of bits 1.169.5:1.

Proposed changes to 45.2.1.88c

Insert 45.2.1.88c and 45.2.1.88c.1 after 45.2.1.88b (as inserted by IEEE Std 802.3bj-201x) as follows:

45.2.1.88c CAUI-4 chip-to-module recommended CTLE register (Register 1.169)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–67c. ~~The value stored in this register corresponds to the CTLE peaking value (see 83E.3.1.6.1) recommended by the host (and used in the evaluation of host output compliance). The module may optionally use this information to adjust its CTLE setting.~~

Table 45–67c—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.169.15:6	Reserved	Value always 0, writes ignored	RO
1.169.5:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	~~RO~~ R/W
1.169.0	Reserved	Value always 0, writes ignored	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.88c.1 Recommended CTLE peaking (1.169.5:1)

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 chip-to-module interface defined in Annex 83E (see 83E.3.1.6). The module may optionally use this information to adjust its CTLE setting.

Thanks!