CAUI-4 Ad hoc

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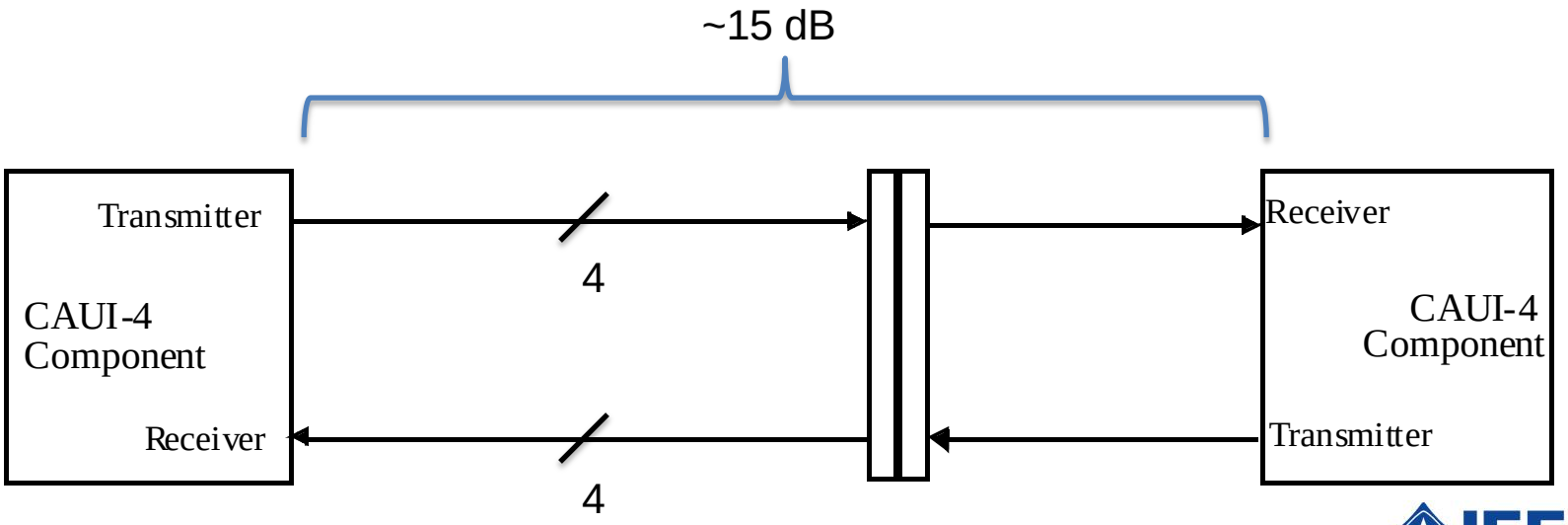
Agenda

- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- **Adhoc objective: chip-chip baseline for March**
- Chip to chip draft baseline
  - Application space
    - Channel
    - Transmitter
    - Receiver
  - Areas of focus

Application

- Chip to chip interface
  - Low power, low latency, AC coupled interface between ICs running at 4 x 25.78Gb/s
    - No FEC, No-DFE/or limited DFE (e.g., 1-tap or analog), no transmitter training
  - ~15 dB loss target with 1 connector (connector is optional)
    - Consistent with 25cm reach target
    - See http://www.ieee802.org/3/bm/public/nov12/palkert_02_1112_optx.pdf, http://www.ieee802.org/3/bm/public/nov12/ghiasi_03_1112_optx.pdf
    - Higher loss channels also under analysis to enable longer links



CAUI-4 chip to chip transmitter considerations

	KR4 (D1.4, TP0a)	MR	CAUI-4 chip to chip Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Differential peak-to-peak output voltage (max) with Tx disabled	30mV		30mVppd
Common Mode Voltage (max)	1.9V	1.7V	1.9V
Common Mode Voltage (min)	0V	-0.1V	0V
Differential output return loss (min)	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=19GHz	6dB , f<10GHz 4dB, 10G<f<25.78125GHz	RL(f)>= 6dB, 0.05<=f<=19GHz
Common-mode AC output voltage (max,rms)	12mV	12mV	12mV
Amplitude peak-to-peak (max)	1200mV	1200mV	1200mV
Transition Time (20%-80%, min, no EQ)	8ps	8ps	8ps
Max output Jitter			See following slide
Output eye mask			See following slide
De-emphasis range			See following slide

CAUI-4 chip to chip transmitter leveraging: 802.3ba

- Define output jitter at TP0a
  - Effective random jitter: 0.15UIpp
  - Even – odd jitter: 0.035UIpp
  - Total jitter: 0.28UIpp
  - No (or default) de-emphasis
- Define X1, X2, Y1, Y2 (TBD right now)
  - X1 = 0.14
  - Y2 = 600mV
  - X2/Y1 chosen to allow for rise/fall vs. swing trade off
  - De-emphasis off
- De-emphasis range
  - Minimum de-emphasis: TBD
  - Maxim de-emphasis: TBD
  - Minimum VMA: TBD

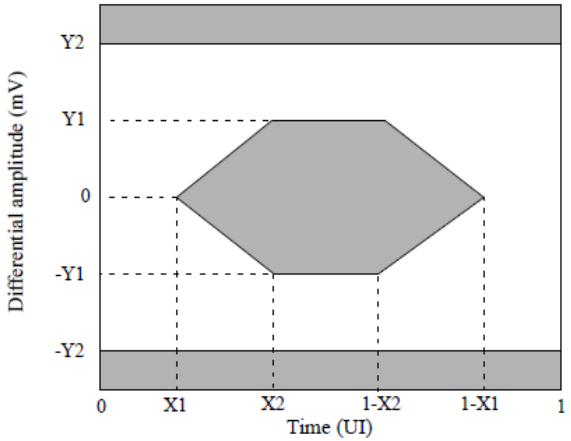


Figure 83A–8—Transmitter eye mask

$$\text{De-emphasis (dB)} = 20\log_{10}\left(\frac{\text{Differential peak-to-peak amplitude}}{\text{VMA}}\right) \quad (83A\text{–}3)$$

$$\text{Minimum VMA (mV)} = (234.64 - 2.13x + 0.18x^2) \times 1.32(10^{-y/20}) \quad (83A\text{–}4)$$

where

x is the rise or fall time (whichever is larger) in ps
y is de-emphasis value in dB

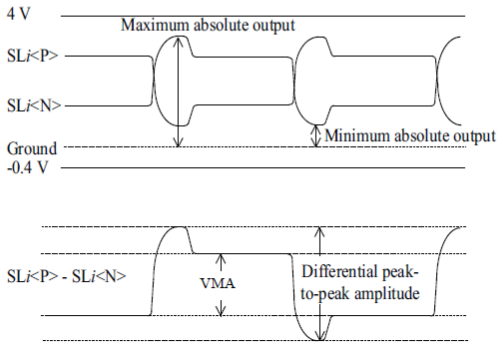


Figure 83A–5—Driver output voltage limits and definitions

CAUI-4 chip to chip transmitter leveraging: 802.3bj

Table 93–4—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	93.8.1.2	25.78125±100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled[a] Transmitter enabled	93.8.1.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	93.8.1.3	1.9	V
DC common-mode output voltage (min.)	93.8.1.3	0	V
AC common-mode output voltage (RMS, max.)	93.8.1.3	12	mV
Differential output return loss (min.)	93.8.1.4	Equation (93–2)	dB
Common-mode output return loss (min.)	93.8.1.4	Equation (93–3)	dB
Transition time (20-80%, min.), no equalization[b]	93.8.1.5	8	ps
Output waveform Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized RMS linear fit error (max.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	93.8.1.6	 0.6 0.4 0.8 × v_f 0.037 0.0083 0.05 1.54 1	 V V V — —
Far-end output noise (max.) Low insertion loss channel High insertion loss channel	93.8.1.7	 2 1	 mV mV
Output jitter (max.) Even-odd jitter Effective deterministic jitter excluding data dependent jitter Effective random jitter Total jitter excluding data dependent jitter	93.8.1.8	 0.035 0.15 0.15 0.28	 UI UI UI UI

Table 93–5—Linear fit pulse and equalizer parameters

Description	Symbol	Value	Units
Linear fit pulse length	N_p	8	UI
Linear fit pulse delay	D_p	2	UI
Equalizer length	N_w	8	UI
Equalizer delay	D_w	2	UI

Remove EQ

De-emphasis setting (s)

CAUI-4 chip –chip is relatively low loss

CAUI-4 chip to chip transmitter leveraging: OIF CEI SR

Table 10-6. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.90		28.05	Gsym/s
Output Differential Voltage	T_Vdiff	Emphasis off. See Note 4	800		1200	mVppd
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf	Emphasis off. See Note 2	8			ps
Common Mode Noise	T_Ncm	Note 3			12	mVrms
Differential Output Return Loss	T_SDD22	See Section 10.3.1.3				dB
Common Mode Output Return Loss	T_SCC22	Below 10 GHz			-6	dB
		10 GHz to baud rate			-4	
Output Common Mode Voltage	T_Vcm	Load Type 0 See Note 1	-100		1700	mV

NOTES:
1. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
2. The transmitter under test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The max value is limited by the linear fit pulse peak value in Table 10-11.
3. Measurement procedure is defined in Section 12.3.
4. T_Vdiff is two times the steady-state value V_f as defined in Section 10.3.1.6.2. The value is given as differential p-p voltage.

Table 10-7. Transmitter Output Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.15	UI_{PP}
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	Note 2			0.15	UI_{PP}
Duty Cycle Distortion (component of UBHPJ)	T_DCD	Note 3			0.035	UI_{PP}
Total Jitter	T_TJ	Note 1			0.28	UI_{PP}

NOTES:
1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Measured with all possible values of transmitter equalization, excluding DDJ as defined in 12.1.1.
3. included in T_UBHPJ

Table 10-11. Transmitter output waveform requirements

Parameter	Condition	Units	
Steady state output voltage, 2 x v_f	max	mVppd	1200
Steady state output voltage, 2 x v_f	min	mVppd	800
Linear fit pulse peak, p_{max}	min	-	0.80 x v_f
RMS error, σ_e	max	-	0.027 x v_f

Table 10-10. Linear fit pulse and equalizing filter parameters

Parameter	Value (UI)
Linear fit pulse length T_N_p	8
Linear fit pulse delay T_D_p	2
Equalizer length T_N_w	8
Equalizer delay T_D_w	2

Link budgets in this document assume adaptive TX FIR equalization that is part of the system management function. The specific implementation is outside the scope of this document.

CAUI-4 chip to chip channel leveraging: “Traditional” / OIF CEI SR

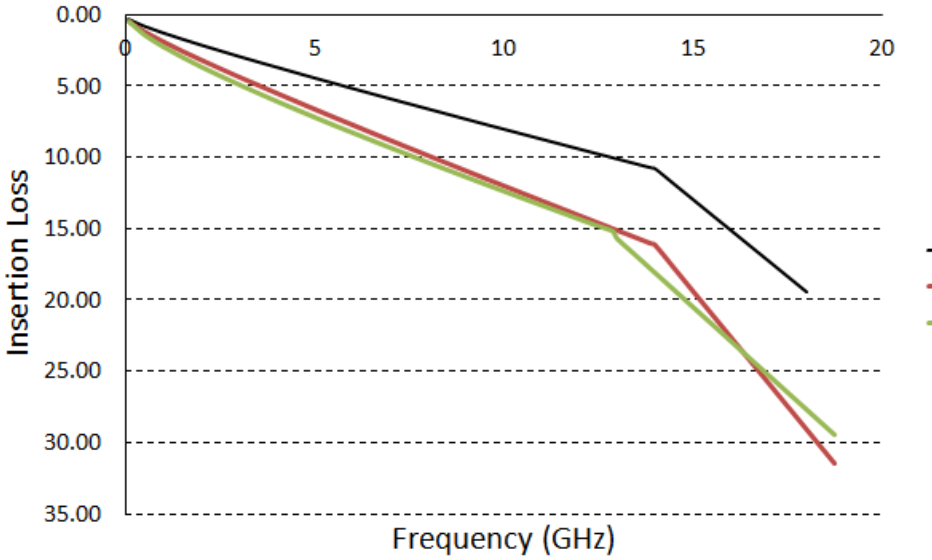


Table 10-1. Measured Channel Parameters

Symbol	Description
$IL(f)$	Differential insertion loss, -SDD21 magnitude (dB)
$RL_1(f)$	Differential input return loss, -SDD11 magnitude (dB)
$RL_2(f)$	Differential output return loss, -SDD22 magnitude (dB)
$NEXT_m(f)$	Differential near-end crosstalk loss (m^{th} aggressor), -SDD21 magnitude (dB)
$FEXT_n(f)$	Differential far-end crosstalk loss (n^{th} aggressor), -SDD21 magnitude (dB)

Table 10-2. Calculated Channel Parameters

Symbol	Description
$IL_{fitted}(f)$	Fitted insertion loss (dB)
$ILD(f)$	Insertion loss deviation (dB)
$ICN(f)$	Integrated crosstalk noise (mV, RMS)
$ILD(rms)$	RMS value of the insertion loss Deviation (dB)

- Insertion Loss = 1.614 (0.075 + .537f^(0.5) + 0.566f) 0.01<=f<14
  1.614 (-18+2f) 14<=f<18.75
- Return loss = TBD
- ILD = TBD
- ICN = TBD
- ILDrms = TBD
- Or insertion loss increase depending on simulation results with Mike’s channel (http://www.ieee802.org/3/bm/public/jan13/li_01_0113_optx.pdf)

CAUI-4 chip to chip channel leveraging: 802.3bj

Table 93–9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance	 C_d z_p C_p	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	14	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.07	UI
Receiver additive Gaussian noise, RMS	σ_r	1	mV
Target detector error ratio	DER_0	10^{-5}	—

93.9.1 Channel operating margin

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 93–9 shall be greater than or equal to 3 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

TBD

Modify to fixed setting

Modify to fixed setting

Increase the AC gain of CTLE?

Set to zero

Remove

1e-12 (or 1e-15) - TBD

CAUI-4 chip to chip receiver considerations

	KR4 (D1.4, TP5a)	MR	CAUI-4 chip to chip Potential
Differential Input Return loss (min)	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz
Differential to common mode input returnloss	RL(f) = 25-1.44f 0.05<=f<=6.95 15 6/95<f<=19		RL(f) = 25-1.44f 0.05<=f<=6.95 15 6/95<f<=19
Interference Tolerance	Table 93-7		RL(f) >= 20-1.44*f for 0.01<=f<=6.95 15 from 6.95<=f<=13
Jitter tolerance	Table 93-8		
Input amplitude (max)		1200	TBD

Receiver Interference/Jitter Tolerance leveraging 802.3bj

Parameter	Test values
Maximum BER*	10^{-12}
Channel Insertion Loss at 12.89GHz	~15dB
Applied peak-to-peak sinusoidal jitter (covering CDR JTOL)	TBD
Applied peak-to-peak random jitter	TBD
Applied even-odd jitter	TBD
Applied RMS broadband noise	TBD

* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Receiver Interference/Jitter Tolerance leveraging OIF CEI SR

Table 10-12. Receiver Electrical Input Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud rate	R_Baud		19.90		28.05	GSym/s
Input Differential Voltage	R_Vdiff	Note 1			1200	mVppd
Differential Input Impedance	R_Rdin		80	100	120	Ω
Input Impedance Mismatch	R_Rm				10	%
Differential Input Return Loss	R_SDD11	See 10.3.2.3				
Common Mode Input Return Loss	R_SCC11	Below 10 GHz			-6	dB
		10GHz to baud rate			-4	
Input Common Mode Voltage	R_Vcm	Load Type 0 See Note 2	-200		1800	mV

NOTES:
1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst case effects of the return losses at the transmitter and receiver.
2. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load. For floating load, input resistance shall be ≥ 1kΩ

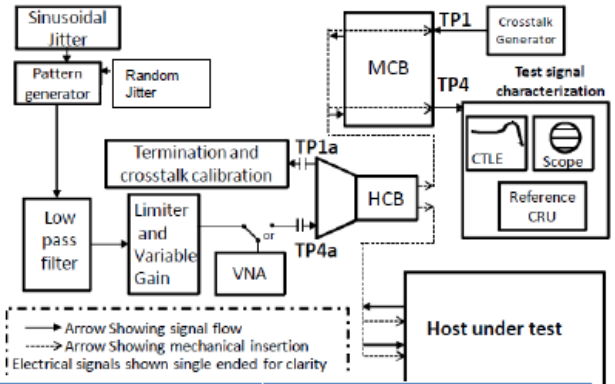
Table 10-13. Receiver Input Jitter Specification

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Sinusoidal Jitter, Maximum	R_SJ-max	See Section 2.5.4, note 1			5	UIpp
Sinusoidal Jitter, High Frequency	R_SJ-hf	See Section 2.5.4, note 1			0.05	UIpp

NOTES:
1. The Receiver shall tolerate the sum of these jitter contributions: Total transmitter jitter from Table 10-7;Sinusoidal jitter as defined in Table 10-13;The effects of a channel compliant to the Channel Characteristics (Section 10.2.6).

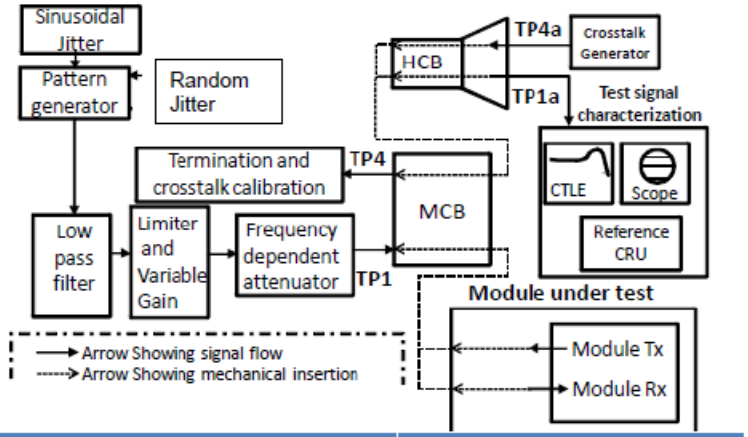
Chip-module methodology

Host Stress Receiver Test



Host Stress Receiver Test	Eye Opening after reference CTLE
Minimum Total Input Jitter Tolerance	0.41UIpp 10^{-12}
Applied peak-peak sinusoidal jitter	5 x 10^5/f (100kHz<f<=10MHz) 0.05UI (10MHz<f<10 LB)
Eye Height	246mVpp

Module Stress Receiver Test



Module Stress Receiver Test	Eye Opening after reference CTLE
Minimum Total Input Jitter Tolerance	0.51UIpp 10^{-12}
Applied peak-peak sinusoidal jitter	5 x 10^5/f (100kHz<f<=10MHz) 0.05UI (10MHz<f<10 LB)
Eye Height	106mVpp

Compliance points

- **See 93.8.2.1 Receiver test fixture from 802.3bj for TP5a**
- **See 93.8.1.1 Transmitter test fixture from 802.3bj for TP0a**

Straw Poll

- I prefer to specify the transmitter for CAUI chip-chip using the methodology described in
  A. 802.3ba CL 83A
  B. 802.3bj CL93 / OIF CEI 28G SR
  C. CAUI-4 chip-module (TP4)
  D. CAUI-4 chip-module (with software channel)
- I prefer to specify the channel for CAUI chip-chip using the methodology described in
  A. 802.3bj CL93 (COM)
  B. OIF CEI 28G SR
- I prefer to specify the receiver / tolerance for CAUI chip-chip using the methodology described in
  A. 802.3bj CL93
  B. OIF CEI 28G SR
  C. CAUI-4 chip-module

Minutes

- Discussed IEEE patent policy
- Reviewed latchman_01_0213_caui
  - Adhoc should ideally agree on methodology for baseline, but a baseline can still be put together without full agreement (leverage TBDs)
  - Discussed chip-chip DC coupling
    - Potentially two specs
    - Concern with potential interoperability
- Transmitter methodology discussion
  - VSR methodology discussed with software channel + CTLE -> look at eye diagram
    - Actual far end channel measurements also discussed
    - CAUI chip-chip specification ideally should allow designers to trade-off rise/fall, de-emphasis, swing
  - 802.3bj CL93 methodology discussed
    - Interest in leveraging chip-module methodology, or bj methodology (avoid creating new methodology)
    - Can KR spec be a super set?
    - Potential to relax amplitude, linear fit error
    - Have fixed number of de-emphasis settings to keep solution space manageable (~2 settings), discussed post cursor only emphasis
- Channel methodology discussion
  - OIF SR 28G method discussed
  - COM method discussed, added reference to COM value with TBD (potentially use 3dB as a starting point)
- Receiver methodology discussion
  - Discussed OIF and 802.3bj CL93 methodology
  - Added chip-module methodology
  - Preference to use simpler setup
- Next meeting: 28/02/2013 at 9:00am PT