CAUI-4 Ad hoc

Ryan Latchman, MACOM

Agenda

- Patent Policy: This meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting.
  http://www.ieee802.org/3/patent.html
- Presentations:
  - Proposed modifications for bounded uncorrelated jitter used in host and module stressed test setup
  - Adee Ran: MDIO for chip-chip
- Next meeting: TBD

- Host stress text modification

83E.3.3.3.1 Host stressed input test procedure¶

The host stressed input test is summarized in Figure 83E–14. The stress signal is applied at TP4a, and is calibrated at TP4. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9) as defined in Table 86-11. The reference receiver includes a selectable software CTLE given by Equation (83E–4) and the first two rows of Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern. The amount of applied peak-to-peak sinusoidal jitter used for the host stressed input test is given in Table 83E–5. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error rate testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS11. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 Gbd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit single pole roll-off with a -3dB knee between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter is added such that the output of the pattern generator approximates a jitter profile given in Table 83E–6.¶

• • • • • •

the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude is adjusted to result in the eye height and eye width given in Table 83E–5 using the reference receiver. ¶

- Host stress updated figure

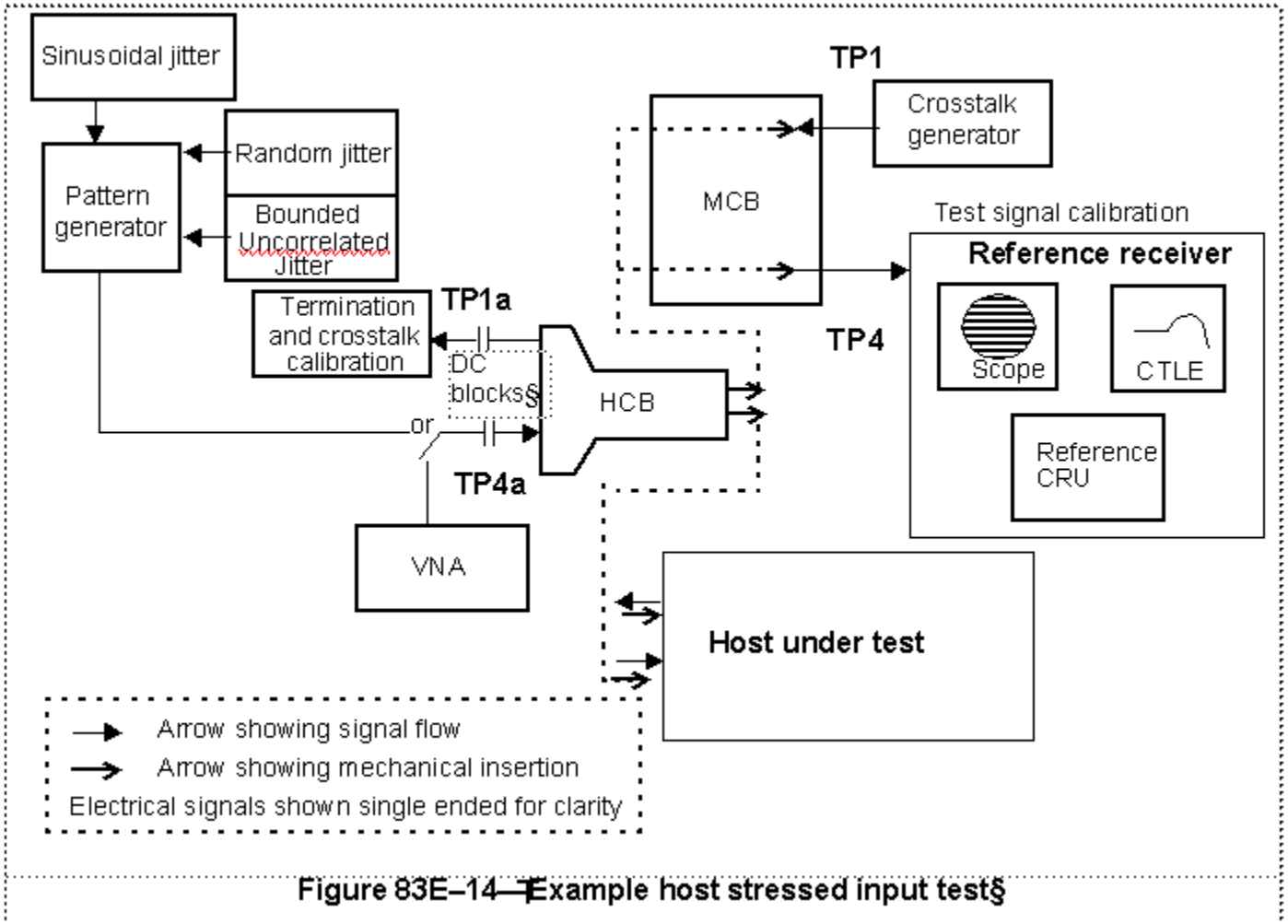

Figure 83E–14—Example host stressed input test§

- Module stress text modification

83E.3.4.2.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 83E–15. The stress signal is applied at TP1, and is calibrated at TP1a. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9) as defined in Table 86-11. The reference receiver includes a selectable software CTLE given by Equation (83E–4) and Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel, and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 83E–8. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error rate testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS11. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 Gbd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit single pole roll-off with a -3dB knee between 150MHz and 300MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter is added such that the output of the limiting function approximates a jitter profile given in Table 83E–9.

• • • • • •

the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. For the low loss case, discrete frequency dependent attenuation is removed such that from the output of the limiter to TP1a comprises the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the

- Module stress updated figure

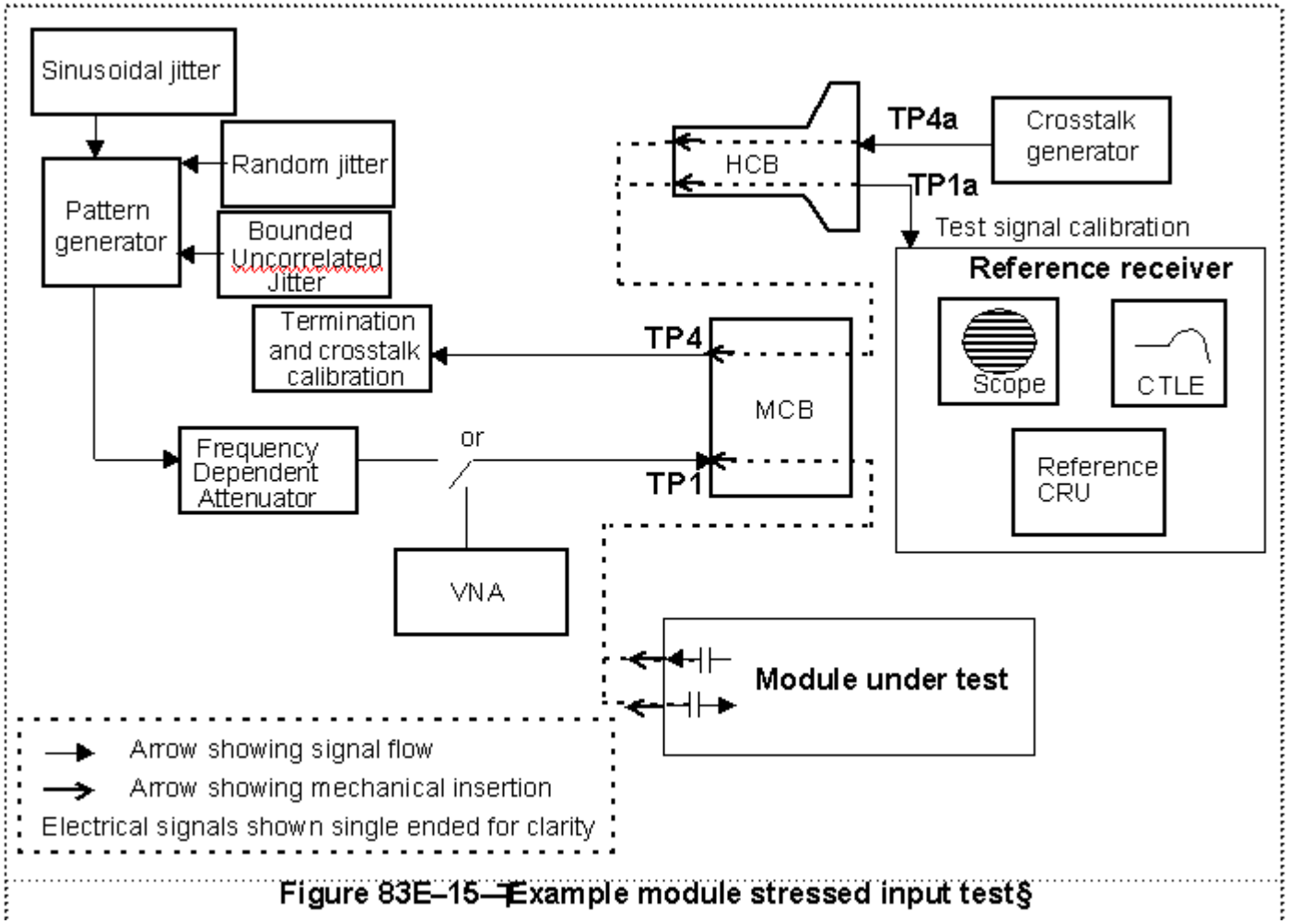

Figure 83E–15—Example module stressed input test§