

MDIO access to CAUI-4 C2C

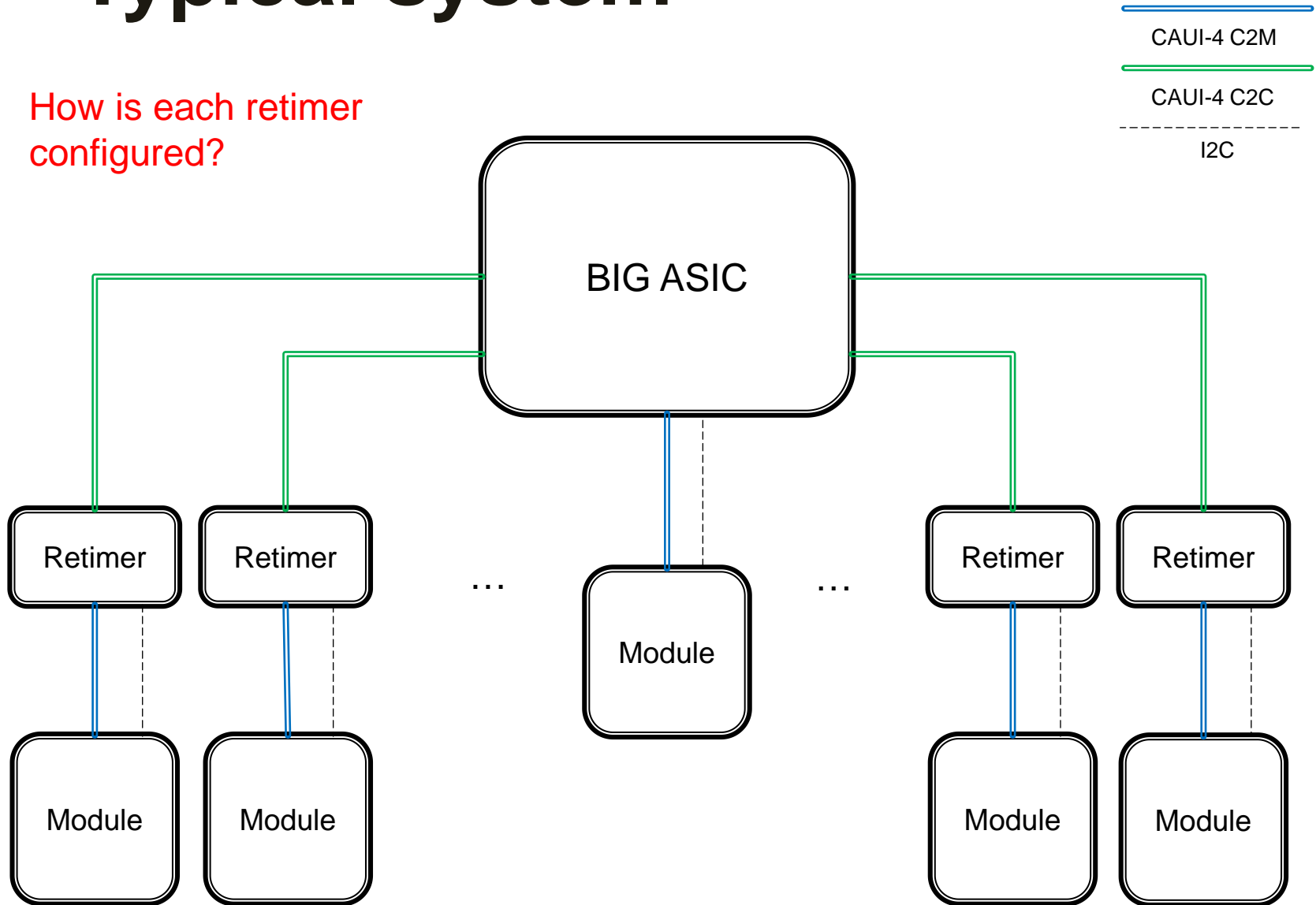
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February 2014

In short

- A system can comprise several CAUI-4 C2C links and multiple “chips”
- Chips are likely to require different settings:
 - Transmitter equalization toward the “partner”
 - CTLE settings for receiving from the “partner” (may or may not be adaptive)
 - CTLE settings for receiving from an attached module (C2M) (may or may not be adaptive)
 - Recommended CTLE settings for the attached module
- These settings would be easier to manage if stored centrally and communicated to the chips in a standardized way. MDIO is a natural choice.

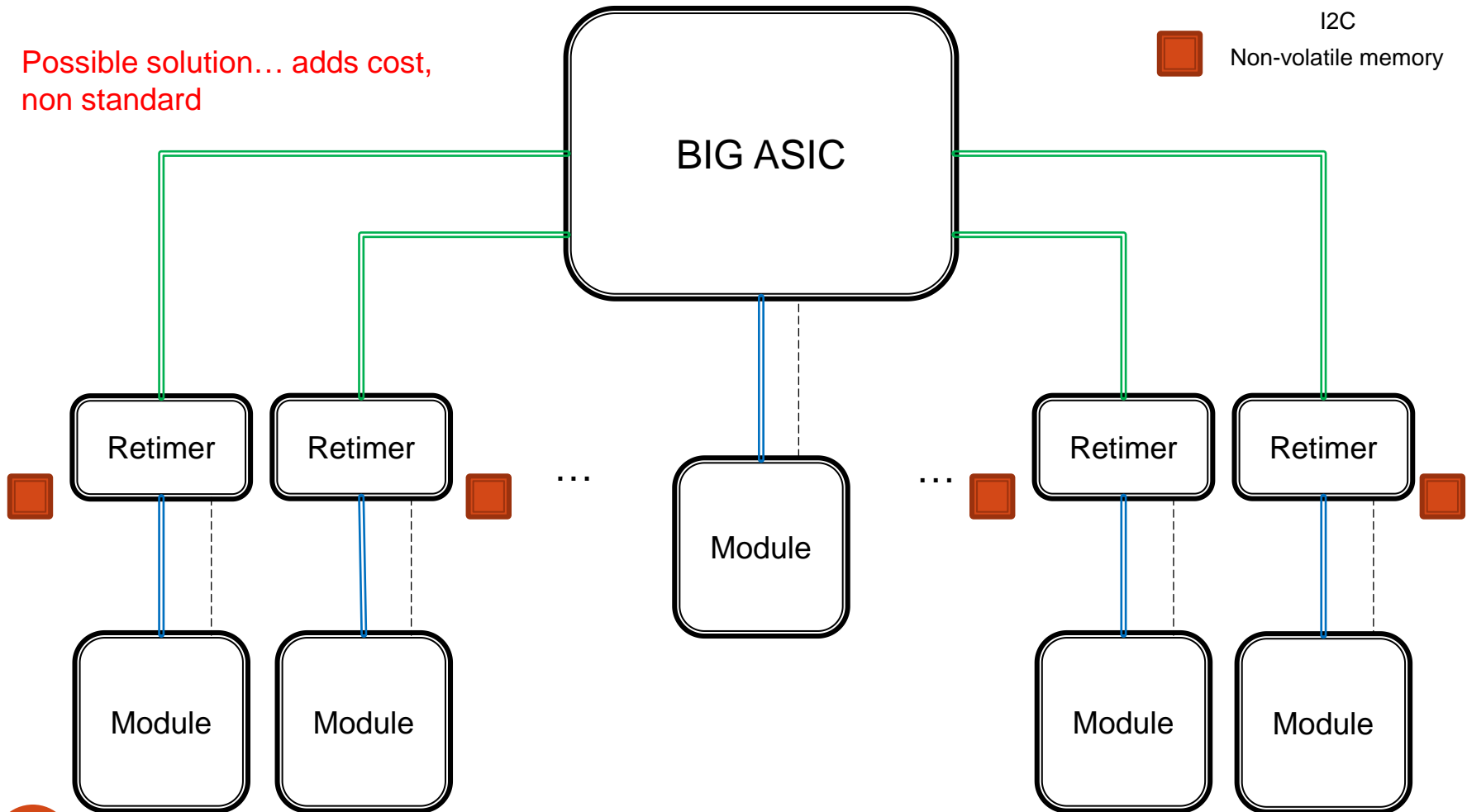
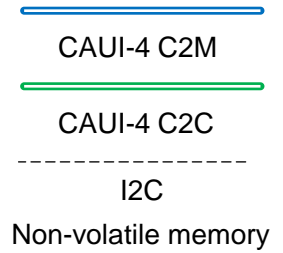
Typical system

How is each retimer configured?

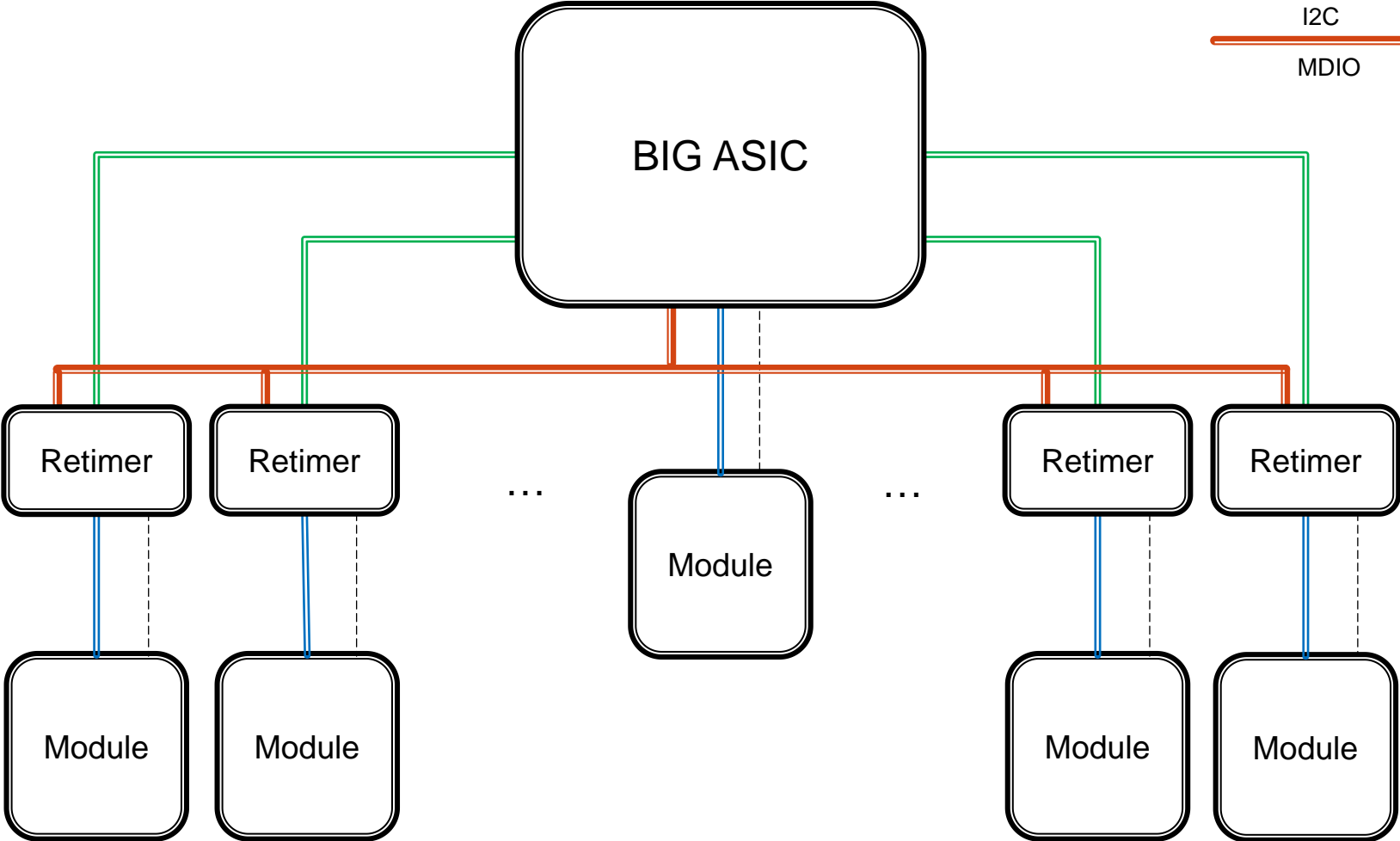
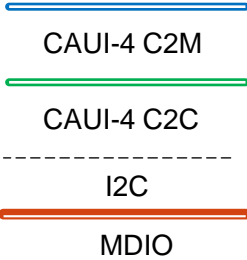


Without a management interface...

Possible solution... adds cost, non standard



With MDIO



Notes

- Transmitter has 4 setting for $c(-1)$, 6 settings for $c(1)$ – making 24 combinations (assuming $c(0)$ complements to 1)
- There is a possibility for multiple retimers in the path.
 - If each one has its own device ID, they can be programmed separately.
 - It is possible to have two sets of parameters per device – one for transmit direction, one for receive direction (as defined in clause 83).
- Additional registers can be used for each device to be informed of, and ask to change its partner's TX setting
 - Enables FFE tuning with a request/response mechanism
 - Managed by one MDIO device by MDIO reads/writes
 - Implementation need not be specified

Proposed solution

- Add optional MDIO registers for a PMA/PMD device controlling CAUI-4 C2C equalization.
- Two registers in each direction (transmit/receive):
 1. Local equalization control
 - Transmitter coefficient setting – 2 bits for $c(-1)$, 3 bits for $c(1)$ \Rightarrow 5 bits, R/W
 - Receiver CTLE setting – 4 bits, R/W
 2. Remote equalization control
 - Equalization setting of the partner's PMA transmitter – 2 bits for $c(-1)$, 3 bits for $c(1)$ \Rightarrow 5 bits, R/W
 - Equalization setting requested from the partner's PMA transmitter – 2 bits for $c(-1)$, 3 bits for $c(1)$ \Rightarrow 5 bits, RO
- Four addresses need to be allocated (in addition to the existing chip-to-module CTLE register).

Bit assignments and meaning

- For the CTLE setting: 4 bits
 - Decimal value 0: unspecified (let device decide)
 - Decimal values 1-12: programmed peaking value
 - Decimal values 13-15: reserved
- For the transmitter coefficient settings:
 - Bits 1:0 – precursor coefficient ($c(-1)$) per table 83D–7
 - Bits 4:2 – postcursor coefficient ($c(1)$) per table 83D–8; values 6 and 7 reserved
 - Bits 7:5 – reserved
- If the “transmit direction” is a CAUI-4 C2M, then
 - Only the CTLE part of the Local equalization control register can be used (possibly limiting to settings 1-9)
 - Remote equalization control register has no effect.

Thank you

Discussion...?