CAUI-4 Chip to Chip Burst Errors

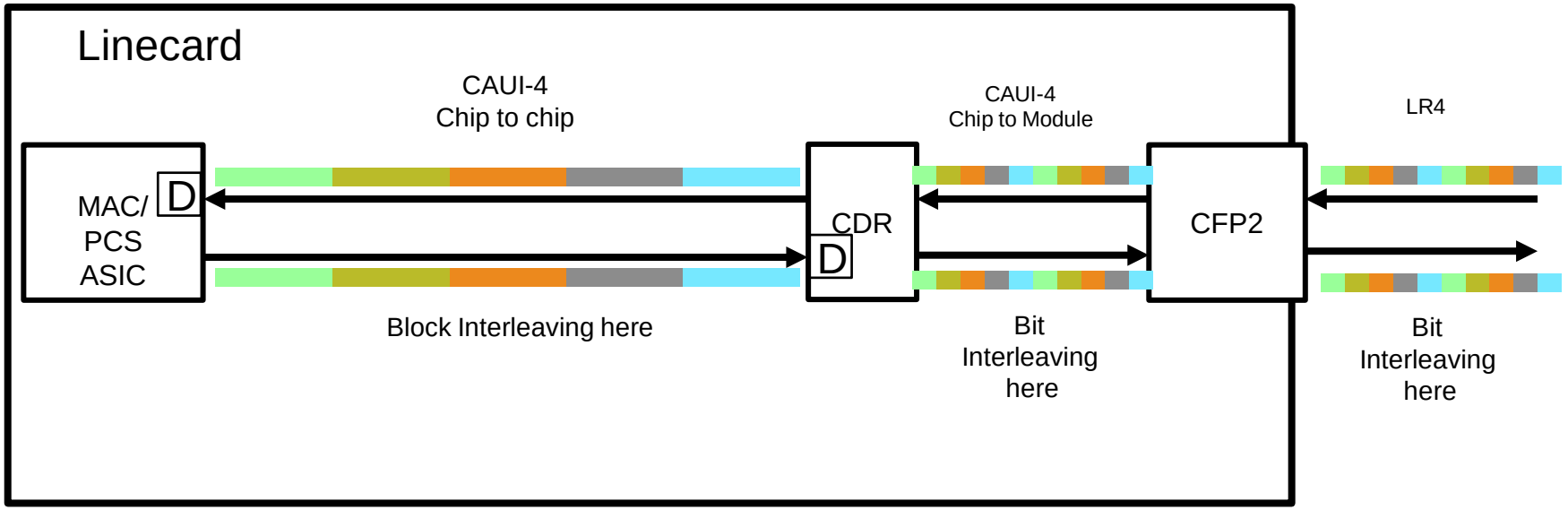
IEEE P802.3bm

January 2014 Indian Wells??

Introduction

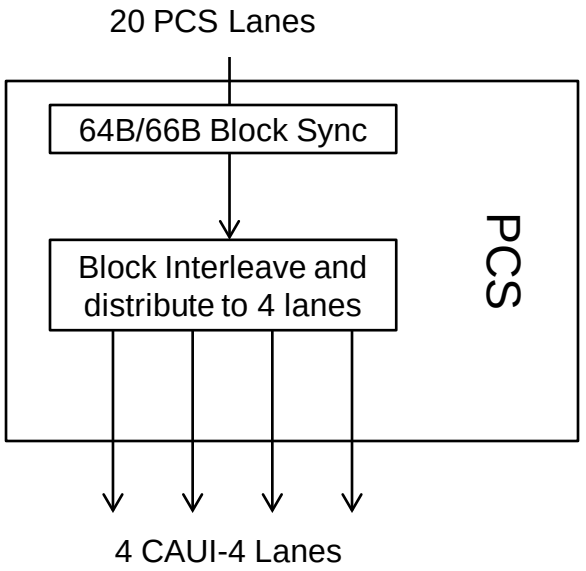
- The current 20dB CAUI-4 chip to chip interface requires DFE to close the link
- DFE can cause burst errors can cause a lower MTTFPA than some are comfortable with
- Why do burst errors cause the concern?
  - With CAUI-4 spans without FEC, and with bit multiplexing, a single 4 bit burst can cause errors in 4 separate PCS lanes
  - With skew and the muxing in the path, you cannot predict where the errors are in the packet
  - Therefore you rely on the CRC32 to detect the errors, with a probability of 1/(2^32)
- A simple fix is to block multiplex, why does this solve the issue?
  - With block multiplexing, a single burst error impacts up to two PCS lanes only and creates up to two burst errors
  - CRC32 is guaranteed to detect a double burst error up to 9bits per burst, anywhere in the packet
- Block muxing would only be done on a non FEC encoded link, and only for CAUI-4 chip to chip interfaces

System Example



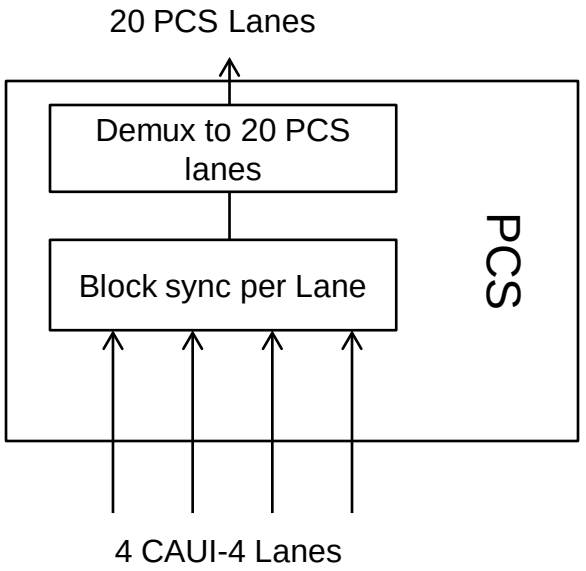
Data Flow - TX

- You find block sync on all 20 PCS lanes
- Then perform block interleaving and distribute to 4 CAUI-4 lanes
- No need to fully de-skew or reorder lanes



Data Flow - RX

- You find block sync on all 4 CAUI-4 lanes
- Then distribute to 20 PCS lanes
- No need to fully de-skew or reorder PCS lanes



Thanks!