CAUI-4 MTTFPA: "Divide and Conquer"?

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Rationale

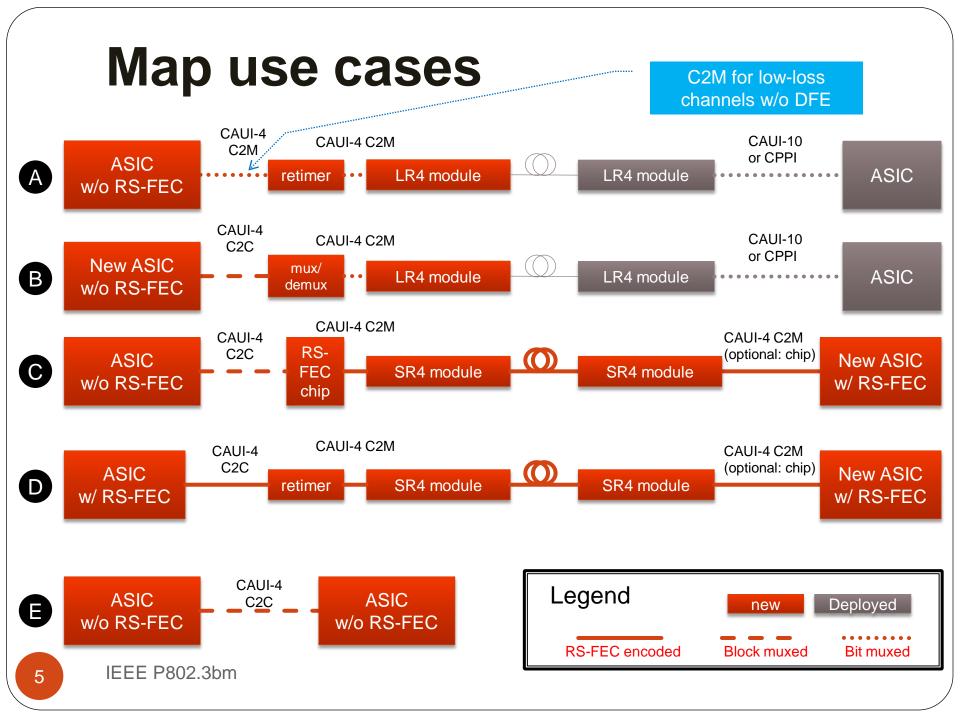
- From recent discussions it seems that there is no 100% acceptable solution to MTTFPA concerns in CAUI-4.
- Trying to think out of the box
- Redefine the playground boundaries... what would be acceptable?

We would like to have

- CAUI-4 C2C usage models:
 - 1. Extension of ASIC-to-Module range using an extender chip
 - Full link includes a partner of the same type, possibly an existing LR4 system
 - The extender output must be compatible with SR4/LR4
 - 2. Inter-ASIC short-reach connection
 - No PMD
 - No existing CAUI-4 systems (but perhaps "candidate chips")
- Specifications must be testable in a reasonable period
- MTTFPA should be guaranteed by design

Further drill down use cases

- 100GBASE-LR4: if CAUI-4 channel is short enough it can do without a DFE (simple retimer)
- 100GBASE-SR4: if CAUI-4 is below the RS-FEC sublayer, it is protected – MTTFPA not an issue
- Otherwise (CAUI-4 needs DFE and is not protected by RS-FEC):
 - MTTFPA concern if bit muxing is used (20:4 PMA)
 - Ideas for mitigation included transformations of the data stream on both sides (e.g. new FEC, precoding)...
 - An easy transformation is to use **66-bit block muxing** instead if bit muxing; this makes error bursts tolerable.
 - This should be undone by the Extender chip.



How is each case solved?

- Case A does not include a DFE so errors can be expected to be independent.
 - Assumes both sides of the retimer ("chip" specs) and both channels meet Annex 83E specs.
- Cases B, C and E:
 - Have segments which may require a DFE, but all traffic uses 66-bit block multiplexing, which is tolerant to bursts
 - This can be viewed as a PMA replacement or an additional translation sublayer on both sides of the CAUI-4 C2C.
- Case D is tolerant to bursts due to RS-FEC.