CAUI-4 Chip to Chip Simulations

IEEE 802.3bm Task Force

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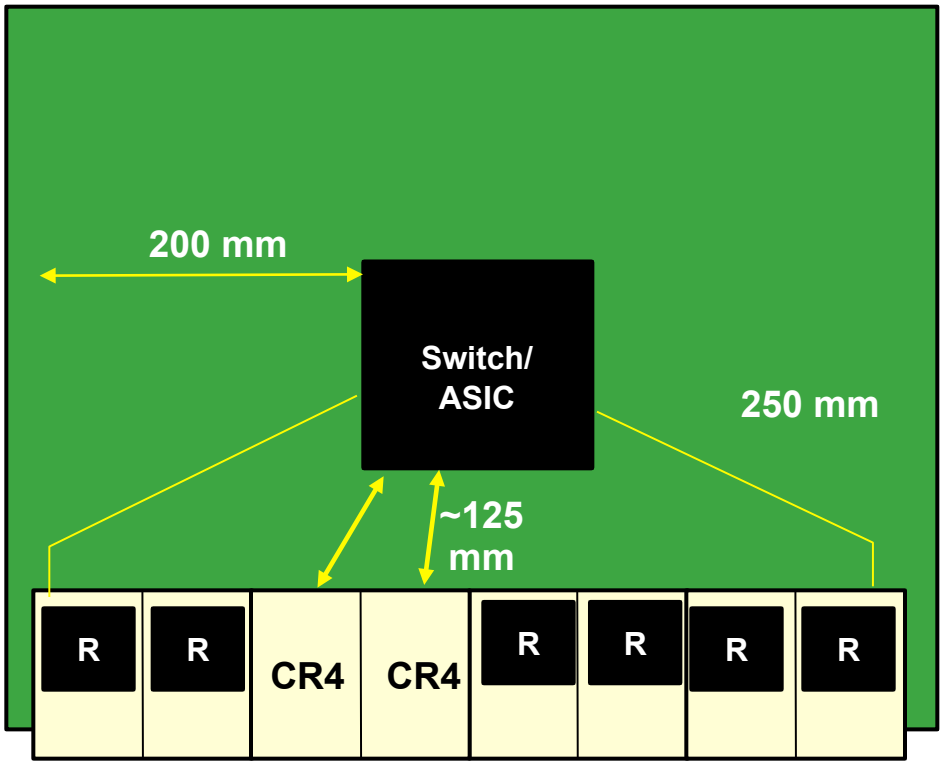
Phoenix

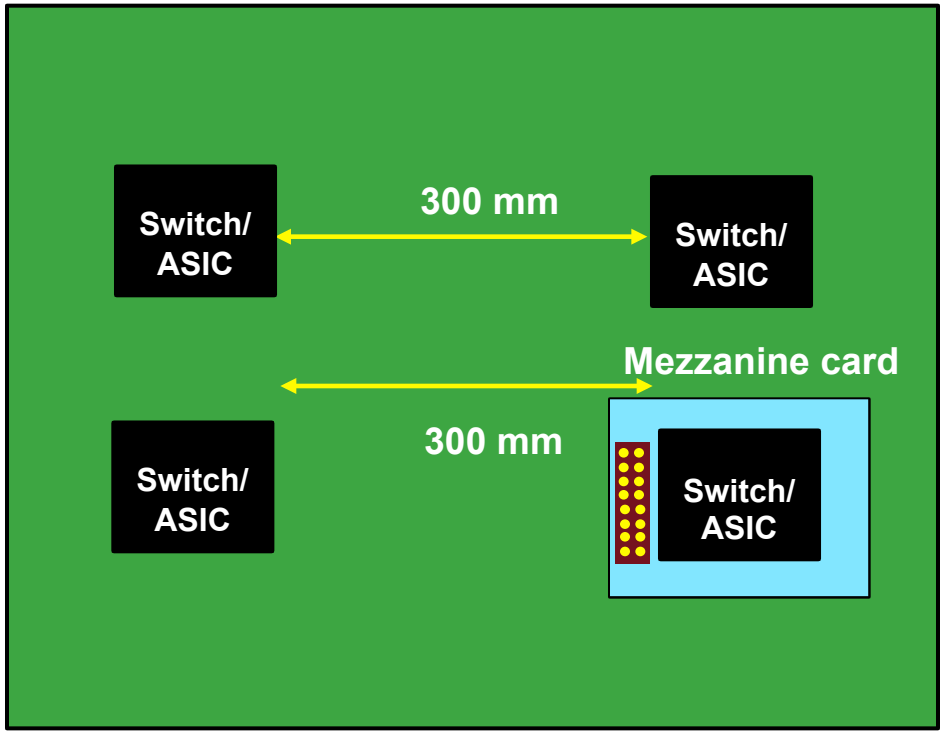
Overview

- A CAUI-4 chip to chip link with 20 dB loss budget require DFE receiver and to avoid MTTFPA capability similar to 100Gbase-K4 is required
  - Based on the above limitation turning down some of the bj KR4 capability is the best option
  - MTTFPA was studied in great details in the bj group http://www.ieee802.org/3/bj/public/may12/cideciyan_01_0512.pdf
  - Non-symmetrical link based on host with greater capability to deliver the required signal at TP1a and relying on host DFE receiver also may not be an option
- Based on above limitations and the market need for higher than 10 dB loss budget
  - CAUI-4 chip to chip can be defined with loss budget up to 13 dB and could be engineered to as much as 15 dB with CTLE receiver
  - CAUI-4 chip to chip will be compatible with CAUI-4 chip to module

CAUI-4 Applications and Background

- http://www.ieee802.org/3/bj/public/jul12/ghiasi_02a_0712.pdf identified CAUI-4 applications as well as limitations
  - As result of MTTFPA, non-symmetrical interface is not an option unless module retiemr has FEC capability
  - Supporting 300 mm link require SerDes with bj KR4 capability
  - Is it really worth defining bj-KR4 link with 20 dB loss budget?





PCB Reach for Various Interfaces

- PCB loss estimate assumptions and tools for calculation
  - IEEE 803.bj spreadsheet http://www.ieee802.org/3/bj/public/tools/DkDf_AlgebraicModel_v2.02a.xlsm for N4000-13SI and Megtron-6 calculation
  - Rogers Corp impedance calculator (free download but require registration) https://www.rogerscorp.com/acm/technology/index.aspx for FR4-6 and N4000-13
  - Stripline ~ 50 Ω, trace width is 5 mils, and with ½ oz Cu
  - Surface roughness med per IEEE spreadsheet or 2.8 um RMS
  - FR4-6 DK=4.2 and DF=0.02, N4000-13 DK=3.6 and DF=0.014, N4000-13SI and Meg-6 per IEEE spreadsheet

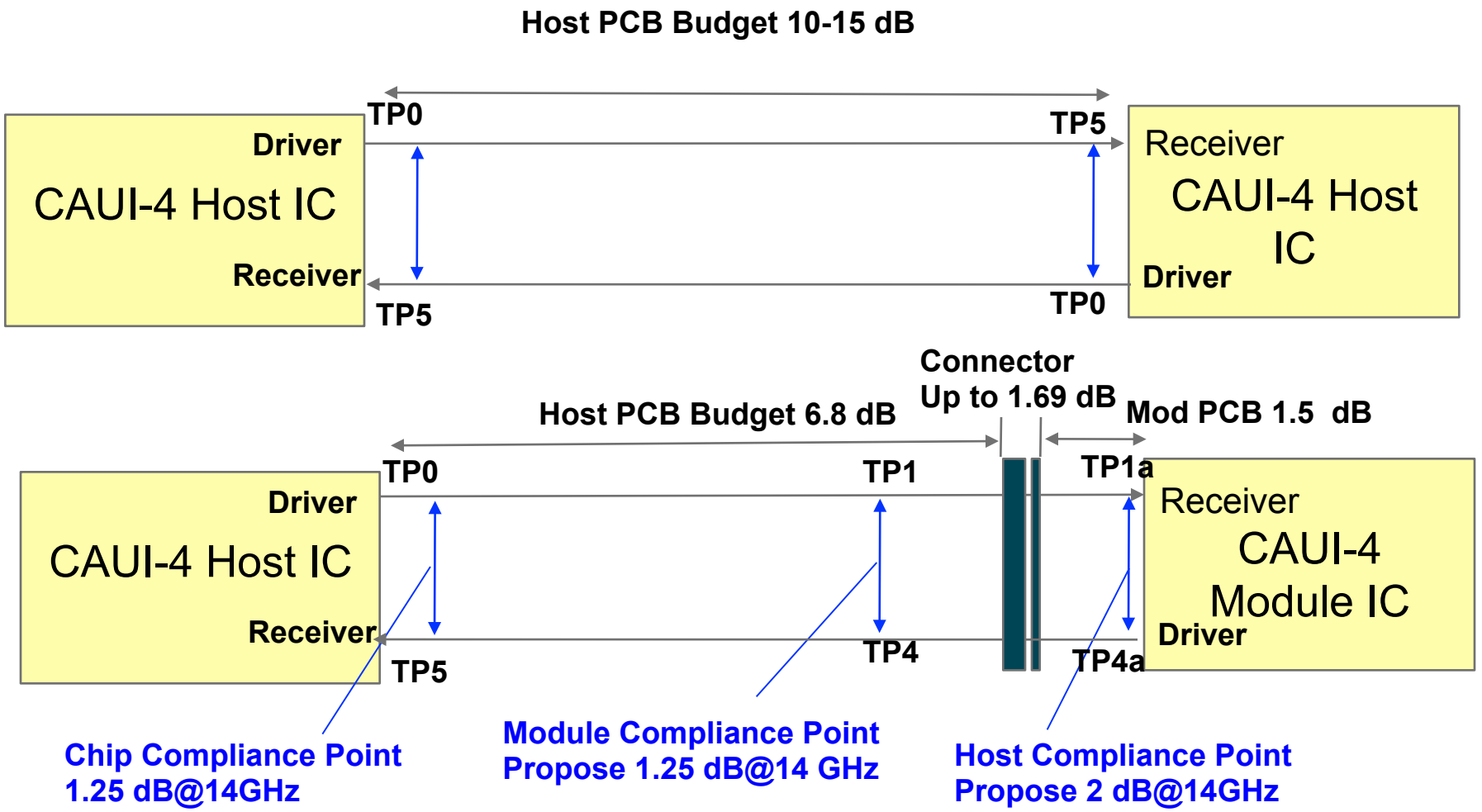
Host Trace Length (in)	Total Loss (dB)	Host Loss(dB)	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal PCB Loss/in at 5.15 GHz	N/A	N/A	1.00	0.79	0.56	0.43
Nominal PCB Loss/in at 12.89 GHz	N/A	N/A	2.00	1.60	1.25	0.92
CAUI Classic	10.5	6.81	6.8	8.6	12.2	15.8
PPI CL85A/86A with one connector & HCB#	6.5	4.37	4.4	5.5	7.8	10.2
CAUI-4 with one connector & HCB*	10.5	6.81	3.4	4.3	5.4	7.4
802.3bj CL92A with one connector & HCB *	10.5	6.81	3.4	4.3	5.4	7.4
CAUI-4 Chip to Chip	10	10	5.0	6.3	8.0	10.9
CAUI-4 Chip to Chip	13	13	6.5	8.1	10.4	14.1
CAUI-4 Chip to Chip Engineered	15	15	7.5	9.4	12.0	16.3
OIF 28G-MR	20	20	10.0	12.5	16.0	21.7

Assumes connector loss is 0.87 dB and HCB loss is 1.26 dB at 5.5 GHz.

* Assumes connector loss is 1.69 dB and HCB loss is 2.0 dB at 12.89 GHz.

CAUI-4 Architecture and Reference Points

- The bm group need to further study CAUI-4 chip to chip application

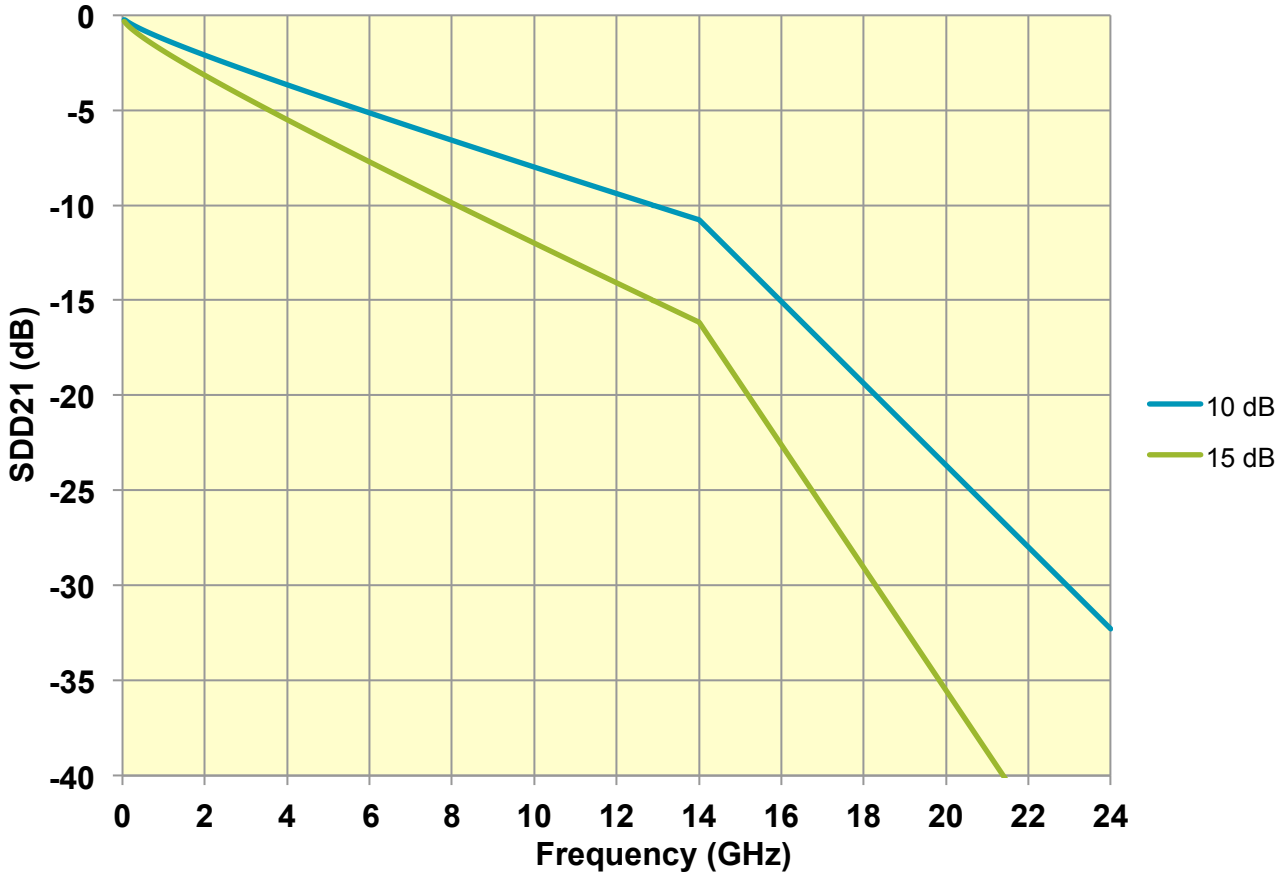


Increasing CAUI-4 Chip to Chip Reach

- Parameters that can increases CAUI-4 chip to chip reach
- Transmitter parameters and exact parameter that can be improved is dependent if this is large ASIC or PHY
  - Rise/fall time – can be made as fast as the min rise/fall time
  - Jitter - could lowered by ~0.1 UI
  - Amplitude - min value can be increased up to 900 mV
  - Return loss – no change
- Channel parameters
  - ILD – template to trade off loss vs ILD
  - ICN – template to trade off loss vs ICN
  - Loss a1 coefficient – needs to be control and only an issue with fat traces on low loss material or super low loss PTFE material
  - Return loss – no change
- Receiver parameters
  - CTLE gain 1-9 dB – no change
  - Sensitivity – to be studied if it needs to improved from 100 mV
  - Return loss – no change

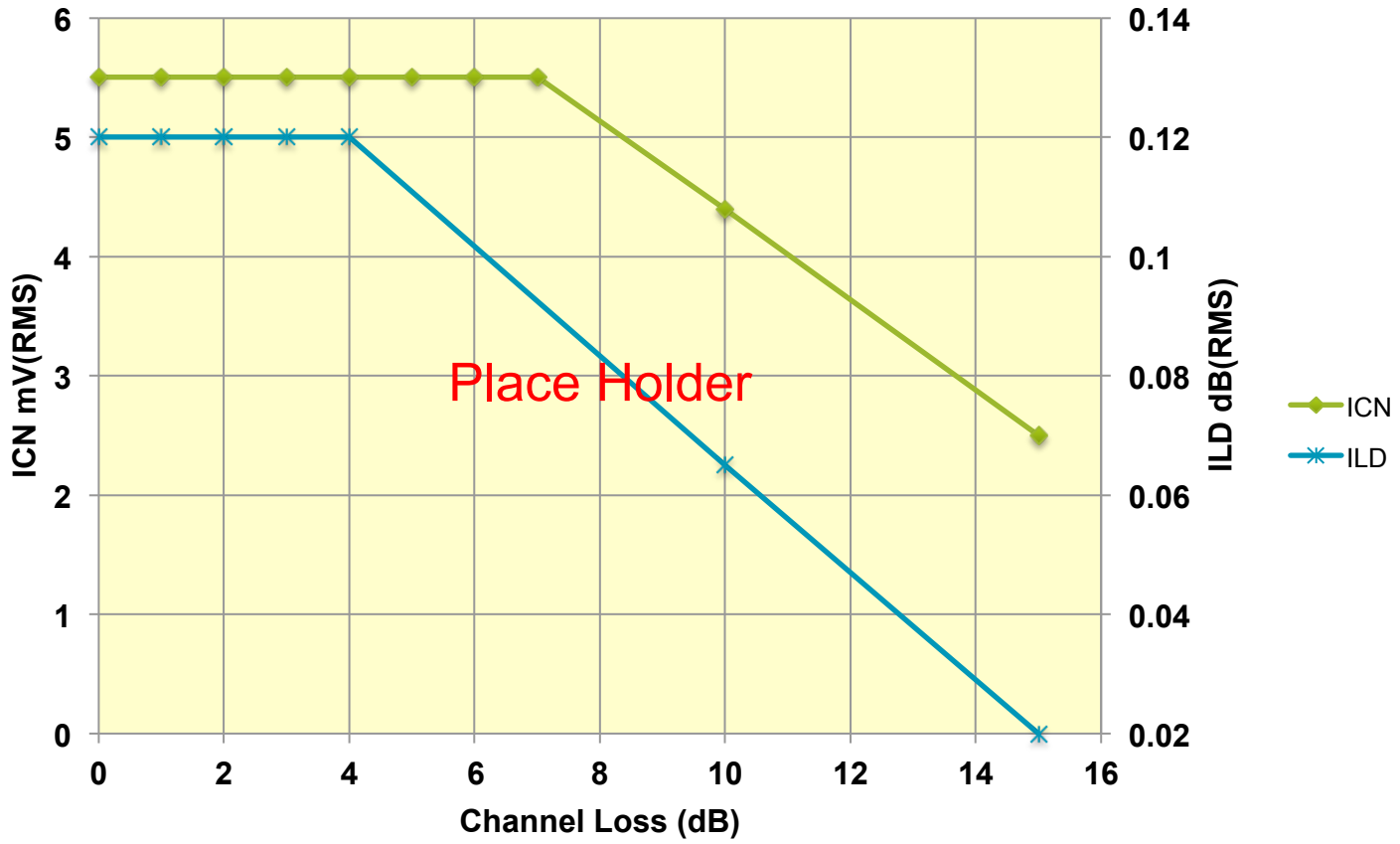
CAUI-4 Chip to Chip Informative Channel

- CAUI-4 chip to chip loss budget
  - Assuming all worst case parameters loss budget is 10 dB
  - By improving some of the transmitter parameters and operating the link where naturally has lower ICN/ILD the loss budget can be 15 dB



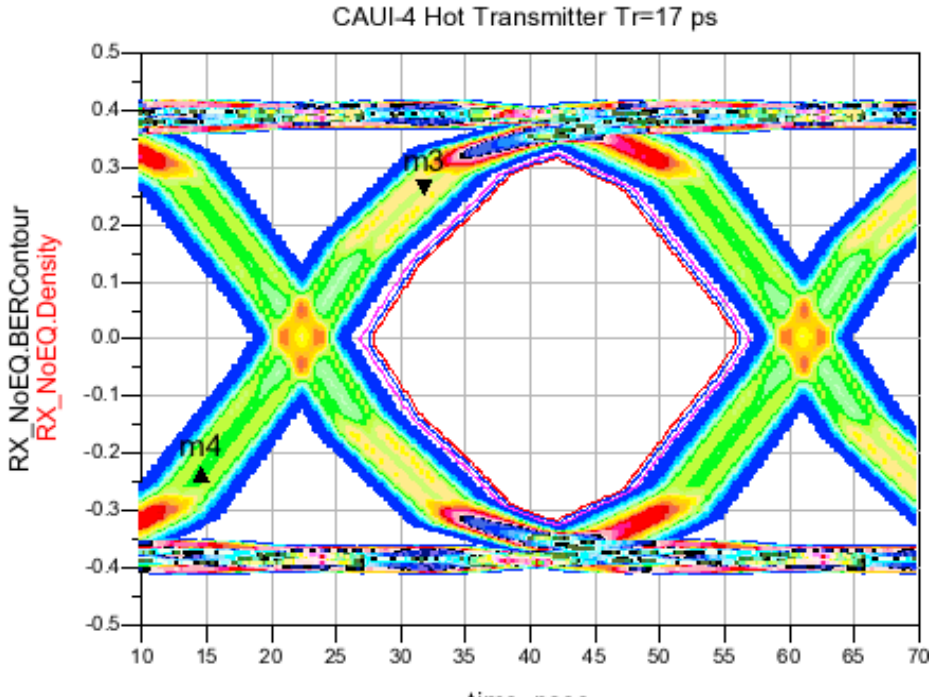
ILD and ICN Template

- ILD and ICN template are compatible at 10 dB with QSFP28/ CFP2 type channels



CAUI-4 Driver

- Define Hot driver with standard jitter but 800 mV output
  - Tr=17 ps TJ=0.28 UI@1E-15
- Define Fast-low jitter with 600 mV output
  - Tr=13ps TJ=0.18 UI@1E-15



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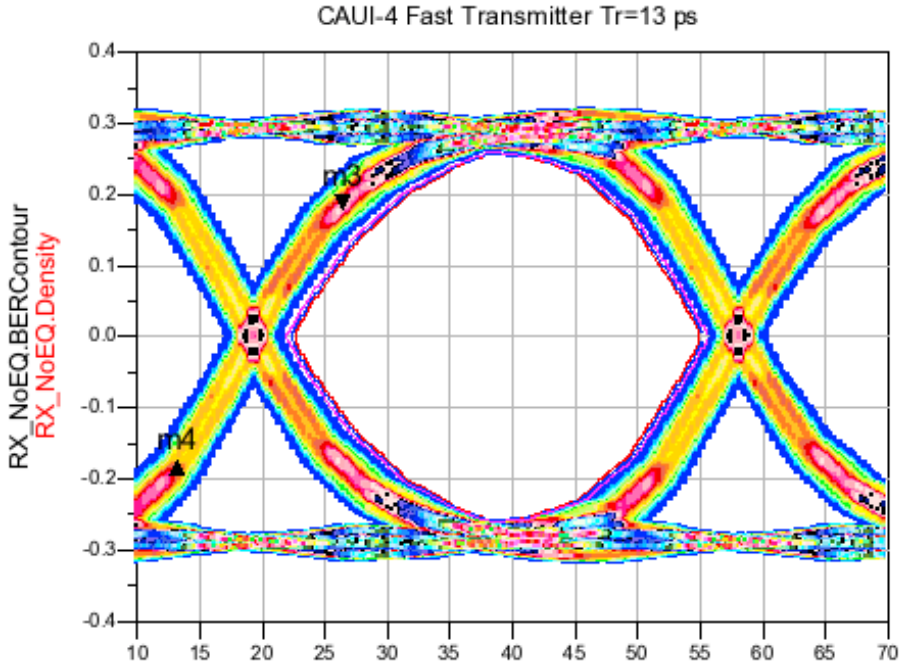

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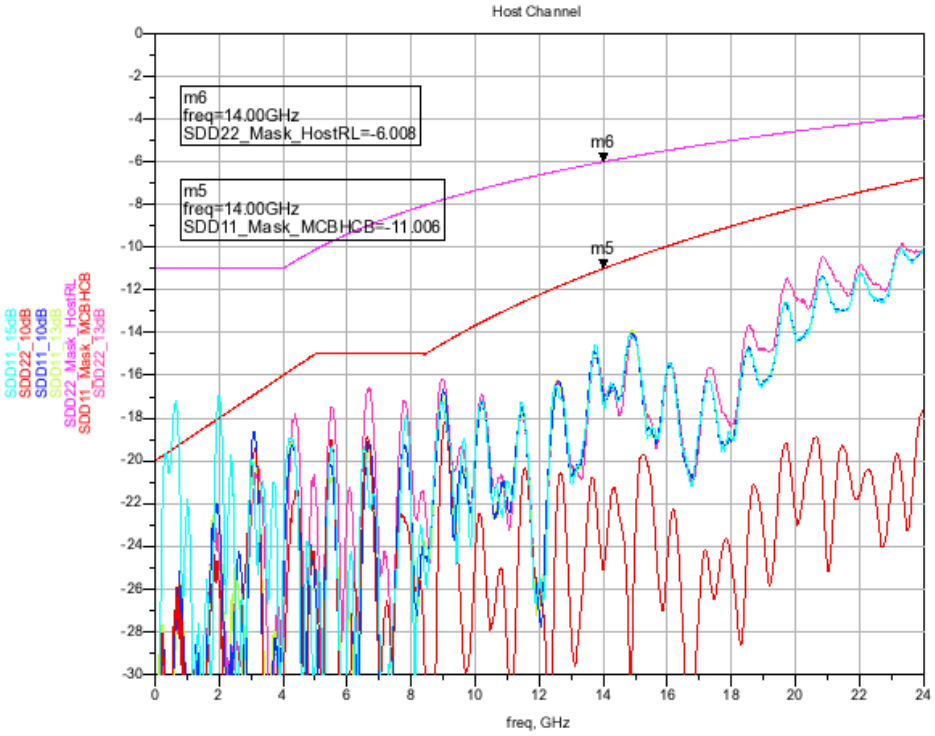
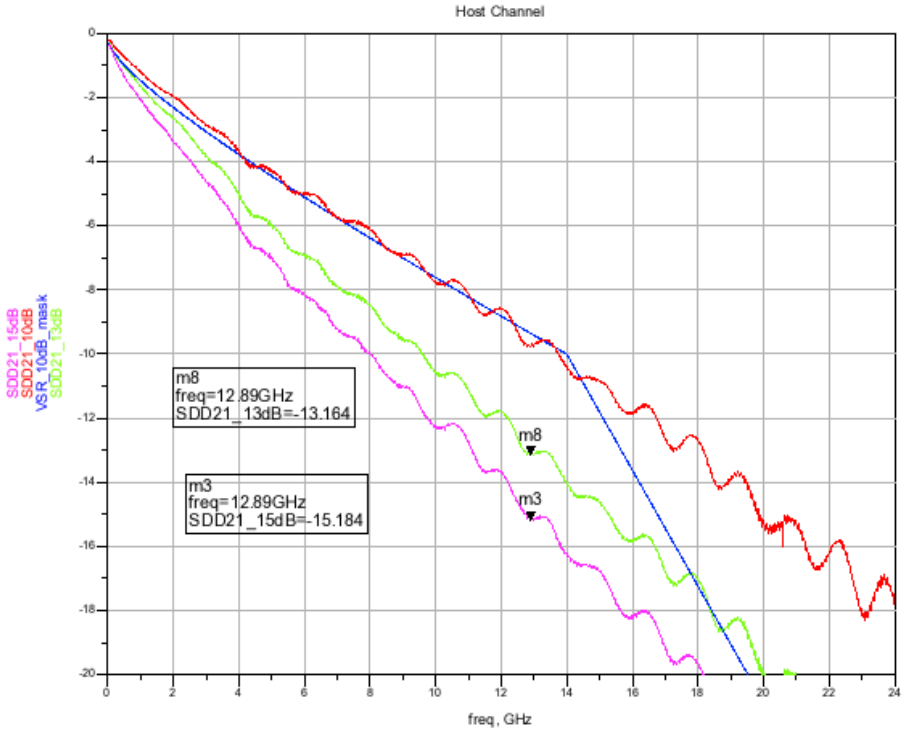
FR4 Channel Response

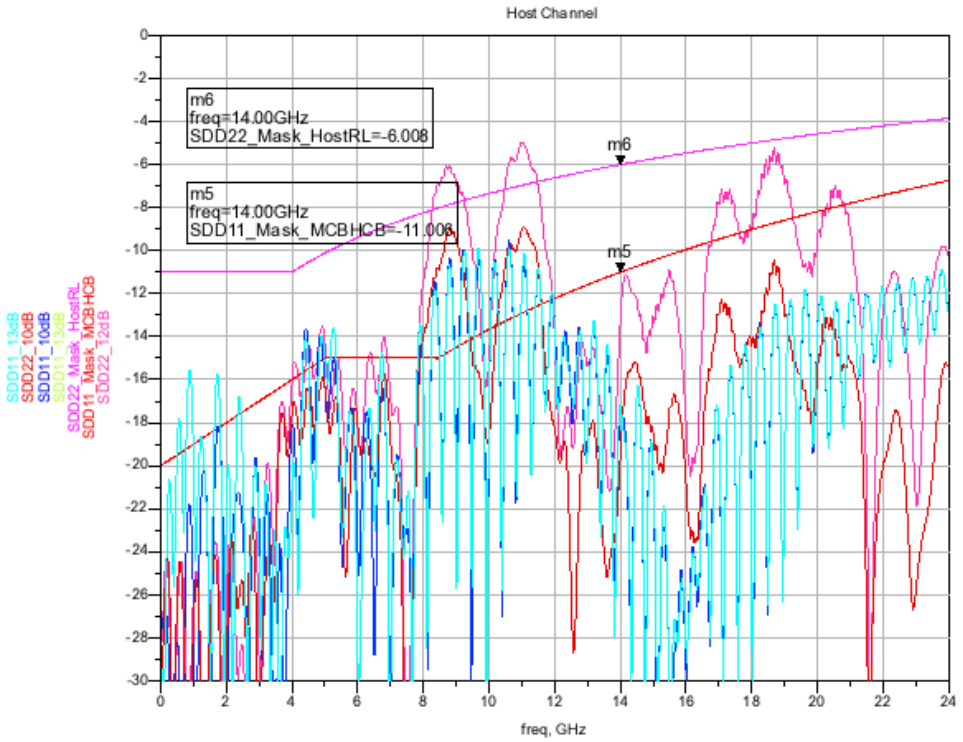
- Channels are
  - 5” FR4 Channel with two long (80 mils) vias and 2 12 mils stub
  - 5” FR4 + 3” Meg6 Channel
  - 5” FR4 + 5” Meg 6 Channel

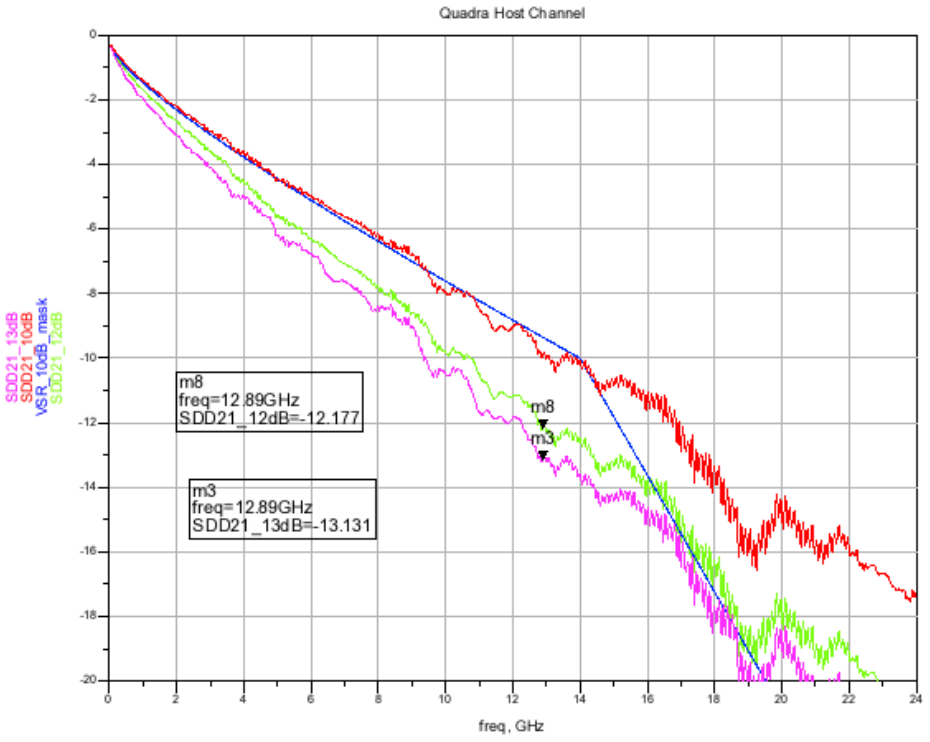




TE 7” Quadra Channel Response

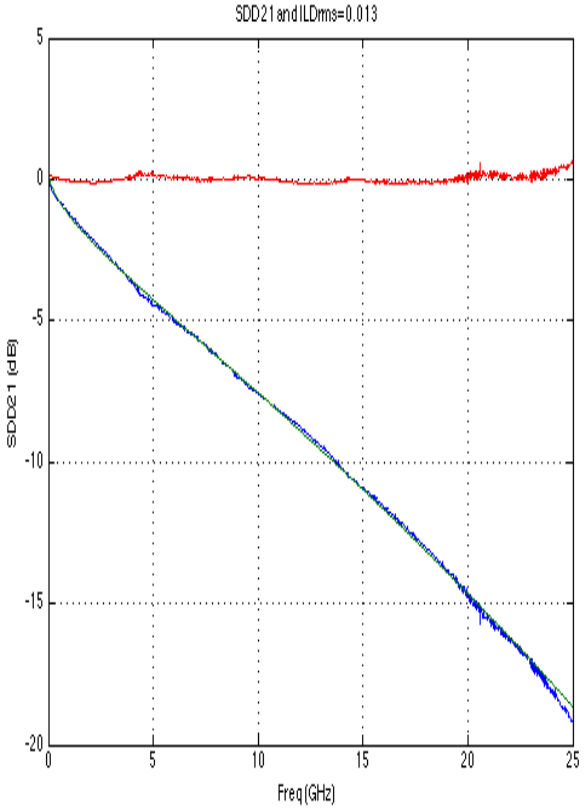
- Channels are
  - TE Quadra channel with 10 dB loss
  - TE 7” Quadra + 1.25” plug board+ 2” Meg6 Channel
  - TE 7” Quadra + 1.25” plug board + 2” FR4 Channel

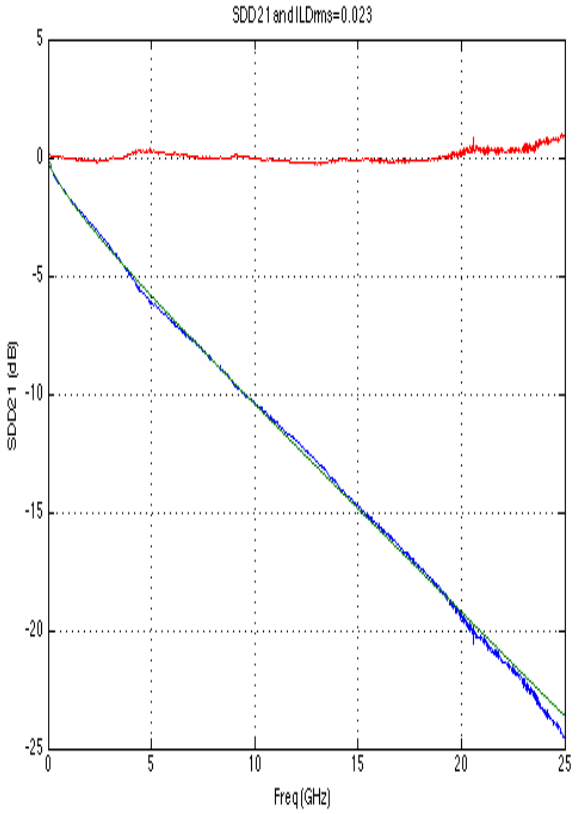


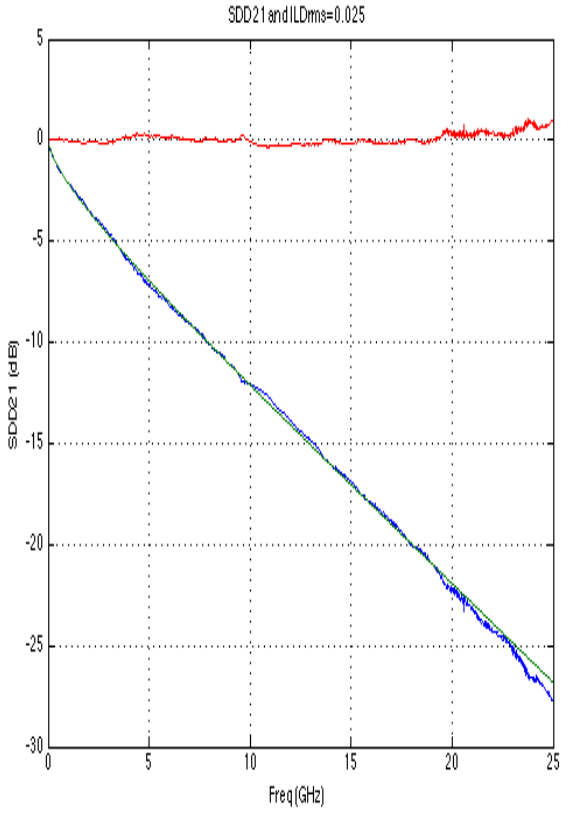


FR4 Channel ILD and Fit

- 10 dB channel has ILDrms=0.013 and a1/a0=0.23
- 13 dB channel has ILDrms=0.023 and a1/a0=0.59
- 15 dB channel has ILDrms=0.025 and a1/a0=0.46

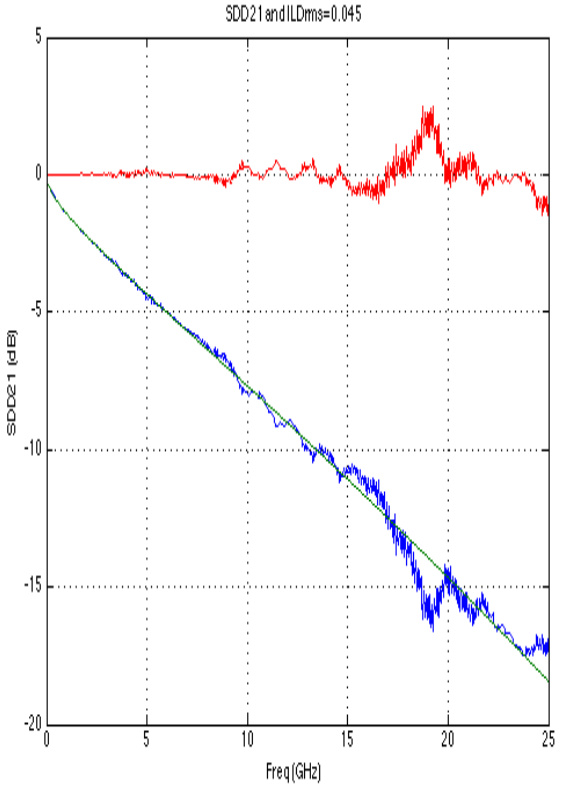


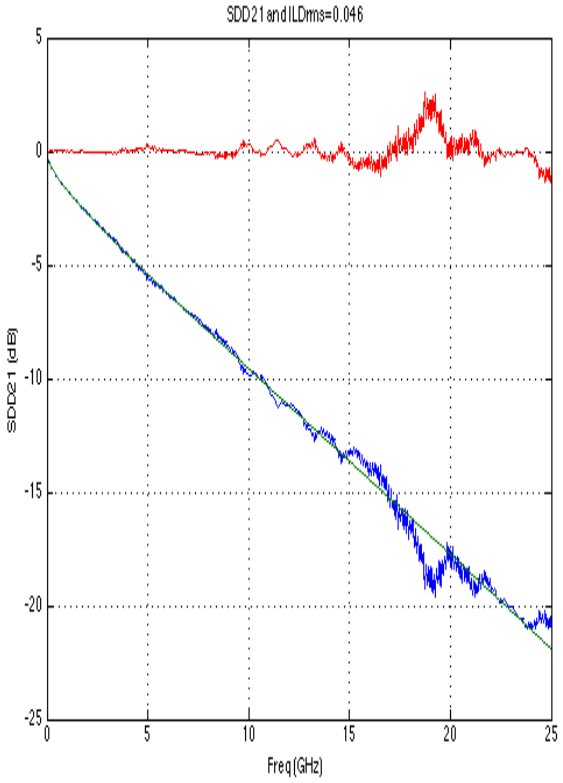


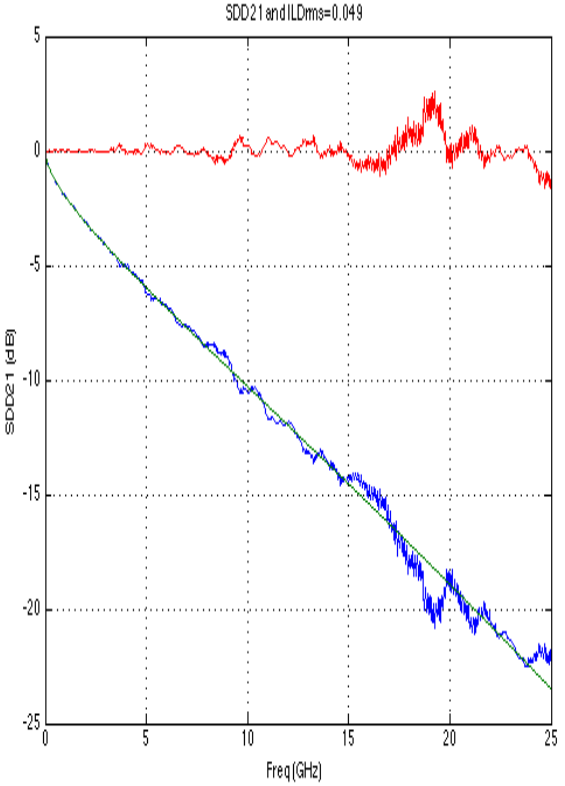


TE Quadra Channel ILD and Fit

- 10 dB channel has ILDrms=0.045 and a1/a0=0.45
- 12 dB channel has ILDrms=0.046 and a1/a0=0.62
- 13 dB channel has ILDrms=0.049 and a1/a0=0.34

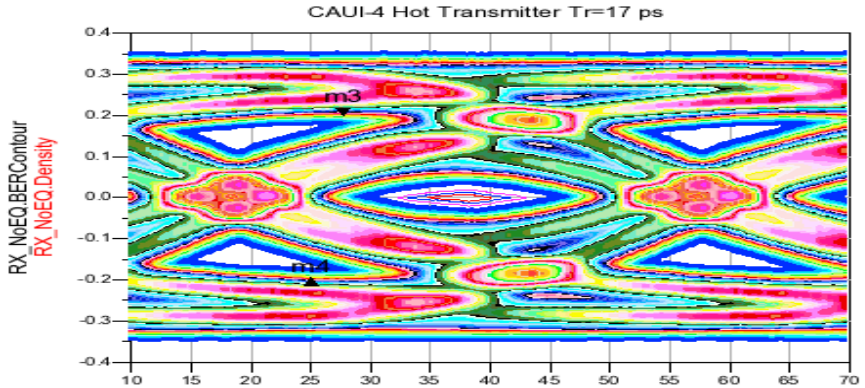






10 dB Channel with Hot and Fast Transmitter

- Optimum TX de-emphasis 1 dB for both TX



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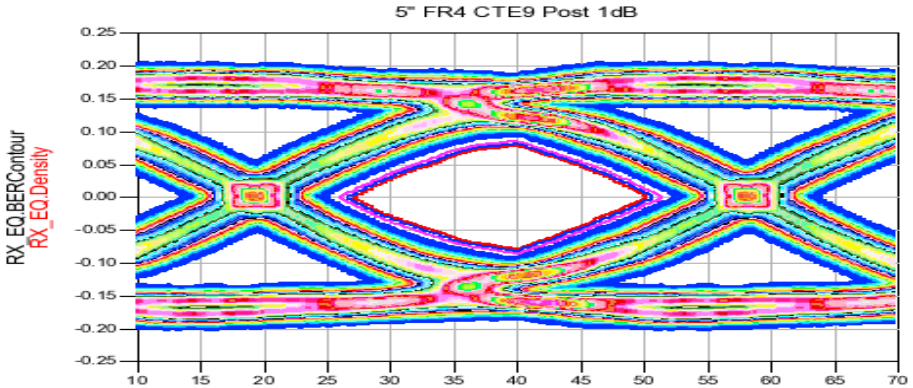

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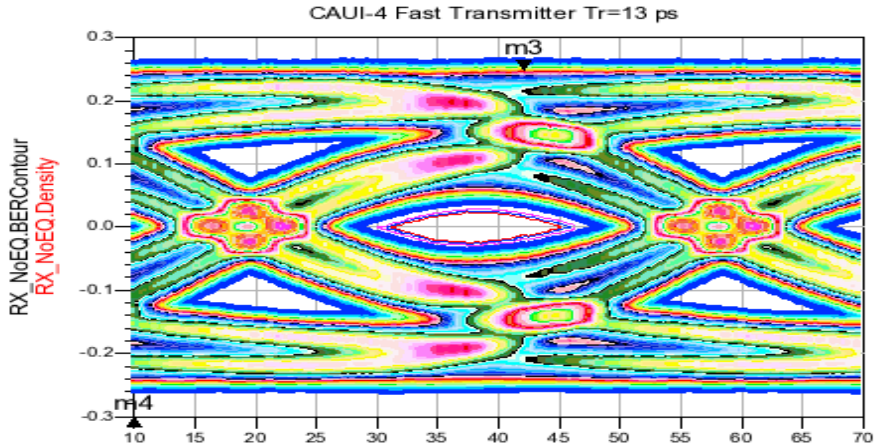

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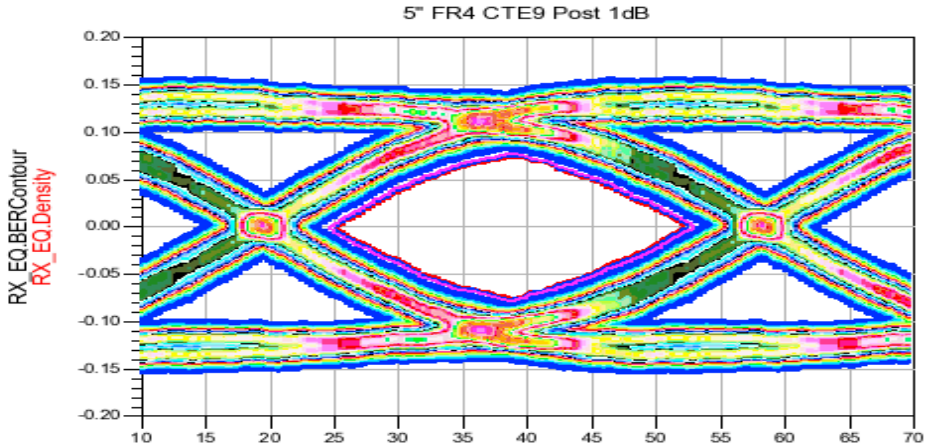

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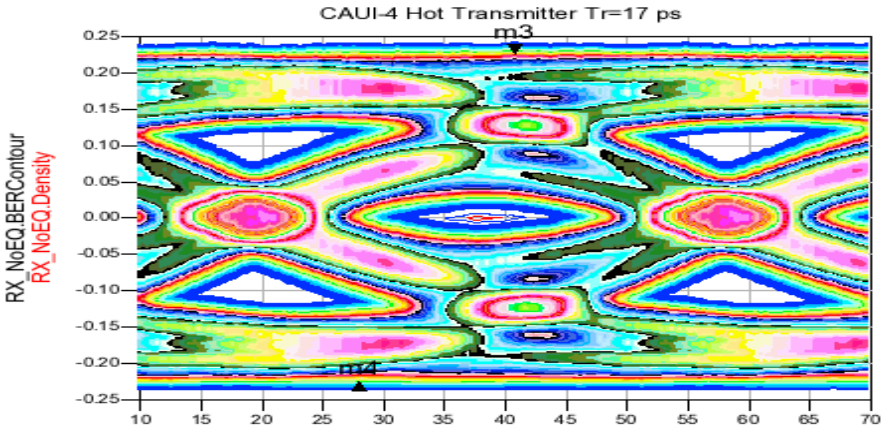
13 dB Channel with Hot and Fast Transmitter

- Optimum TX de-emphasis 4 dB for hot and 3 dB for fast TX



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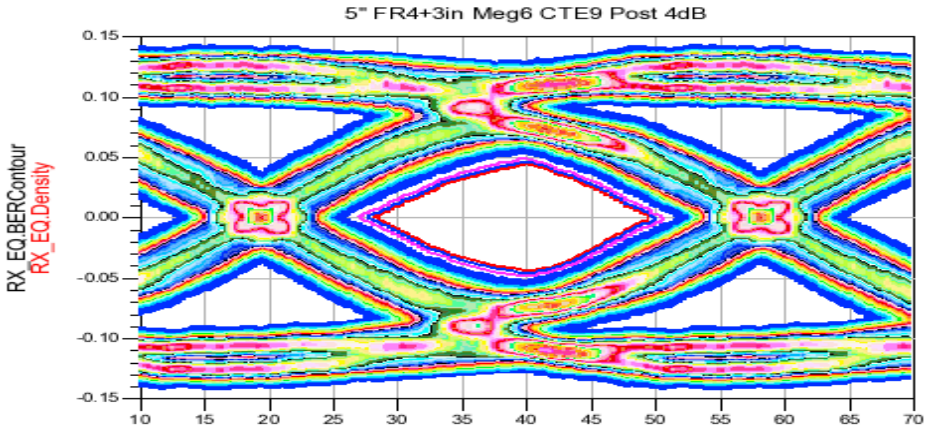

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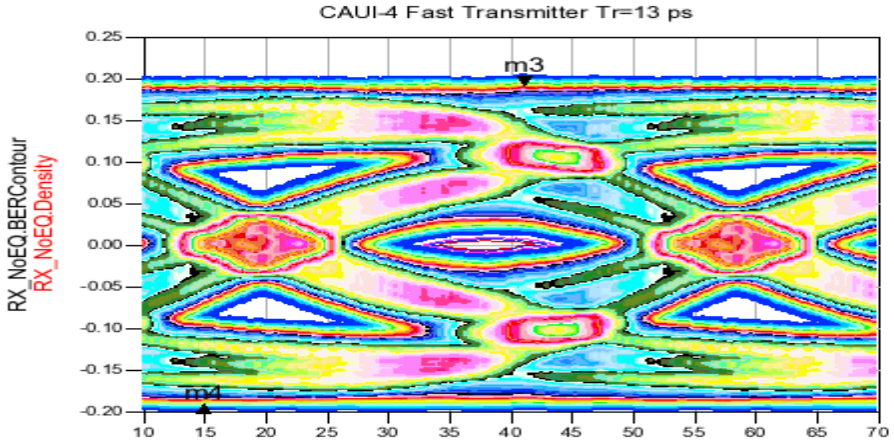

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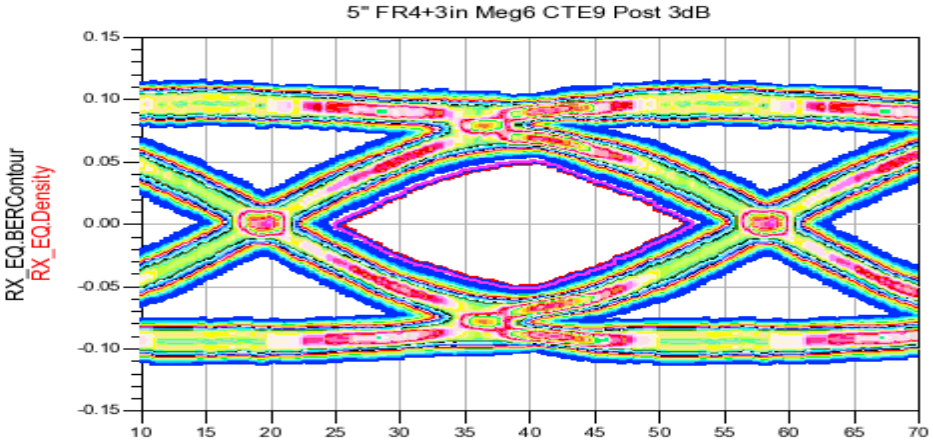

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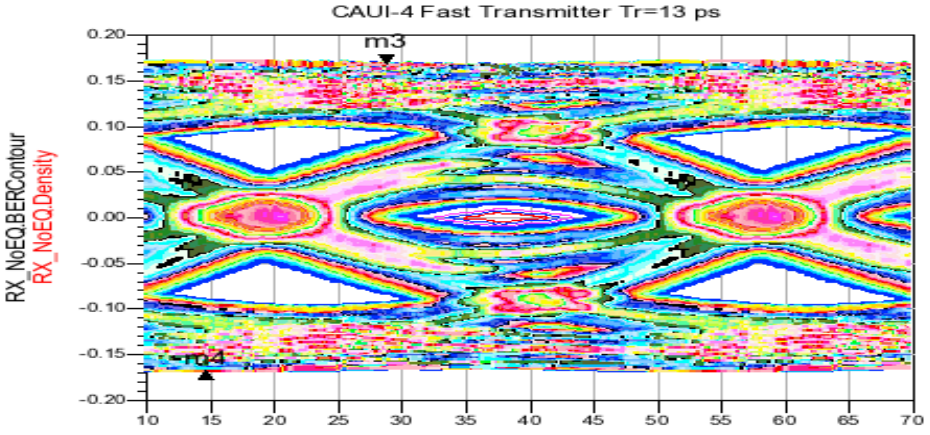
15 dB Channel with Hot and Fast Transmitter

- Optimum TX de-emphasis 6 dB for hot and 6 dB for fast TX



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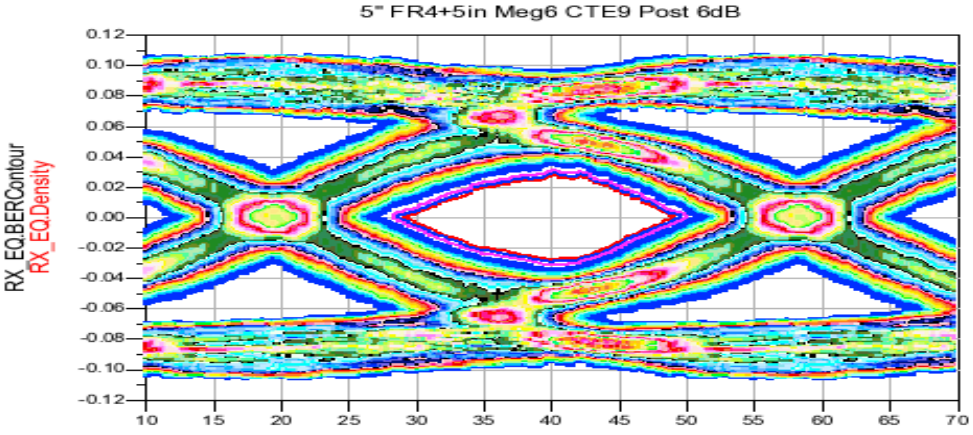

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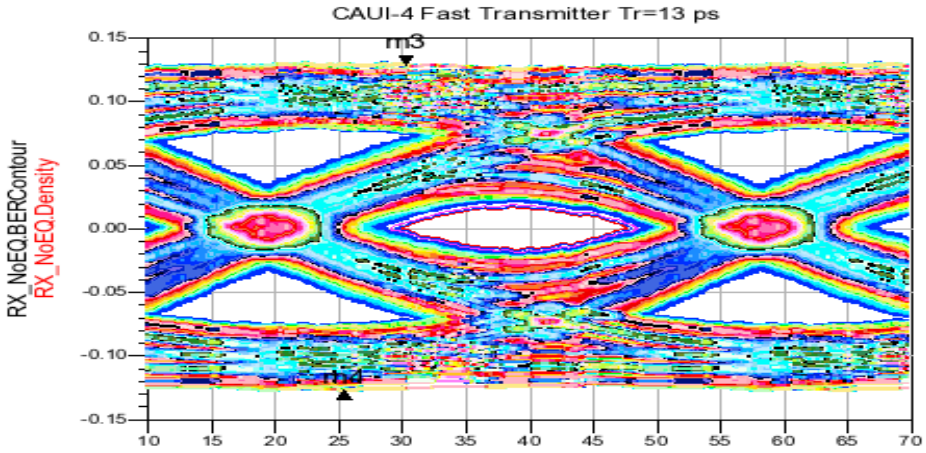

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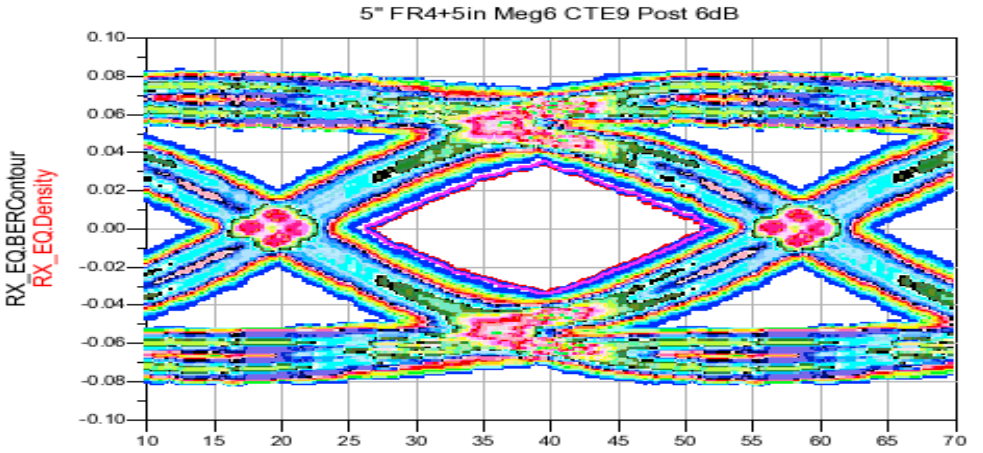

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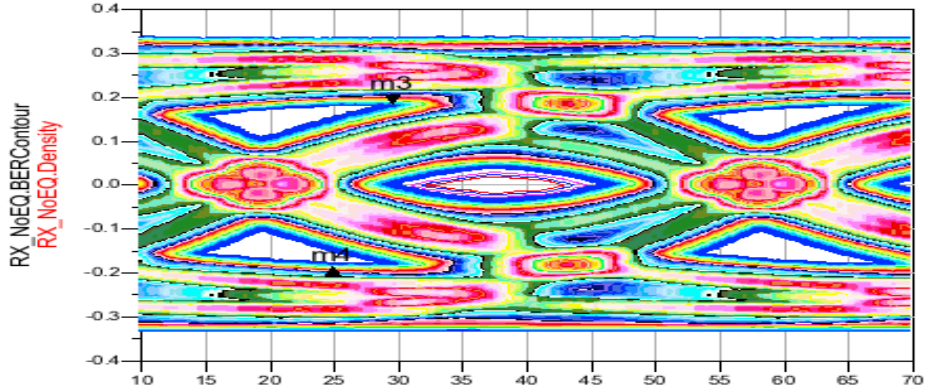
8.25” Quadra Channel with Hot and Fast Transmitter

- Optimum TX de-emphasis 6 dB for hot and 6 dB for fast TX

CAUI-4 Hot Transmitter Tr=16 ps



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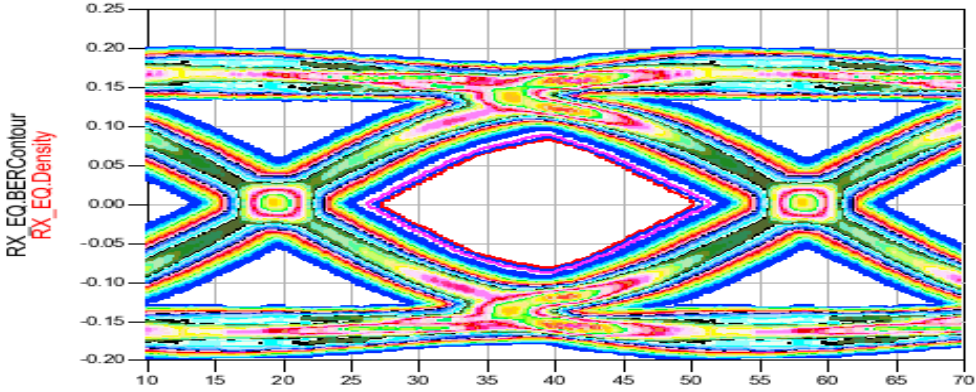
TE Quttro 8.25" CTE9 Post 1dB



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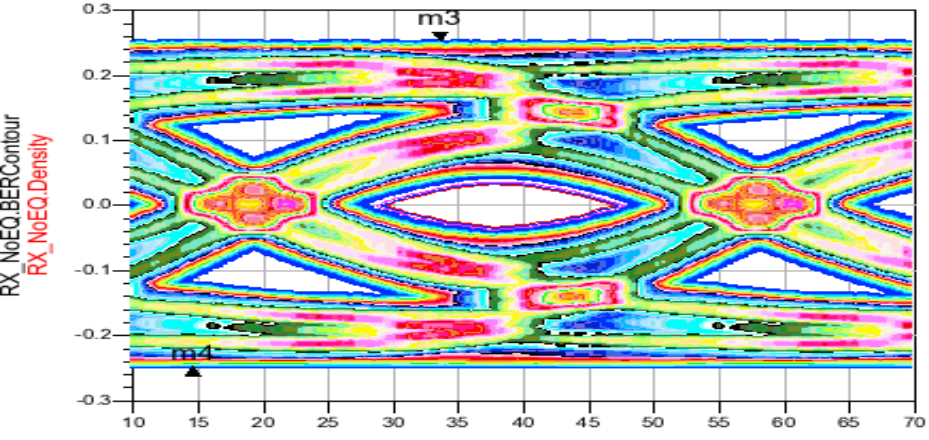
CAUI-4 Fast Transmitter Tr=13 ps



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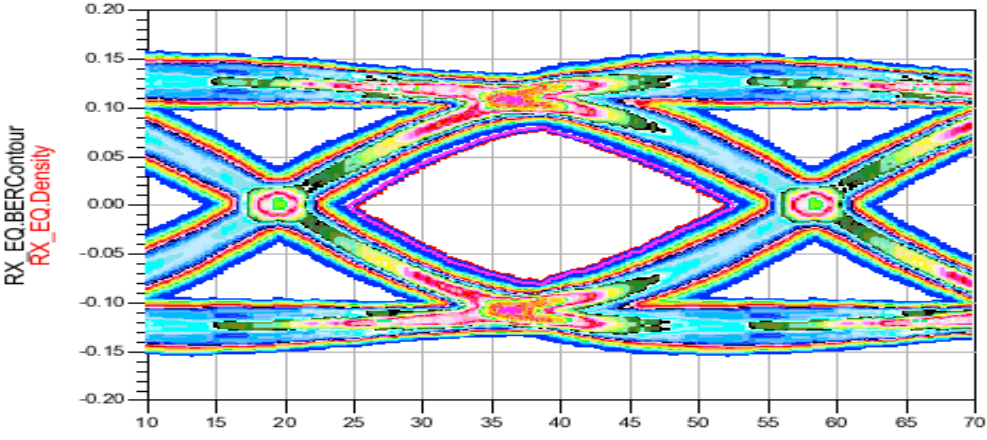
TE Quttro 8.25" CTE9 Post 1dB



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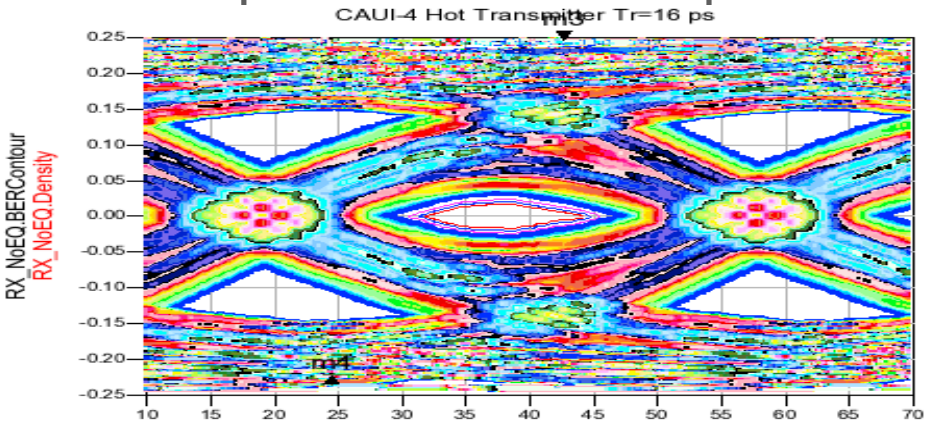
8.25” Quadra Channel + 2dB with Hot and Fast Transmitter

- Optimum TX de-emphasis 6 dB for hot and 6 dB for fast TX



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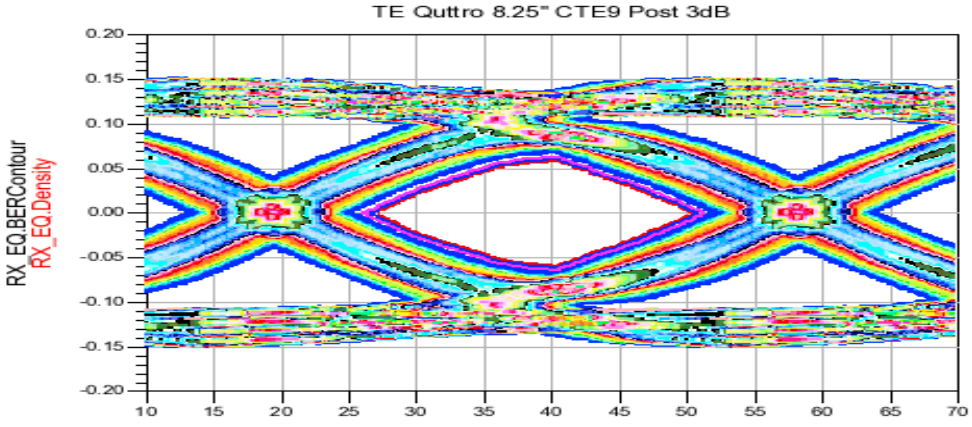

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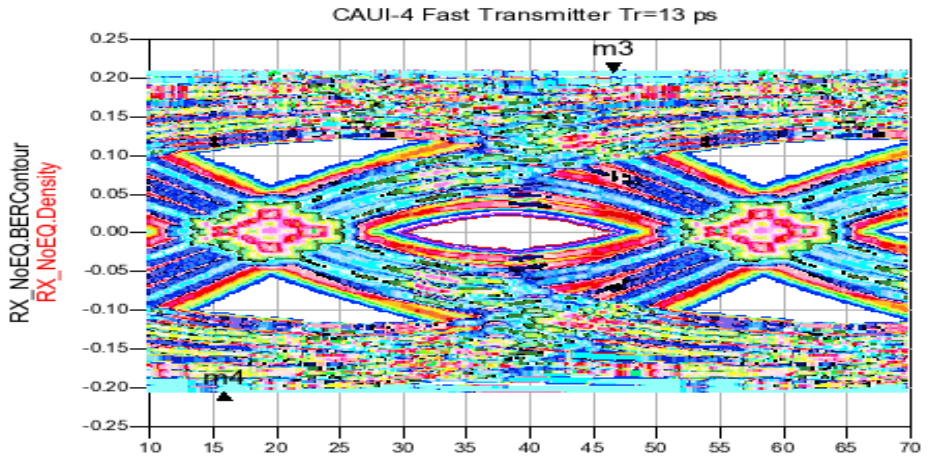

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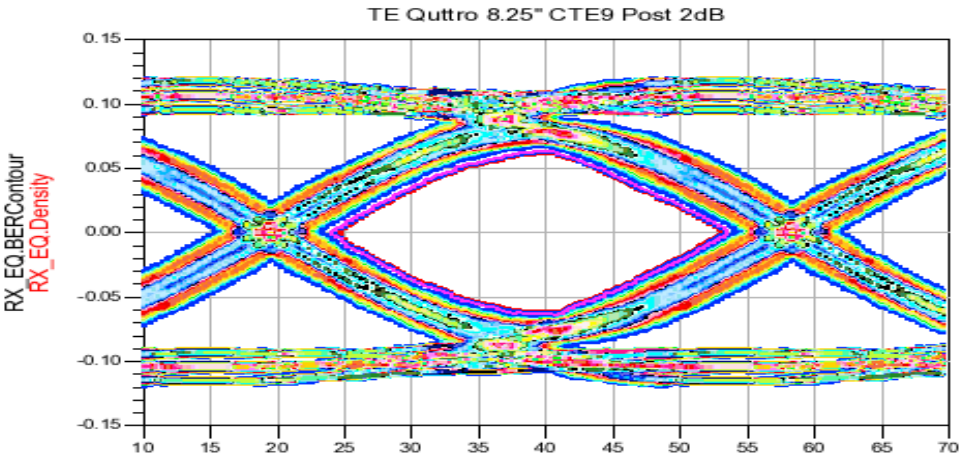

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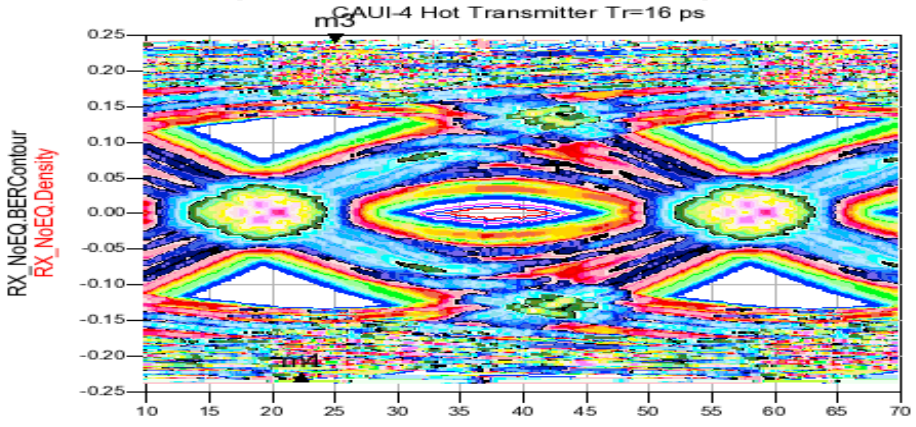
8.25” Quadra Channel + 3dB with Hot and Fast Transmitter

- Optimum TX de-emphasis 6 dB for hot and 6 dB for fast TX



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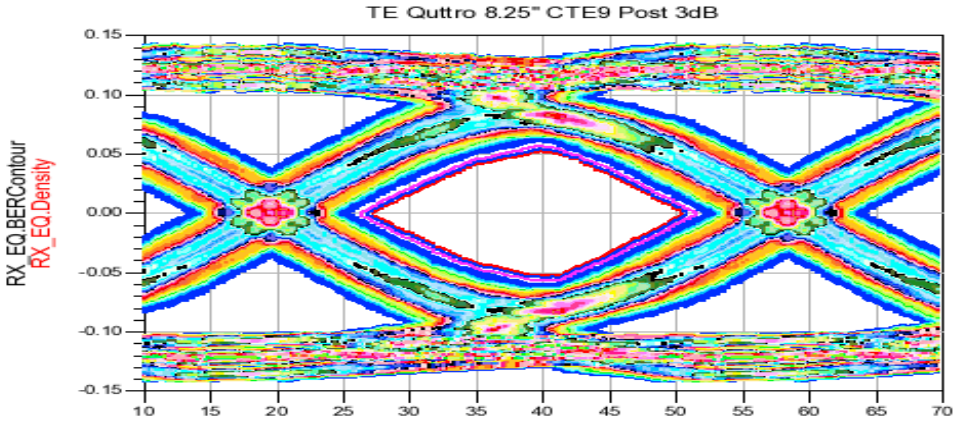

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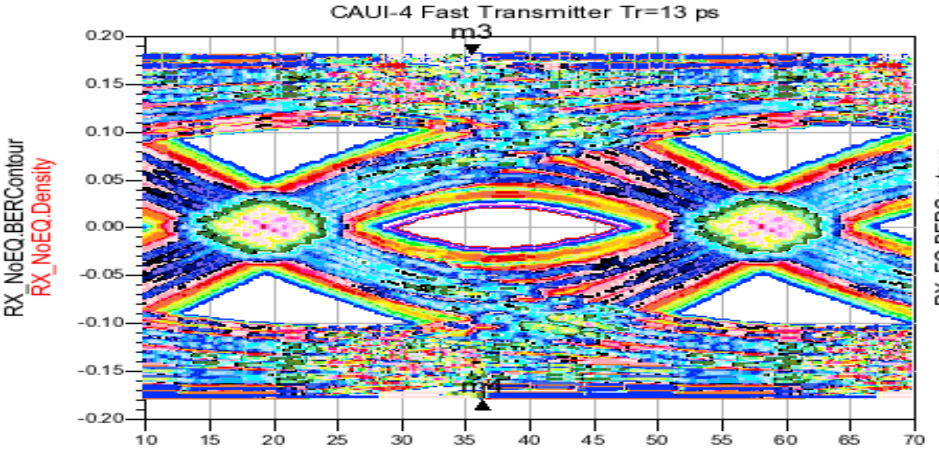

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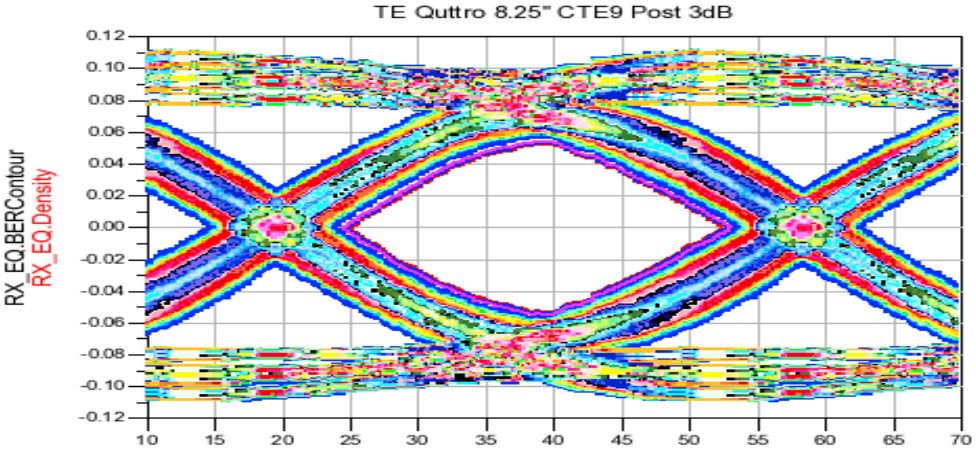
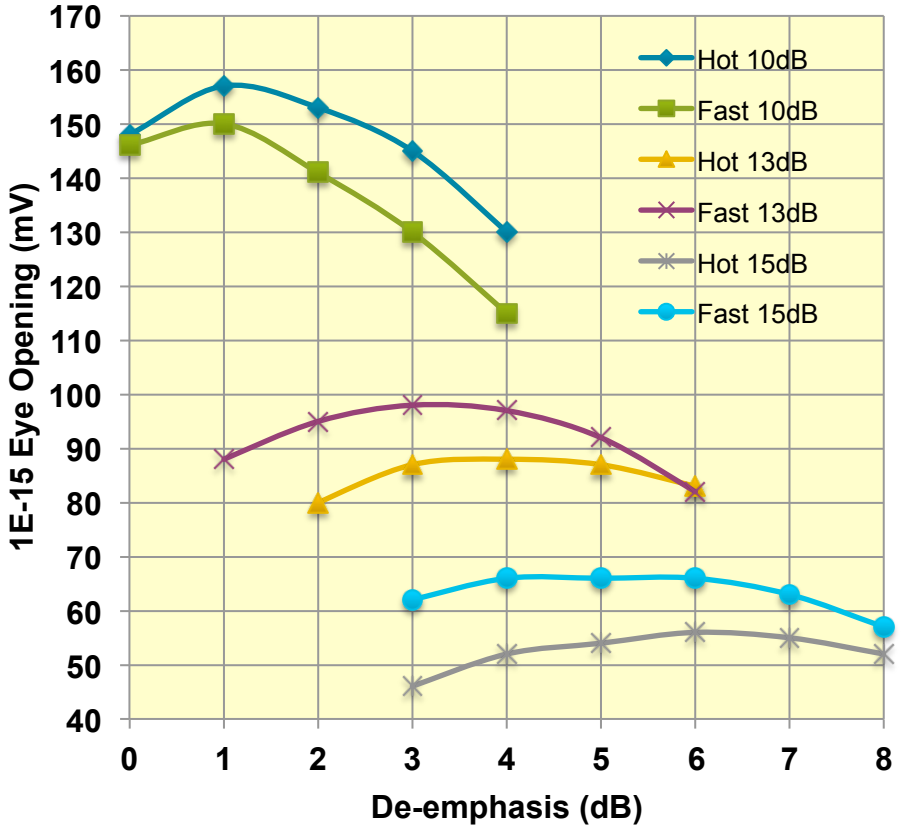
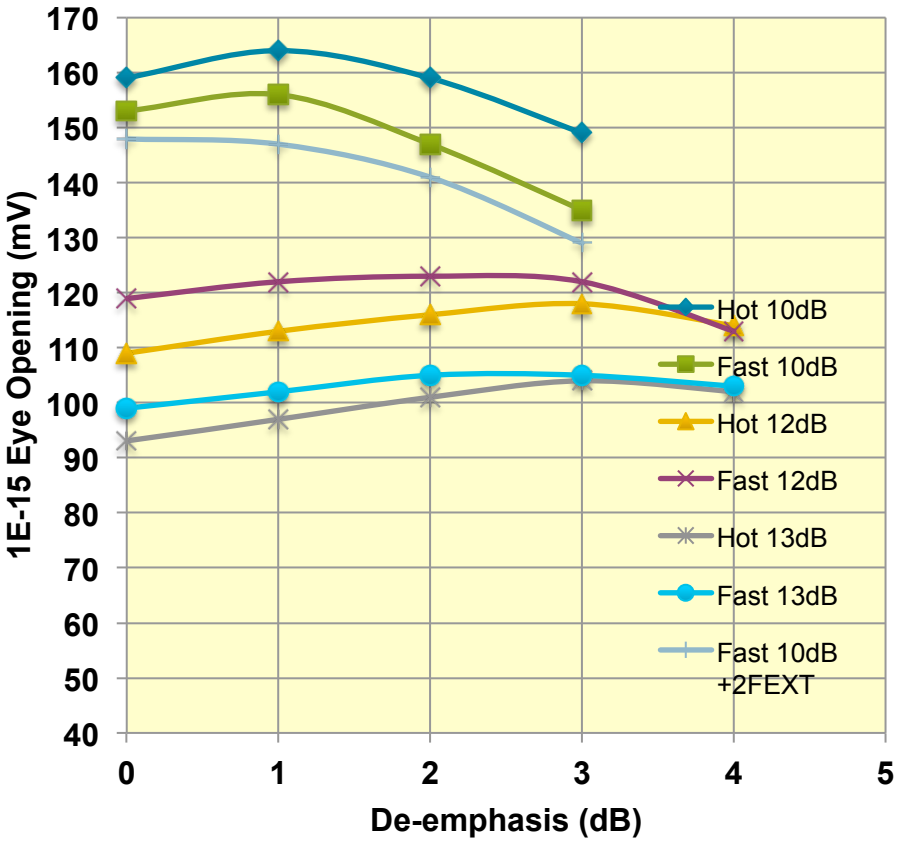


index	..._EQ.WidthAtBER)	...EQ.HeightAtBER)
0.000	2.773E-11	0.105

Summary of Eye Opening

- Hot driver and fast driver have nearly similar far end performance!
- TE Quadra 10 dB channel has slighlty better performance compare to channel with two long vias (~80 mils) and two short stub (~12 mils)
- Considering only 2 FEXT TE 10 dB channel ~ 6% VEC penalty





Summary

- For CAUI-4 chip to chip two channels were investigated
  - FR4 channel with deep vias and short stubs
  - TE Quadra based channel
- Result shown here is far end eye excluding DC block and receiver package and parasitic as observed on the scope with reference CTLE with gain of 9 dB
  - The equalized eye opening at the actual slicer typically ~25% less due to the RX package, ESD, and DC blocks
  - Hot transmitter has comparable performance to fast transmitter having 25% less amplitude
  - As the channel loss increases >12 dB fast TX start performing better
- CAUI-4 chip to chip can support 13 dB assuming TX FFE and RX CTLE having fast/low jitter or 800 mV driver
  - Current CAUI-4 chip to module TP1a limit is 100 mV
  - 13 dB channel will have TP5 eye opening of 90 mV with improved driver
  - 15 dB channel will have TP5 eye opening of just 60 mV with improved driver

Thank You