CAUI-4 Chip – Chip Spec Discussion

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Ryan Latchman <ryan.latchman@mindspeed.com>

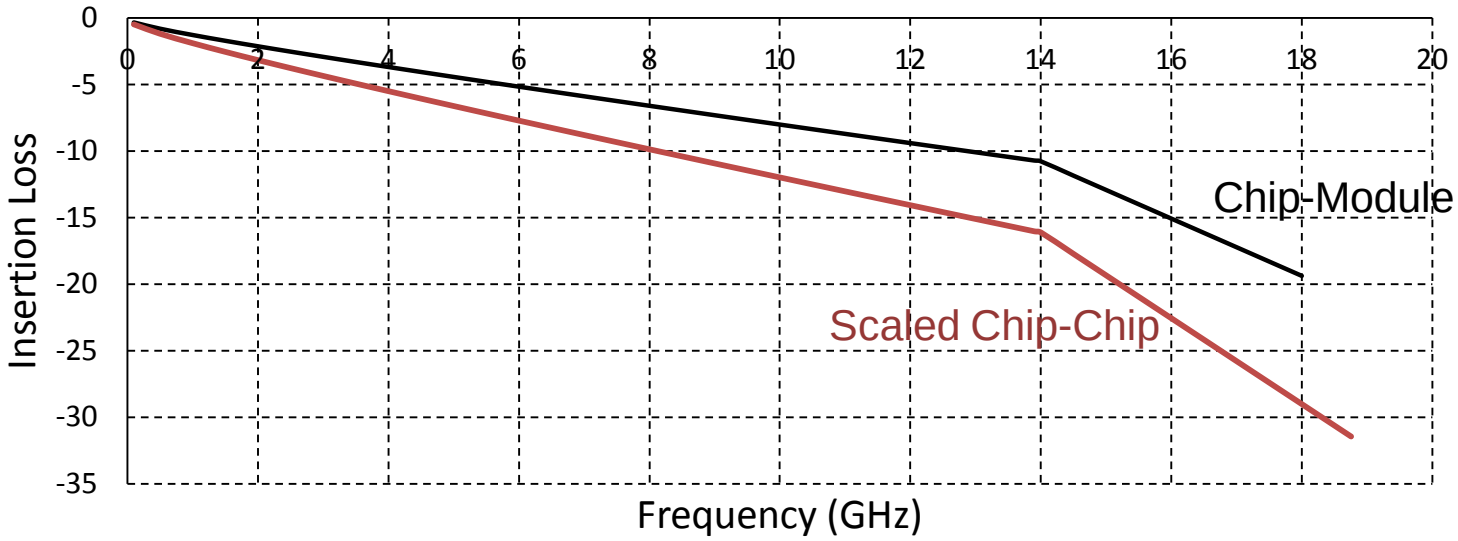
Agenda

- Patent Policy:
  - The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-Chip Discussion
  - Current Status with a view towards baseline
- Ghiasi_01_0113_caui4

Current Status

- Chip-Chip
  - MTTFPA Resolution:
    - If loss is kept to ~15dB, MTTFPA can be avoided without use of FEC
    - Preliminary analysis shows this can still meet ~25cm application targets similar to Annex 83A
  - Need to make progress on:
    - Channel Definition
      - Scale chip-module or bj or OIF
    - Transmitter Requirements
      - Output Jitter and de-emphasis settings etc
    - Receiver Requirements
      - Interference tolerance

Channel Loss



- Other channel parameters may include:
  - ILD, ICN, returnloss…
  - COM (?)

CAUI-4 Chip-Chip transmitter considerations

	KR4 (D1.3, TP2)	MR	CAUI-4 Chip-Chip Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Differential peak-to-peak output voltage (max) with Tx disabled	30mV		30mVppd
Common Mode Voltage (max)	1.9V	1.7V	1.9V
Common Mode Voltage (min)	0V	-0.1V	0V
Differential output return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2)), 0.05<=f<=13GHz
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=13GHz	-6dB , f<10GHz -4dB, 10G<f<25.78125GHz	RL(f)>= 6dB, 0.05<=f<=13GHz
Common-mode AC output voltage (max,rms)	12mV	12mV	12mV
Amplitude peak-to-peak (max)	1200mV	1200mV	1200mV
Amplitude peak-to-peak (min)		800mV	800mV
Transition Time (20%-80%, min, no EQ)	8ps	8ps	8ps

CAUI-4 Chip-Chip transmitter considerations

	KR4 (D1.3, TP2)	MR	CAUI-4 Chip-Chip Potential
Transmitter steady state voltage	0.4 (min) - 0.6V (max)		TBD
Linear fit pulse peak (min)	0.8 x Transmitter steady state voltage		TBD
Transmitted wave form Max RMS normalized error (linear fit), “e” abs coefficient step size (min.) abs coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 0.037 0.0083 0.05 1.54 4	C-1: -20 to 0 C1: -25 to 0 C0: 40 to 100 Step size: 1.25 to 5	TBD
Far end transmit output noise (max)	2mV (low loss channel) 1mV (high loss channel)		TBD
Output jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	TUUGJ = 0.15UIpp T_UBHPJ = 0.15UIpp T_DCD = 0.035UIpp TJ = 0.28UIpp	TBD
Differential Resistance		80 ohms min, 100ohms typ, 120 ohms max	TBD

CAUI-4 Chip-Chip Receiver considerations

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Differential Input Return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2)), 0.05<=f<=13GHz
Common mode input return loss (min)	RL(f) >=6dB, 0.05<=f<=13GHz	6dB , f<10GHz -4dB, 10G<f<25.78125GHz	RL(f) >=6dB, 0.05<=f<=13GHz
Differential to common-mode return loss (min)	TBD		TBD
Input Differential Voltage (max)		1200	1200mV
Differential Impedance		80ohms min, 100ohms typical, 120ohms max	TBD
Input Impedance Mismatch (max)		10%	TBD
Input common mode voltage		-200mV (min), 1800mV (max)	TBD

Receiver Interference Tolerance

Parameter	Test 1 values
Maximum BER*	10^{-12}
Channel Insertion Loss at 12.89GHz	~15dB
Applied peak-to-peak sinusoidal jitter	TBD
Applied peak-to-peak random jitter	TBD
Applied even-odd jitter	TBD
Applied RMS broadband noise	TBD

* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Compliance points

- **See 93.8.2.1 Receiver test fixture from 802.3bj**
- **See 93.8.1.1 Transmitter test fixture from 802.3bj**

Minutes

- Discussion around use of COM and VSR methodology to specify channel
  - Annex 93A will be in the IEEE document
  - Chip-module methodology will also be available for reuse
  - Question on comparing COM with ADS/SiSoft
  - Consider using OIF SR spec as well
- Transmitter spec
  - Far end eye diagram
    - But then channel needs to be defined along with CTLE
  - Eye at TP0a
    - Amplitude and eye width
- Reviewed ghiasi_01_0113_caui4
  - Question on if Transmitter can be tightened for FPGA/ASICs