

# CAUI4 chip to chip by leveraging 100GBASE\_KR4

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## Why leverage 100GBASE\_KR4?

- Focus : 100GBASE\_KR4 was developed by a task force which focused entirely on Copper, CAUI4 is an auxiliary function in its task force
- Lead: 100GBASE\_KR4 is about 1 year further along in its schedule than CAUI4
- Improvement: 100GBASE\_KR4 Tx, channel, and Rx are specified a connected way and as a result should be more meaningful and accurate than previous methods

What is so good about 100GBASE\_KR4

- It closes: COM ties together a normative Tx spec, a normative channel spec, and a normative Rx spec in such a way that interoperability is guaranteed between compliant components with a minimum of performance being left on the table.
- Usable tests: all measurements made on components of the system are as straightforward as possible and provide useful, understandable component information, although sometimes this requires processing, which is specified .

## What to do

1. Transmitter: replace Annex 83D.3.1 with Clause 93.8.1 except:
  1. In Table 93-4, delete references to coefficient step size and range and replace with min and max values for Pre-cursor and Post-cursor values at a number (3?) of discrete settings.
  2. In Clause 93.8.1.6.3 Coefficient initialization, Change description of initialize state to description of discrete settings.
  3. Deleted Clause 93.8.1.6.4 Coefficient step size and Clause 93.8.1.6.5 Coefficient range.
  4. A Clause 93 transmitter with the necessary control to put it into the specified equalization settings will pass Annex 83D Tx specifications

## 2. Channel:

1. Delete Figure 83D–2—Chip-chip insertion loss budget at 12.89 GHz, equation 83D-1, and Figure 83D-3 CAUI-4 chip-chip channel insertion loss.
2. Update Table 83D-5 with latest values from Table 93-9 except Decision feedback equalizer (DFE) length and Target detector error ratio which are correct in Table 83D-5 for CAUI4.
3. Instead of specifying range and step size for precursor and postcursor taps, specify a number of allowed precursor-postcursor pairs values.

### 3. Receiver:

1. Replace 83D.3.2 with Clause 93.8.2, except numerous cases where current text is out of date or cases where references are clearly inappropriate to CAUI4, mostly in Clause 93.8.2 Receiver interference tolerance
2. Delete Table 93-7 and replace with the one below.

Receiver interference tolerance parameters

	Test 1		Test 2		Units
	Min	Max	Min	max	
Bit Error Ratio		$10^{-15}$	$10^{-15}$		--
Insertion loss at 12.89 GHz		8.0	15		dB
Coefficients of fitter insertion loss					
$a_0$	-0.9	0.9	-0.9	0.9	dB
$a_1$	0.0	1.6	0.0	3.0	dB/GHz <sup>1/2</sup>
$a_2$	0.0		0.0		dB/GHz
$a_4$	0.0		0.0		dB/GHz <sup>2</sup>
COM, including effects of broadband noise		3.0		3.0	dB

These proposed changes are based on draft P802d3bm-D1p0.pdf for the current CAUI4 spec and draft P802d3bj\_D2p1.pdf. When these drafts are updated, details of the proposal will have to be updated as well.

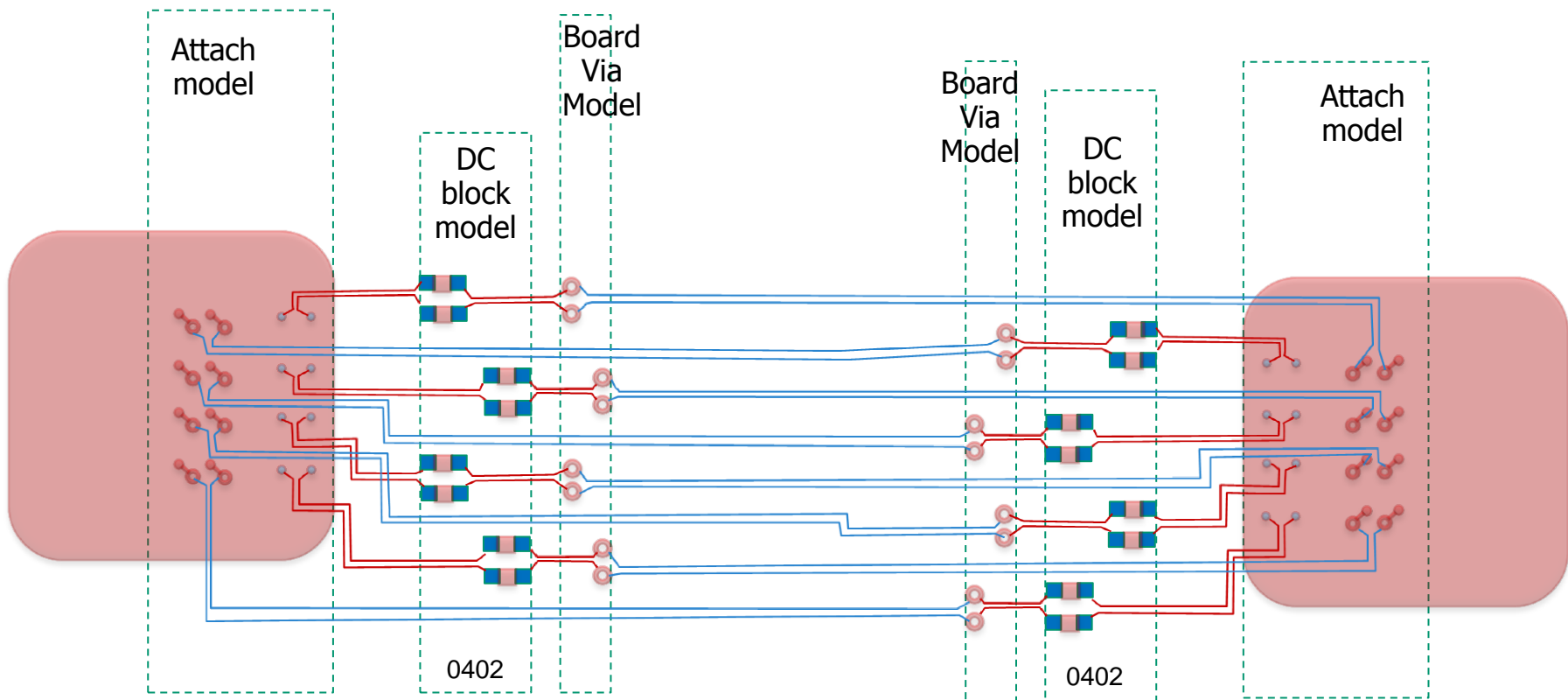
In general if this proposal is followed, it will be necessary to do something to keep CAUI4 in sync with 100GBASE\_KR4 as long as IEEE802.3bj remains active.

This proposal is intended to show how 100GBASE\_KR4 could be used to define CAUI4. There are a number of ways essentially the same specs can be created and editorial discretion can be used to modify the form the CAUI4 while still performing the intent of this proposal. Also a number of parameters are included, suggested, or have their existence implied by this proposal whose values may be defined or change at a later date.

Below we analyze some potential channels using the COM method and explain the value of this analysis.



# CAUI-4 Board Example

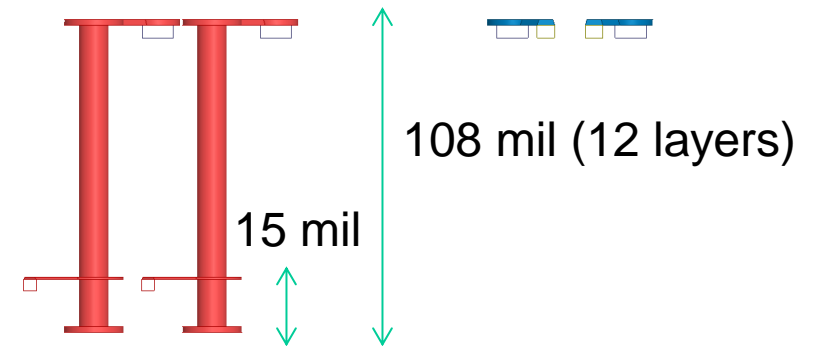
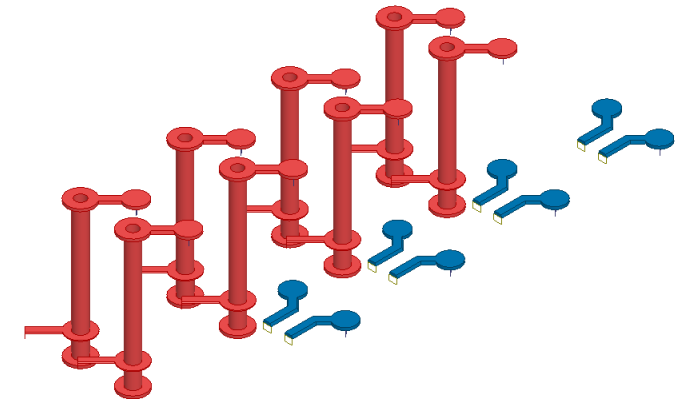
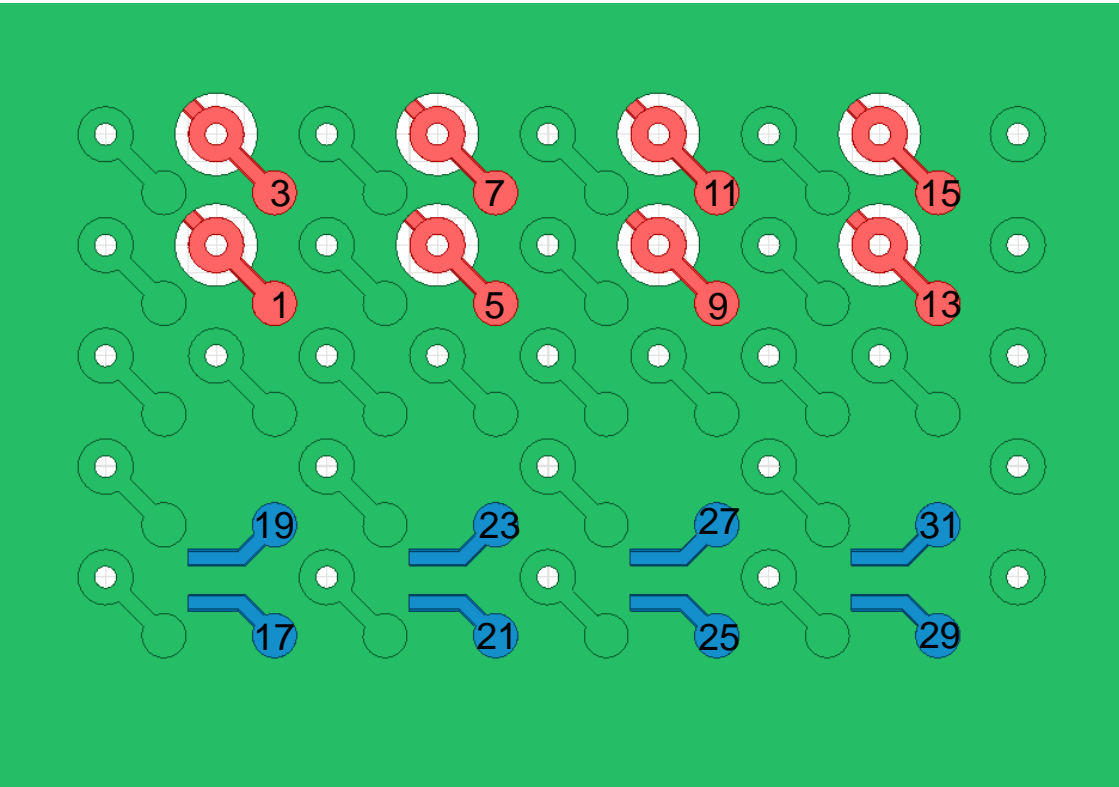
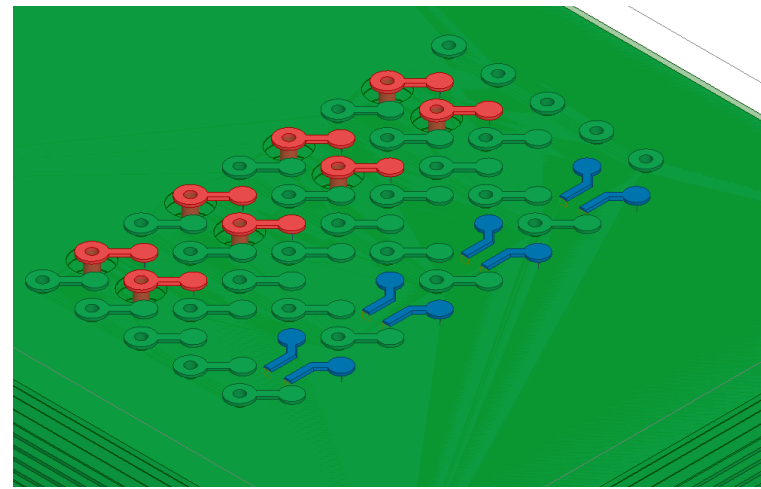


Board Material	Total Length	Loss at 12.9GHz
Meg6_LowSR*	17.5"	14.5dB

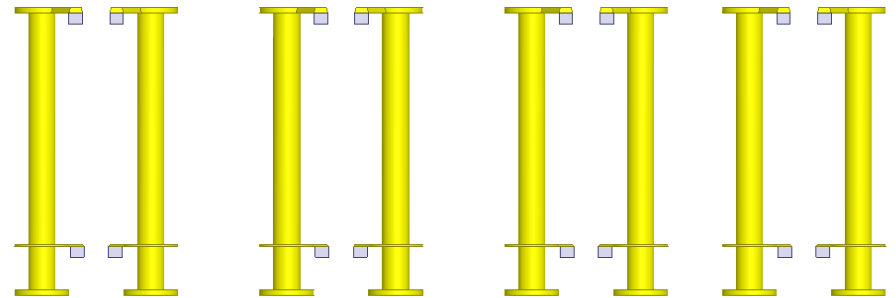
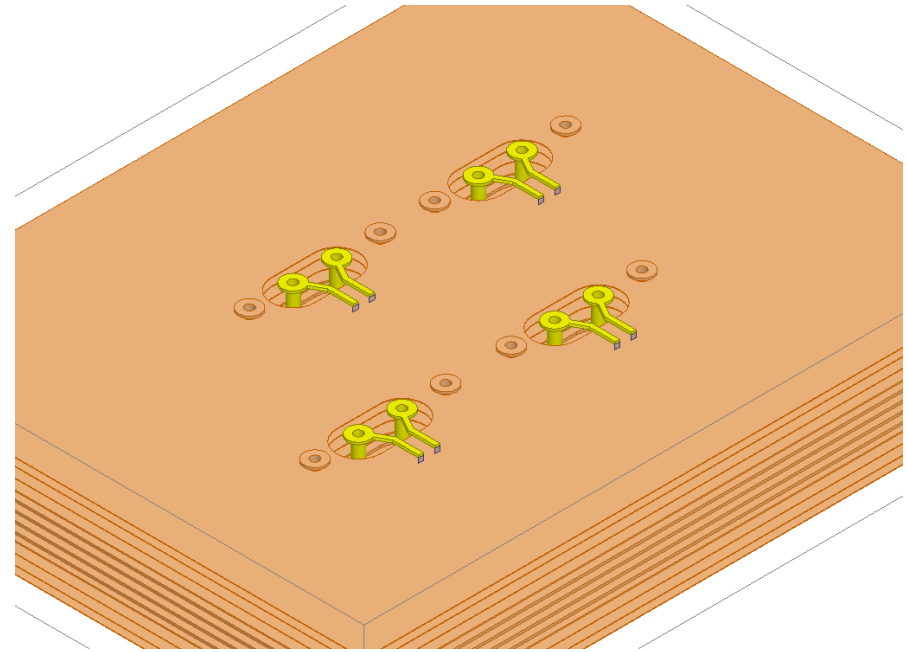
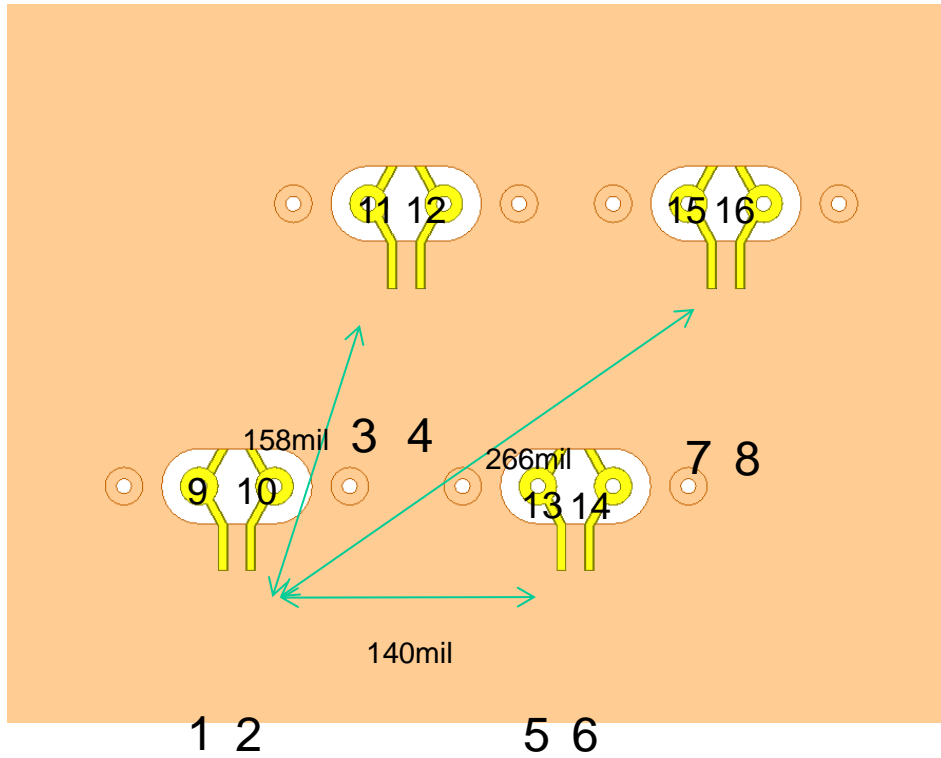
This is the simplest of designs. A design involving an connector will be more challenging. This design needs to have plenty of margin.

\*[http://www.ieee802.org/3/bj/public/jan12/kochuparambil\\_01a\\_0112.pdf](http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf)

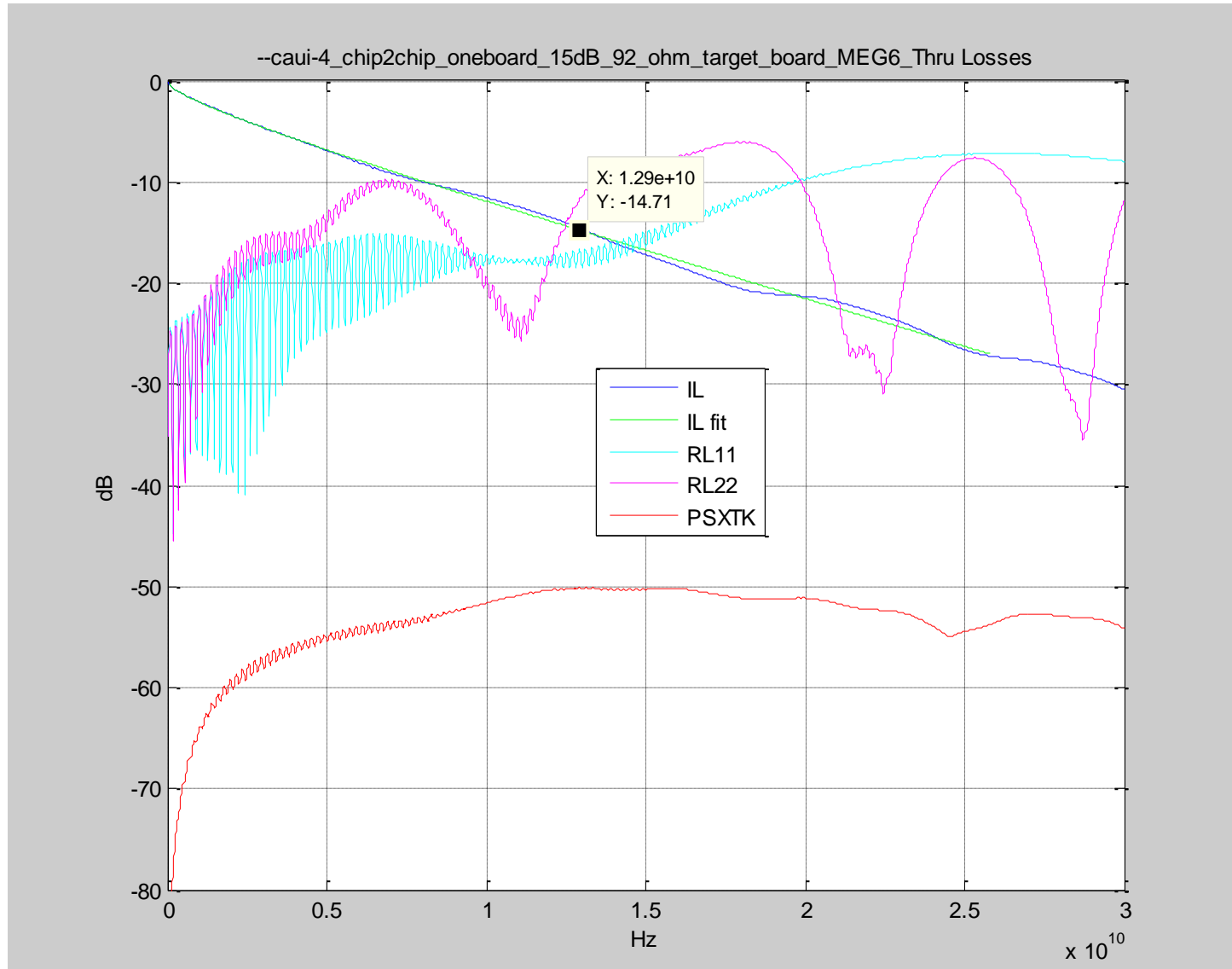
# BGA Attach Model



# Board Via Model



# IL, RL, PSXTK Report for Thru, 3 FEXT, & 4 NEXT ... First Look



# COM Parameters

Parameter	Setting	
Coding/Port Type	CAUI-4	
Signal Rate (fb)	25.78125	GHz
[c(-1) c(1)]	[-.18 -.38]	
Nb	0	UI
Gdc, for CTF	-16	dB
Av	0.4	V
Af	0.4	V
An	0.6	V
L	2	
DER0	1.00E-15	
CC1	3	Min COM dB
sigma_rj	0.01	UI
Add	0.05	UI
eta_0	5.20E-08	V <sup>2</sup> /GHz
PDF_bin_size	1.00E-06	V
Samples Per UI	32	
Port Order	[1 3 2 4]	
CTF_step	1	dB
TXFFE_step	0.02	
bmax(1)	1	
bmax(2..Nb)	1	
f_r	0.75	*fb
package_tl_gamma	complex([-1.067e-03 -3.551e-04 -1.027e-03 0.000 -1.179e-05 ],[000 -3.357e-03 -3.818e-02 0.000 3.360e-05 ] )	
package_tl_rho	complex([1.001e-03 -8.004e-18 -3.233e-04 3.228e-20 1.721e-07 ],[000 -8.120e-03 -3.349e-18 7.435e-06 8.747e-21 ] )	
C_d	2.50E-04	nF
R_d	55	Ohm
C_p	1.80E-04	nF
z_p	[12 30]	mm
TX_SNR	29.00	dB

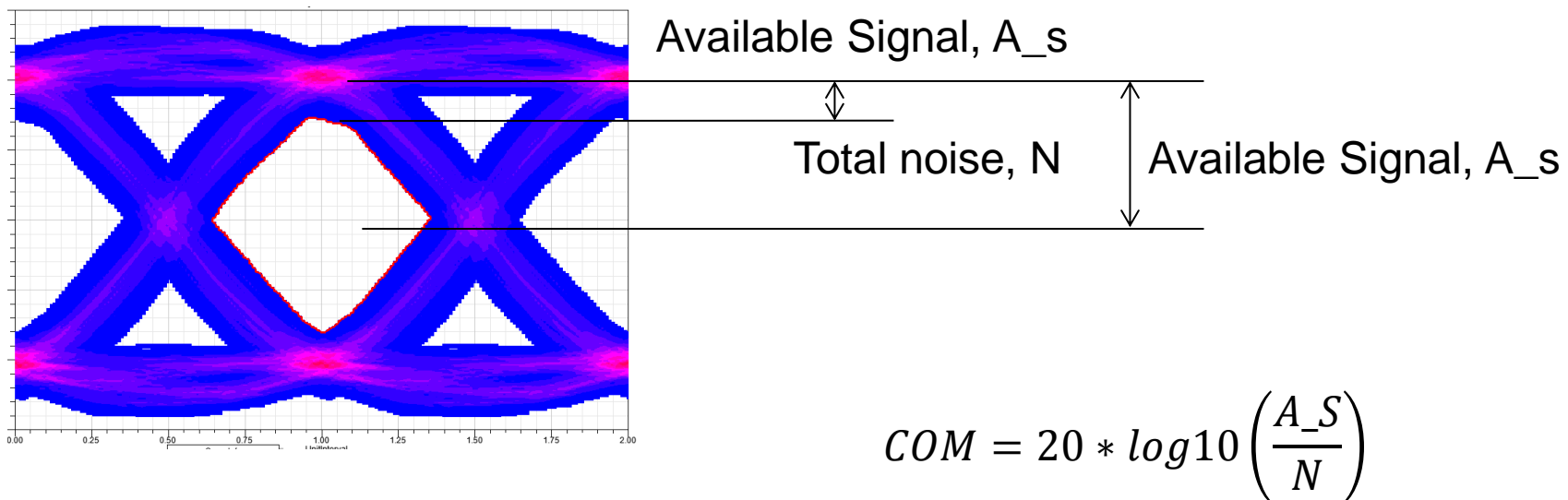
# Critical COM Tx and Rx Parameters

- $Add = 0.05$  (peak dd noise)
  - $\sim 3.8$  ps p-p dual Dirac Jitter
- $\eta_0 = 5.20E-08$  V<sup>2</sup>/GHz
  - $\sim 1$  mV RMS voltage noise
- $\Sigma_{rj} = 0.01$ 
  - $\sim .388$  ps
- $Tx\_SNDR = 29$  dB
  - Transmitter noise

# Relation Between COM and Simulated EYE

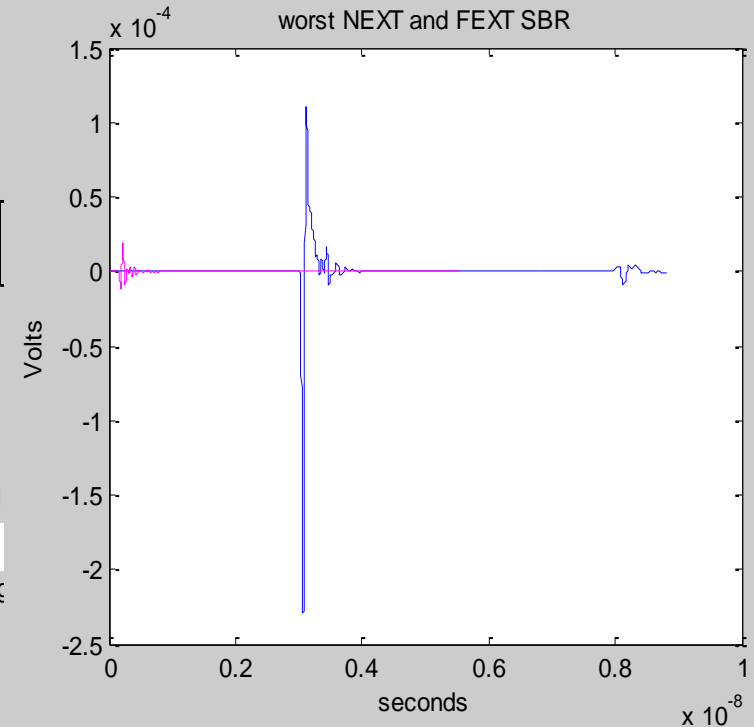
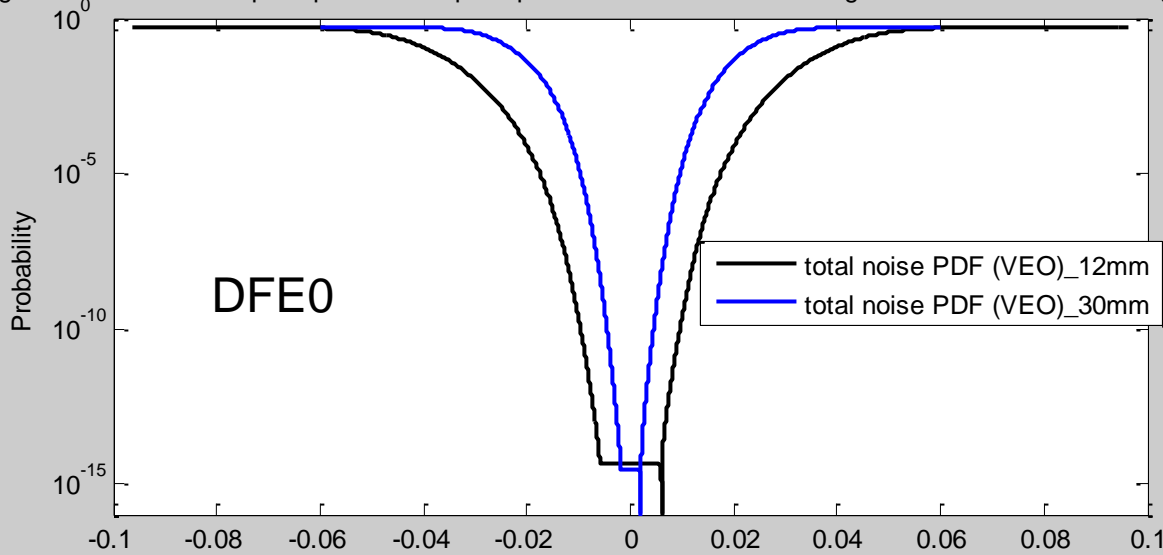
Figure of merit (FOM) used to determine equalization.

- Best ratio of signal at sample point to rms of all appropriate cursors using single bit response (SBR)

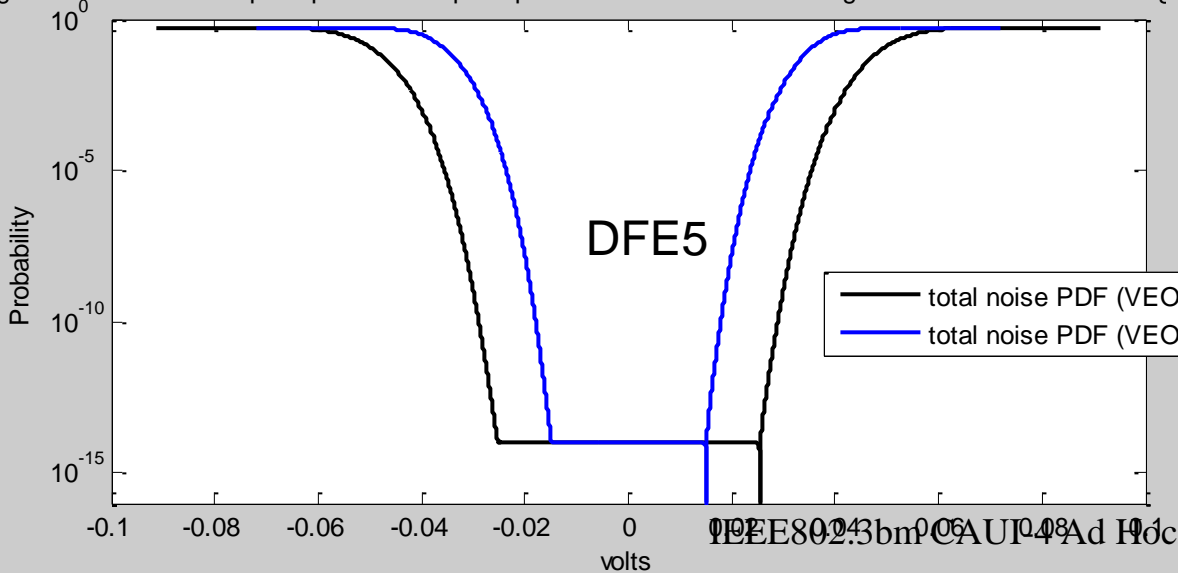


# Vertical Eye Openings (VEO) and WC NEXT/FEXT SBR show DFE5 improvement

B Meg6 LowSR one brd chip2chip--caui-4 chip2chip oneboard 15dB 92 ohm target board MEG6 Thru Voltage bathtul



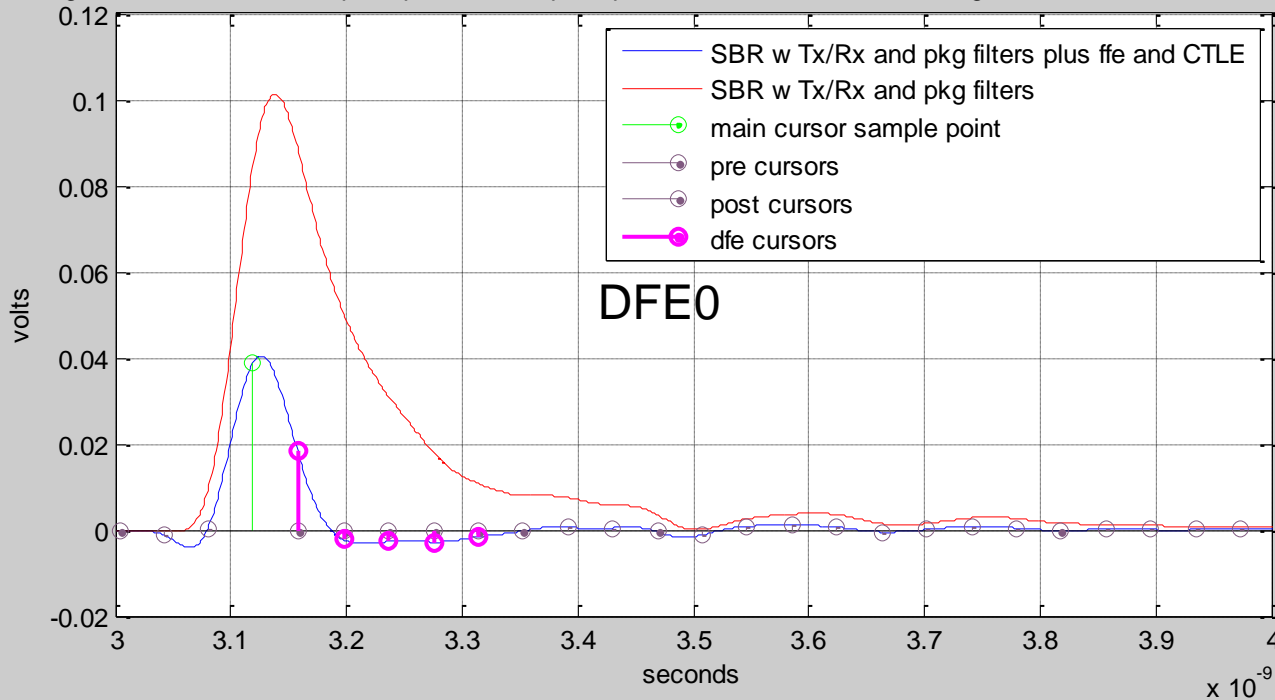
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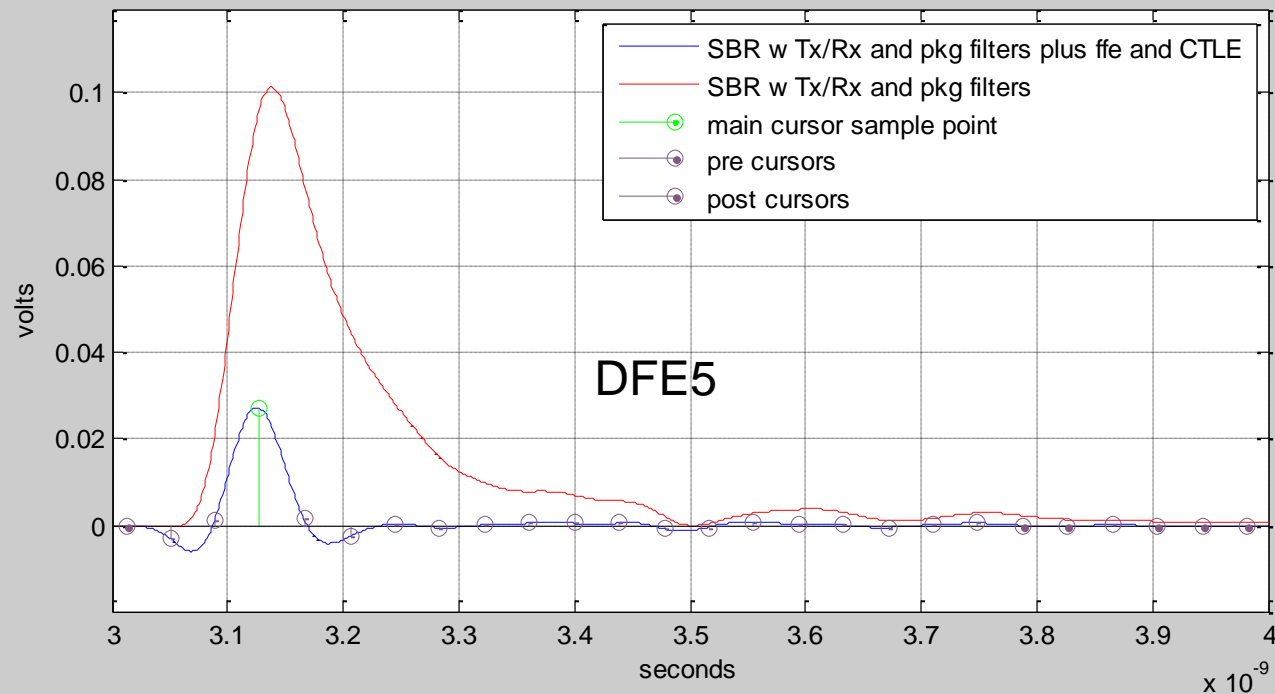
## Crosstalk Pulse Responses

- This case has low XTALK
- Connector systems are expected to have more XTALK.





Single Bit Responses (SBR) illustrate what is going on.



# Results suggest DFE is required

<b>15 dB Meg6_LowSR board model ( vias, etc) Thru, 3 FEXT, 4 NEXT, packages at Tx and Rx</b>		
DFE	Z_p (package Length)	COM / VEO
0	12	0.99 dB / 10mV
0	30	0.43dB / 2.5mV
5	0	3.9db / 28mV
5	30	5.2dB / 48mV

Results suggest no DFE into and instrument would look OK

<b>15 dB Meg6_LowSR board model ( vias, etc) Ideal Instrument Rx Termination, package at Tx only.</b>		
DFE	Z_p (package Length)	COM VEO
0	12	4.38dB / 36mv
0	30	4.01dB / 34mV