CAUI-4 Ad hoc

Ryan Latchman ryan.latchman@mindspeed.com

Agenda

- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Send email confirming attendance, company and affiliation to ryan.latchman@mindspeed.com
- COM discussion (mellitz_bm_CAUI_4_adhoc_01_070313)
- TBDs and consensus building (with a focus on 83D)

COM

- http://www.ieee802.org/3/bj/public/tools.html
- Further evaluation of CAUI-4 settings in COM required

Table 93–9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_d z_p C_b	TBD	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	TBD	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	TBD	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	TBD	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit	$b_{max}(n)$	1 for $n = 1$ to N_b	—
Random jitter, RMS	σ_{RJ}	TBD	UI
Dual-Dirac jitter, peak	A_{DD}	TBD	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^15	—

Informative Insertion Loss Budget

- TBC 15dB budget
  - Maintain TBC in next draft

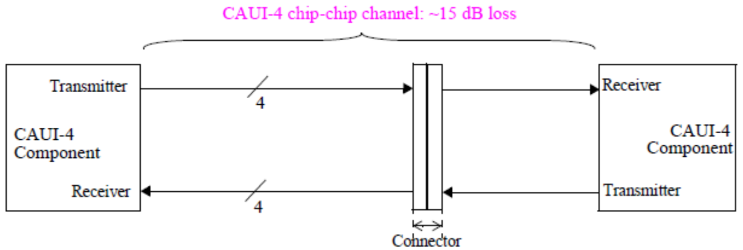

Figure 83D–2—Chip-chip insertion loss budget at 12.89 GHz

EDITORS NOTE: Insertion_loss equation is TBC

$$Insertion\_loss(f) \le \begin{cases} 1.614(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.614(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad (83D\text{–}1)$$

where

f	is the frequency in GHz
$Insertion\_loss(f)$	is the informative CAUI-4 chip-chip insertion loss

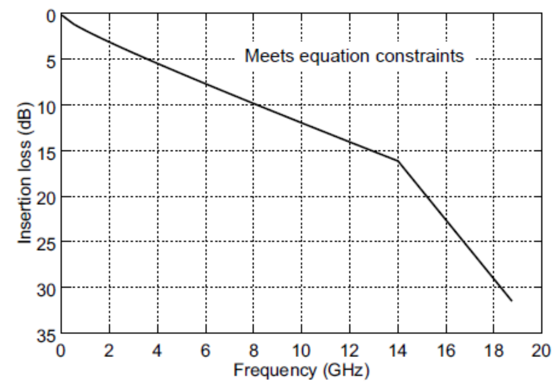

Figure 83D–3—CAUI-4 chip-chip channel insertion loss

Chip-chip transmitter spec

Parameter	Subclause Reference	Value	Units
Output Jitter (max) Random jitter[a] Deterministic jitter[b] Total jitter[c]	83D.3.1.4	0.15 ~~with reference CTLE~~ 0.15 0.28, ~~with reference CTLE~~	UI
Output waveform	83D.3.1.5	TBD (eye mask or other)	
De-emphasis range	83D.3.1.6	TBD (no Tx training or back channel)	

[a]Random jitter at BER of 10^{-15}
[b]~~measured with reference CTLE per section TBD~~
[c]Total jitter at BER of 10^{-15}

Reference CTLE not needed given compliance points

Output Waveform

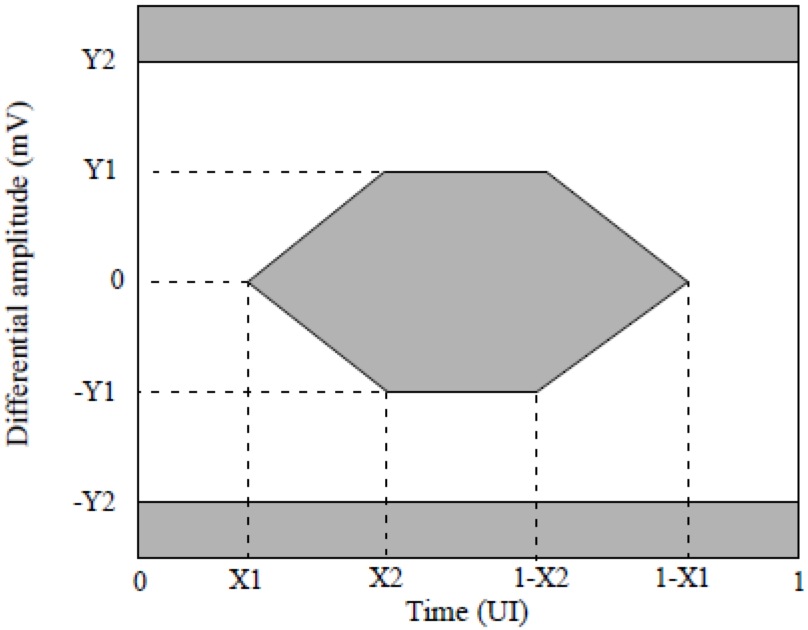

Figure 83A–8—Transmitter eye mask

The above eye mask is defined at BER 1E-15, using the methodology described in section 83D.3.4. Transmitter de-emphasis may be adjusted for optimal mask results

Transmitter mask definition X1: 0.14
Transmitter mask definition X2: TBD
Transmitter mask definition Y1: TBD
Transmitter mask definition Y2: 600

De-emphasis range

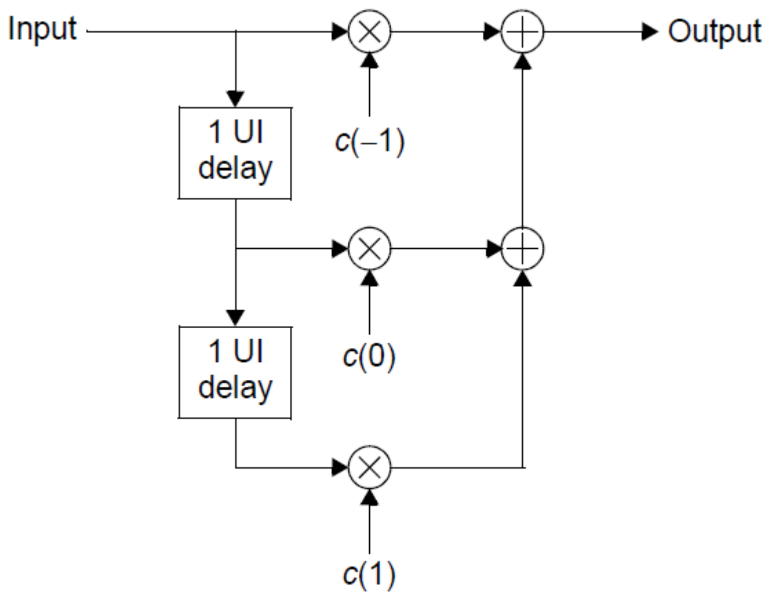

Figure 93–7—Transmit equalizer functional model

Minimum De-emphasis(a):
Post Cursor: TBD dB
Pre Cursor: TBD dB

(a) independent of optimal setting used for transmitter jitter and output waveform measurements

Add to section 83D.3.1.6
The CAUI-4 chip-chip transmitter includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in TBD. The minimum precursor de-emphasis (c(-1)) is TBD. The minimum post cursor de-emphasis (c(1)) is TBD.

The transmitter output de-emphasis is characterized using the procedure described in TBD [editor note: add section on transmitter de-emphasis]

Interference Tolerance Test

The interference tolerance test is performed with the setup shown in Figure 83D–10. A reference CRU with bandwidth of 10 MHz and peaking of less than 0.1 dB is used to characterize the stress signal using a PRBS9 pattern. The reference receiver includes a selectable software CTLE given by Equation TBD and Table TBD. The stressed signal is generated by adding deterministic sinusoidal jitter to a clean pattern, followed by frequency dependent attenuation, and interference injection. The amount of applied peak-to-peak sinusoidal jitter used in the interference tolerance test is given in Table 83D–3. Frequency dependent attenuation is applied using a channel with insertion loss and COM value given in table 83D-3. Broadband noise is added via the interference generator and is added such that the eye opening using the reference receiver and optimal CTLE setting is TBD. The minimum level of broad band noise applied is given in table 83D-3. Eye height and eye width are measured using the reference CTLE setting which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2.

Counter propagating crosstalk channels are asynchronous with target amplitude of TBD mV peak-to-peak differential.

The pattern is changed to PRBS31 for the interference tolerance test with different seeds for each lane. All lanes are active during the stressed receiver test.

Table 83D–4—Receiver interference tolerance parameters

Parameter	Test Value	Units
Maximum BER[a]	10^{-15}	dB
Applied peak-to-peak sinusoidal jitter	$5 \times \frac{105}{f}(100\text{kHz} < f \leq 10\text{MHz})$ $0.05(10\text{MHz} < f \leq 10\text{LB})$	UI
Applied broad band noise	TBD	
Applied peak-to-peak random jitter	TBD	V
Minimum eye height after reference CTLE	TBD	
Channel insertion loss at 12.89 GHz	TBD	
COM of ISI channel	TBD	

[a]Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of the standard

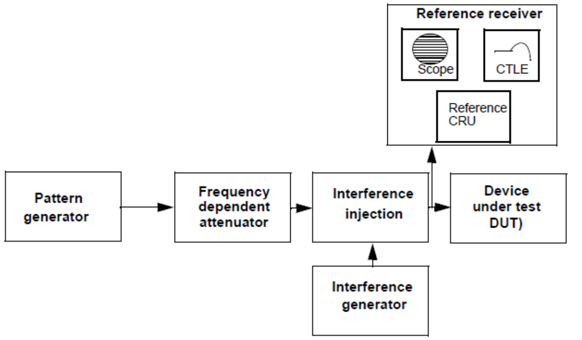

Figure 83D–10—Interference tolerance test setup