CAUI-4 Chip to Chip Simulations

CAUI-4 Adhoc

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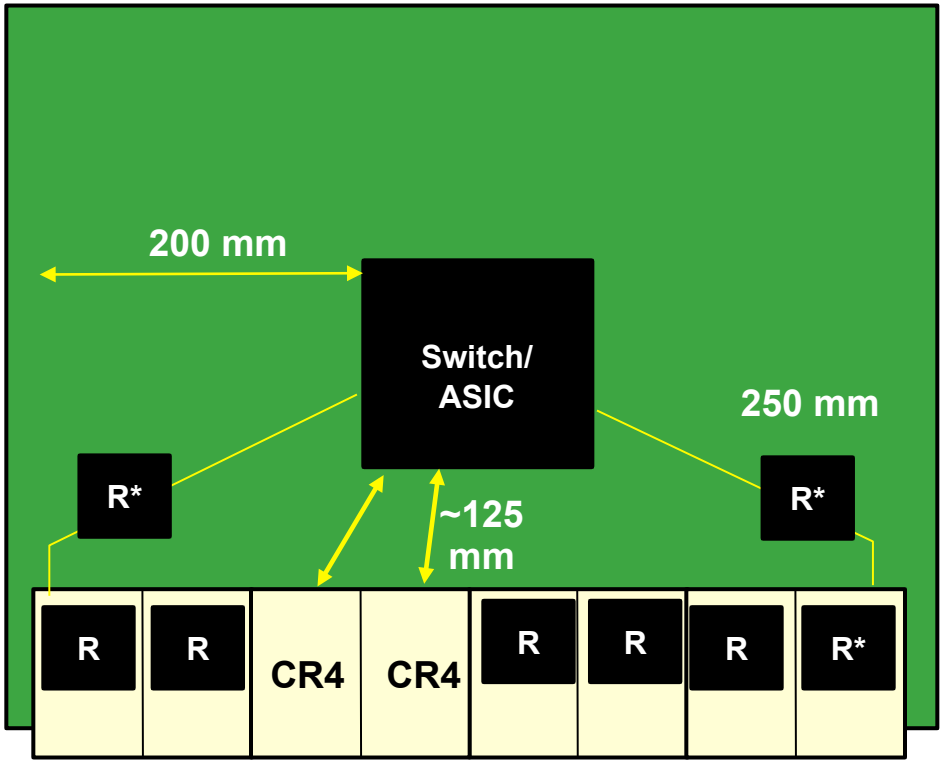
Overview

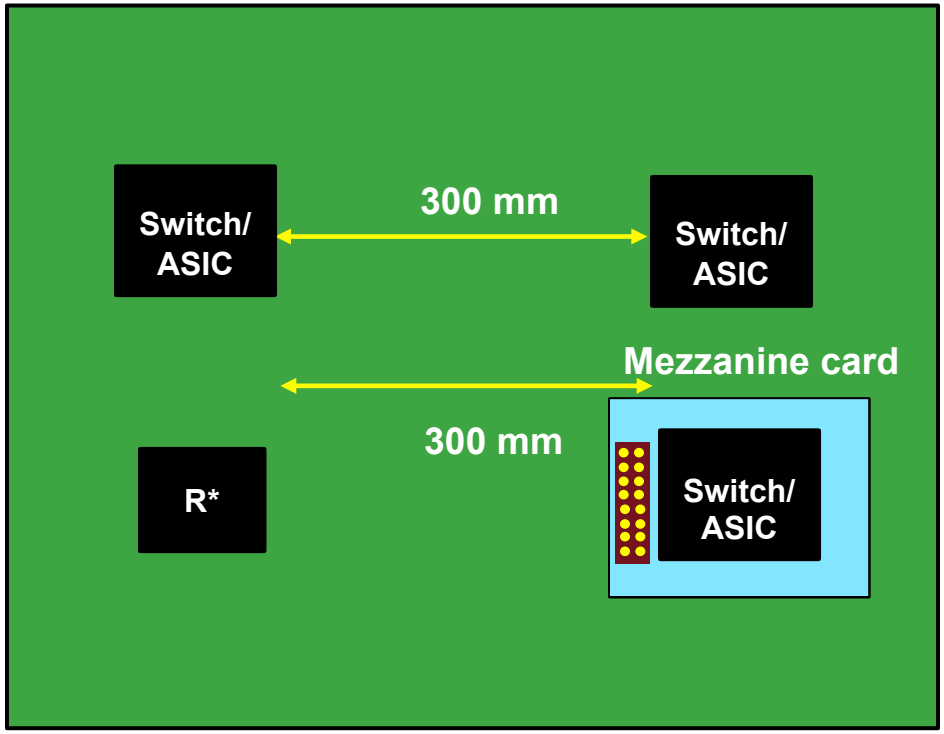
- A CAUI-4 chip to chip adhoc has been investigating channel with13-20 dB assuming TX FIR with RX CTLE
- Results presented in Phoenix showed feasibility of 15 dB channel http://www.ieee802.org/3/bm/public/jan13/ghiasi_01a_0113_optx.pdf
- Results presented in Phoenix also showed far end is function of transmitter amplitude, rise/fall time, and jitter
- Two type of transmitter were defined
  - Hot transmitter with 800 mV diff Amp, TJ=0.28 UI, and Tr/Tf=17 ps
  - Fast transmitter with 600 mV p-p diff Amp, TJ=0.18 UI, Tr/Tf=12 ps
- Hot transmitter delivered greater far end eye opening up to about 11-12 channel loss but as the channel loss increased fast transmitter with less amplitude delivered better far end eye
- Transmitter trade off on the far end are further investigated as function of rise and jitter.

CAUI-4 Applications and Background

- http://www.ieee802.org/3/bj/public/jul12/ghiasi_02a_0712.pdf identified CAUI-4 applications as well as limitations
- Most common CAUI-4 C2C application is between big chip and little chip
  - Big chip will have challenging ball map and package loss will in ~ 2 to 3 dB
  - Little chip have easily routable ball map and package loss will be in 0.5 to 1.5 dB



* R – Retimer/CDR



PCB Reach for Various Interfaces

- PCB loss estimate assumptions and tools for calculation
  - IEEE 803.bj spreadsheet http://www.ieee802.org/3/bj/public/tools/DkDf_AlgebraicModel_v2.02a.xlsm for N4000-13SI and Megtron-6 calculation
  - Rogers Corp impedance calculator (free download but require registration) https://www.rogerscorp.com/acm/technology/index.aspx for FR4-6 and N4000-13
  - Stripline ~ 50 Ω, trace width is 5 mils, and with ½ oz Cu
  - Surface roughness med per IEEE spreadsheet or 2.8 um RMS
  - FR4-6 DK=4.2 and DF=0.02, N4000-13 DK=3.6 and DF=0.014, N4000-13SI and Meg-6 per IEEE spreadsheet

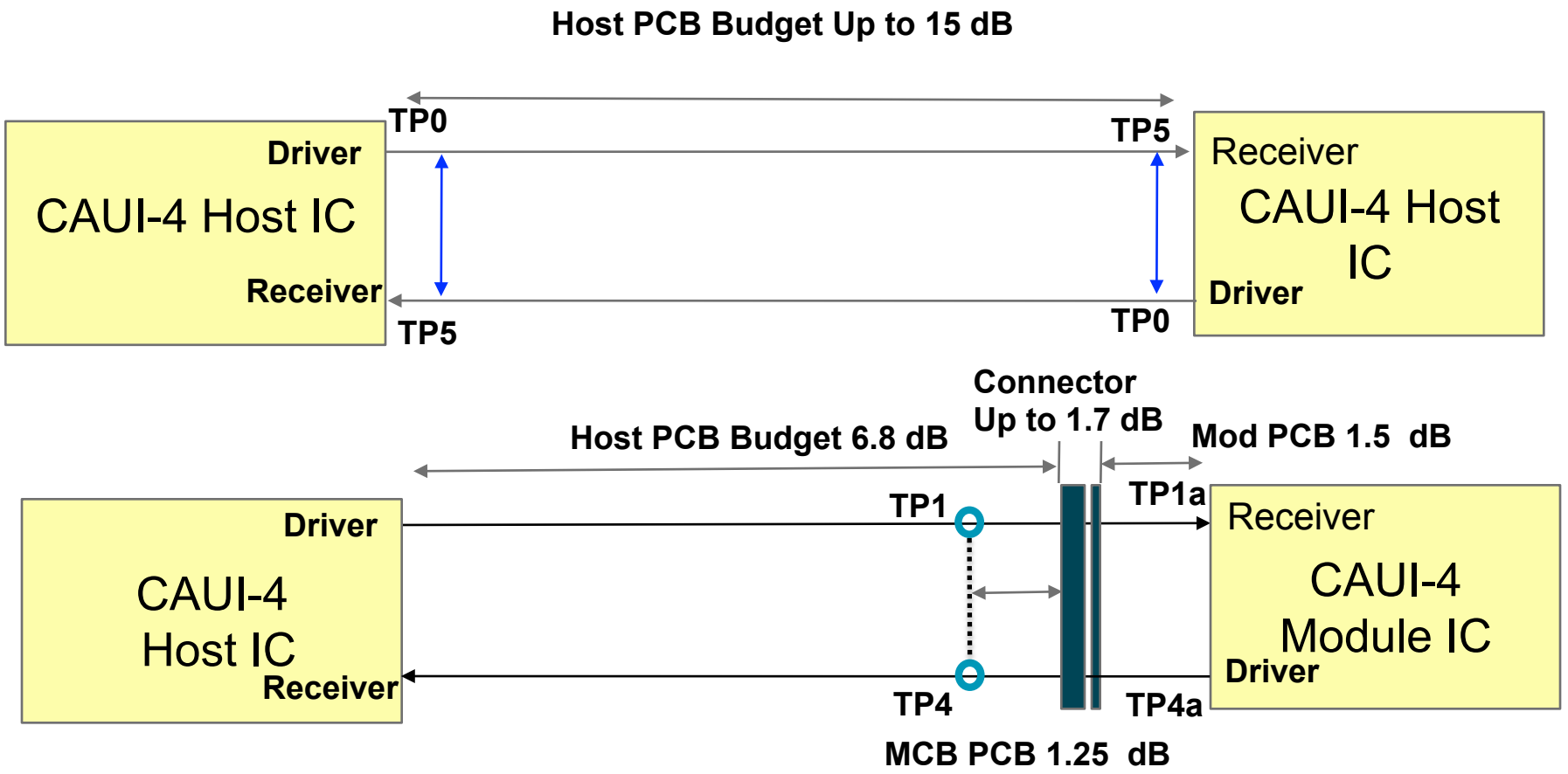
Host Trace Length (in)	Total Loss (dB)	Host Loss(dB)	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal PCB Loss/in at 5.15 GHz	N/A	N/A	1.00	0.79	0.56	0.43
Nominal PCB Loss/in at 12.89 GHz	N/A	N/A	2.00	1.60	1.25	0.92
CAUI Classic	10.5	6.81	6.8	8.6	12.2	15.8
PPI CL85A/86A with one connector & HCB#	6.5	4.37	4.4	5.5	7.8	10.2
CAUI-4 with one connector & HCB*	10.5	6.81	3.4	4.3	5.4	7.4
802.3bj CL92A with one connector & HCB *	10.5	6.81	3.4	4.3	5.4	7.4
CAUI-4 Chip to Module	10	10	5.0	6.3	8.0	10.9
CAUI-4 Chip to Chip	13	13	6.5	8.1	10.4	14.1
CAUI-4 Chip to Chip	15	15	7.5	9.4	12.0	16.3
OIF 28G-MR	20	20	10.0	12.5	16.0	21.7

Assumes connector loss is 0.87 dB and HCB loss is 1.26 dB at 5.5 GHz.

* Assumes connector loss is 1.69 dB and HCB loss is 2.0 dB at 12.89 GHz.

CAUI-4 Architecture and Reference Points

- The bm group need to further study CAUI-4 chip to chip application

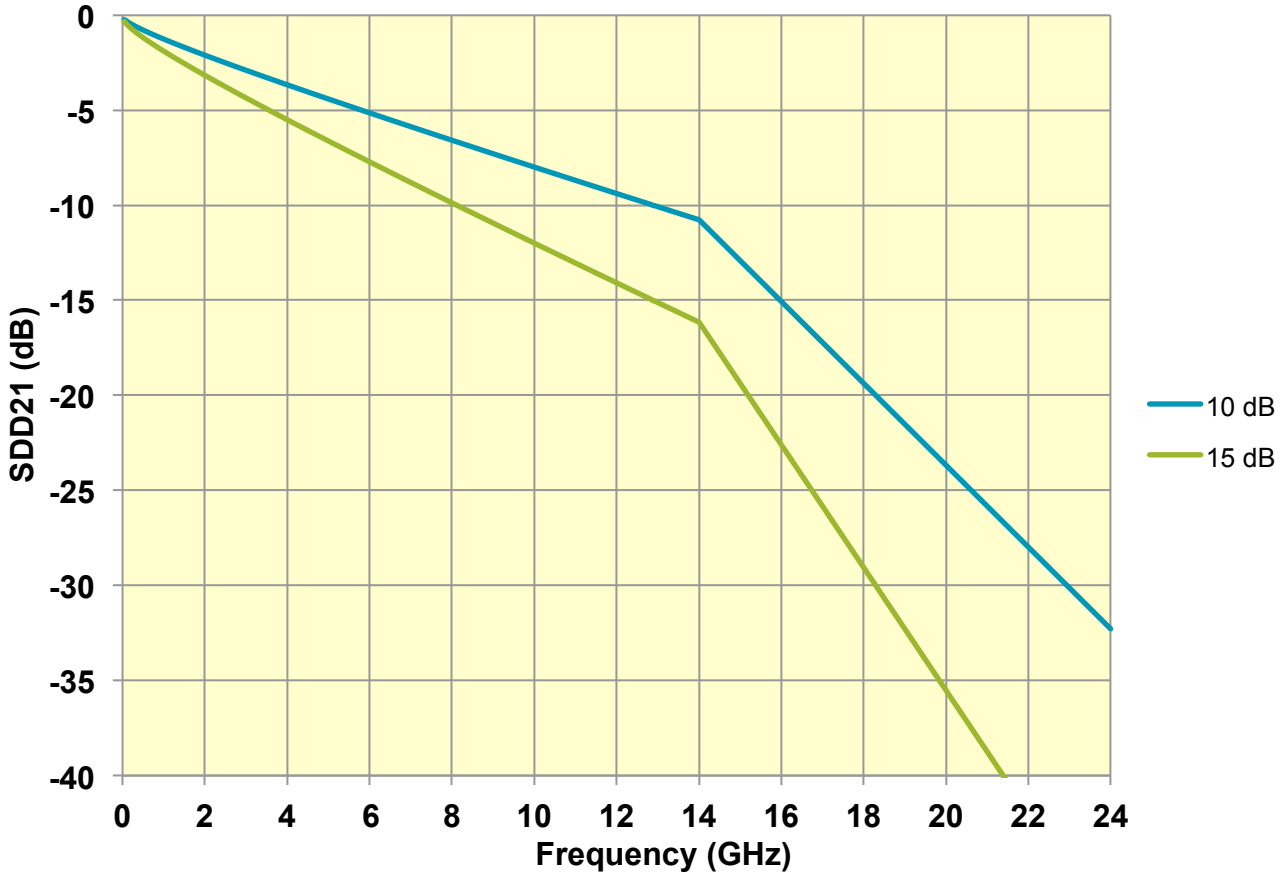


Increasing CAUI-4 Chip to Chip Reach

- Parameters that can increases CAUI-4 chip to chip reach
- Transmitter parameters and exact parameter that can be improved is dependent if this is large ASIC or PHY
  - Rise/fall time – can be made as fast as the min rise/fall time
  - Jitter - could lowered by ~0.1 UI
  - Amplitude - min value can be increased up to 900 mV
  - Return loss – no change
- Channel parameters
  - ILD – template to trade off loss vs ILD
  - ICN – template to trade off loss vs ICN
  - Loss a1 coefficient – needs to be control and only an issue with fat traces on low loss material or super low loss PTFE material
  - Return loss – no change
- Receiver parameters
  - CTLE gain 1-9 dB – no change
  - Sensitivity – to be studied if it needs to improved from 100 mV
  - Return loss – no change

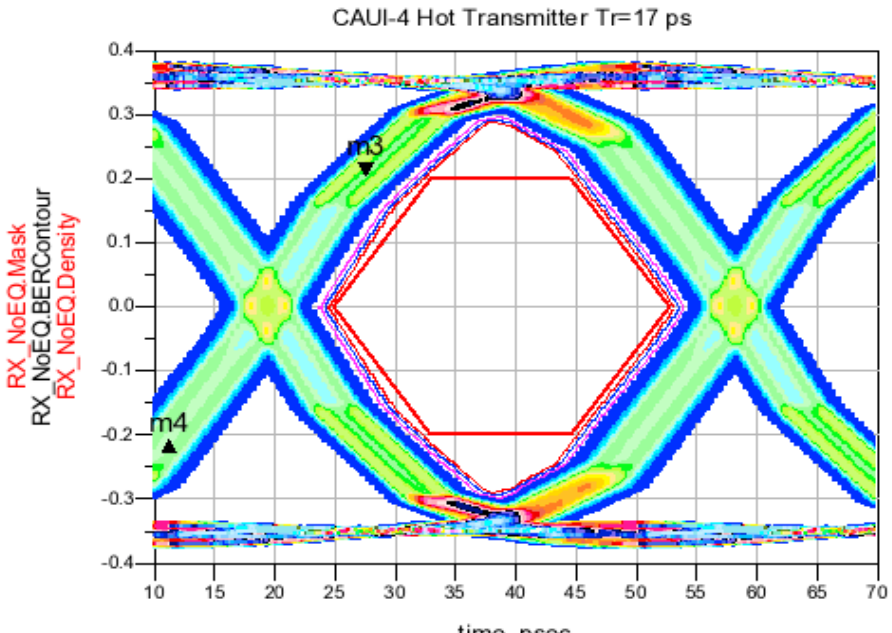
CAUI-4 Chip to Chip Informative Channel

- CAUI-4 chip to chip loss budget
  - By improving some of the transmitter parameters and operating the link where naturally has lower ICN/ILD the loss budget can be 15 dB



Example Big and Little Chip CAUI-4 Transmitter

- Define Hot driver with standard jitter but 800 mV output
  - Tr ~ 17 ps TJ=0.28 UI@1E-15 (de-emphasis 1 dB)
- Define Fast-low jitter with 600 mV output
  - Tr ~ 12 ps TJ=0.18 UI@1E-15 (de-emphasis 0.5 dB)
- Eye mask at TP0a provide flexibility to trade off Tr/Tf, amplitude, and jitter
  - Mask coordinates (0.14,0), (0.35,±0.2), (0.65,±0.2), (0.86,0)



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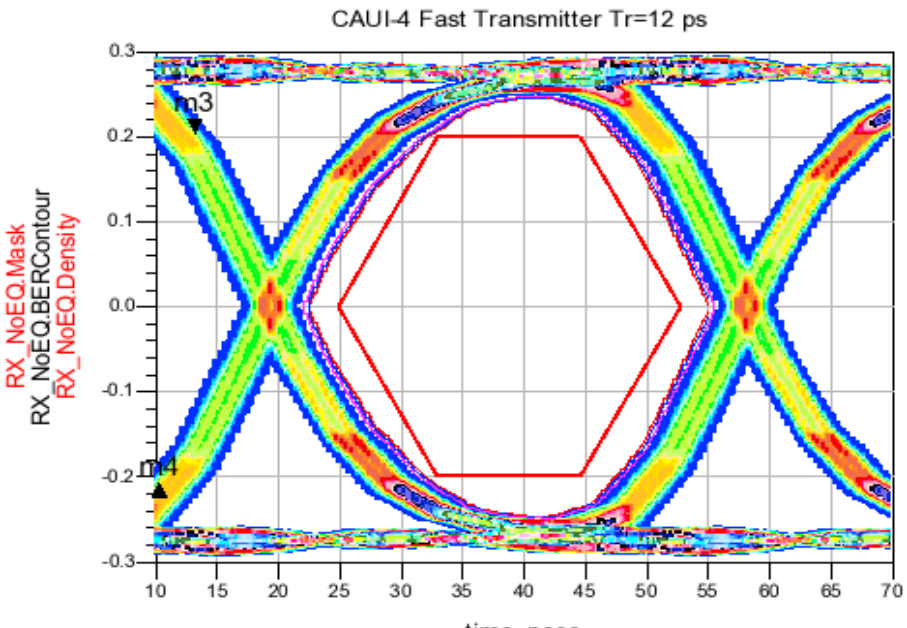

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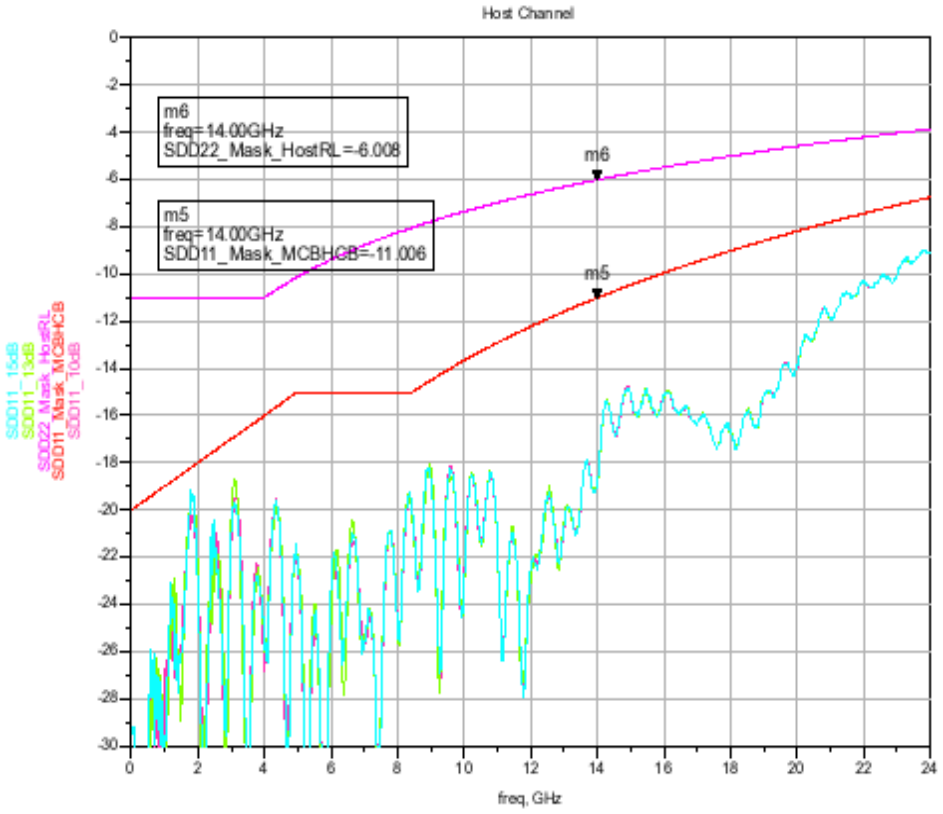
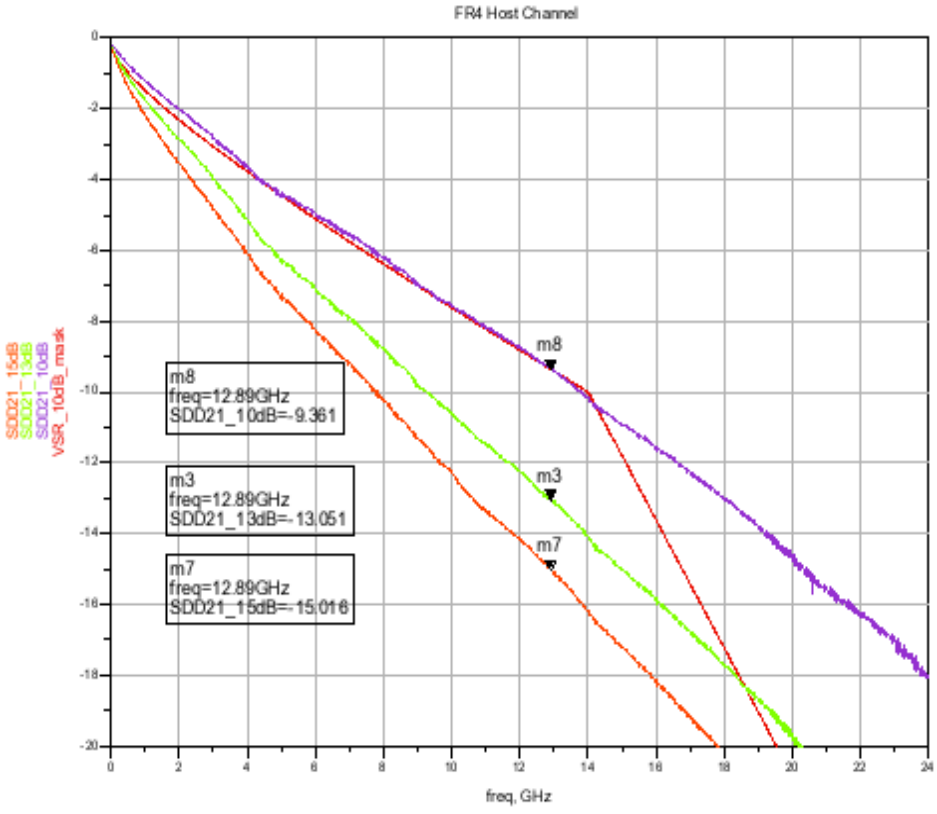
FR4 Channel Response

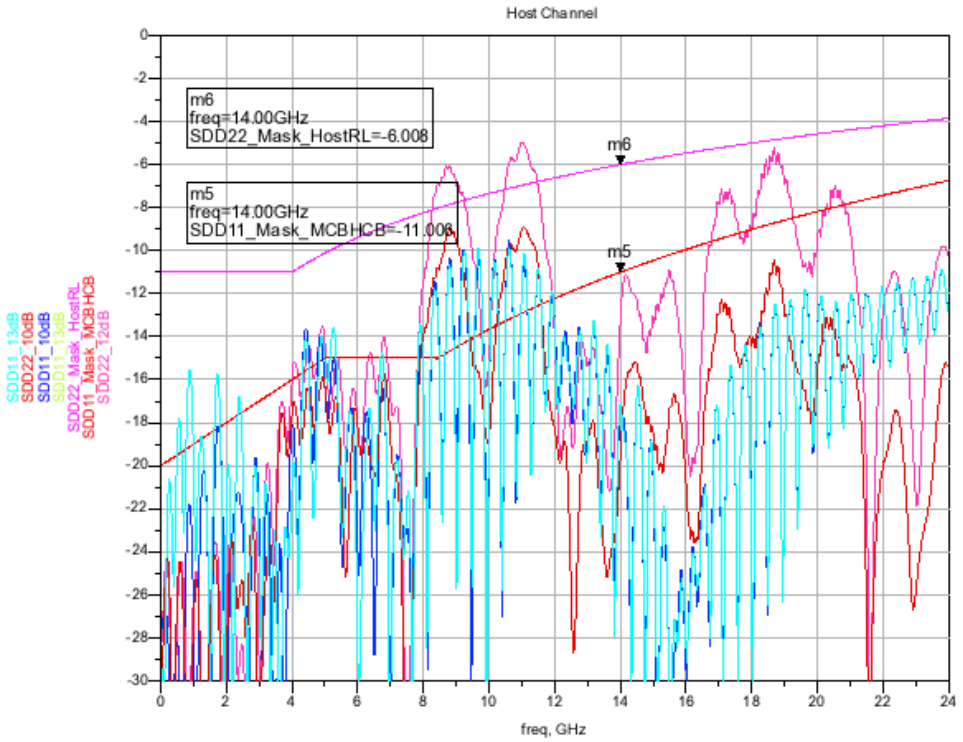
- Channels are
  - 5” FR4 Channel with two long (80 mils) vias and 2 12 mils stub
  - 5” FR4 + 3” Meg6 Channel
  - 5” FR4 + 5” Meg 6 Channel

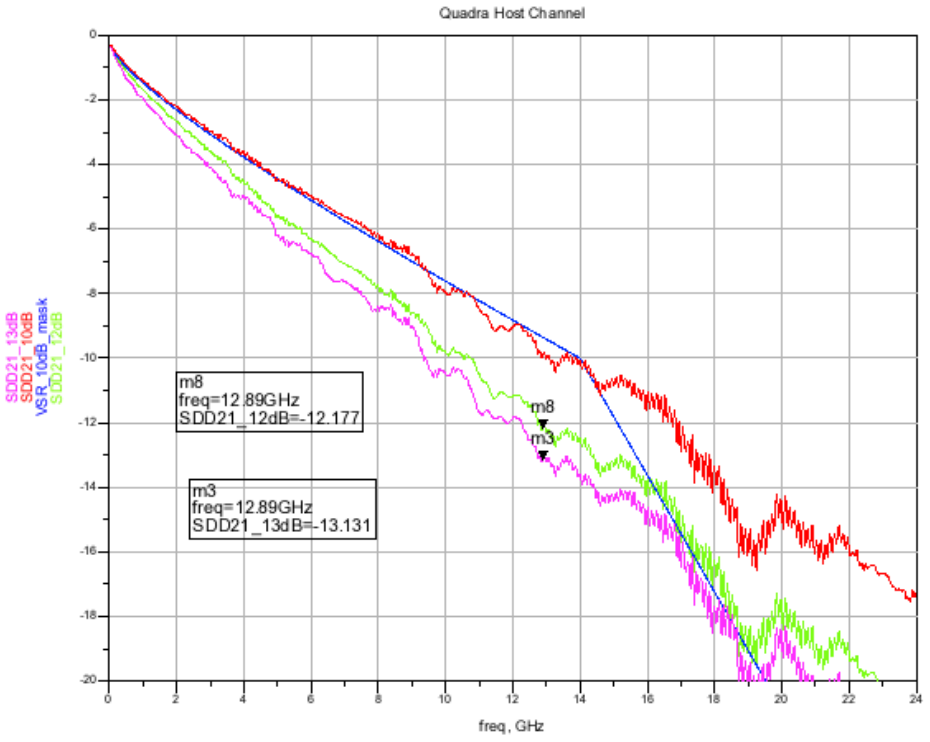




TE 7” Quadra Channel Response

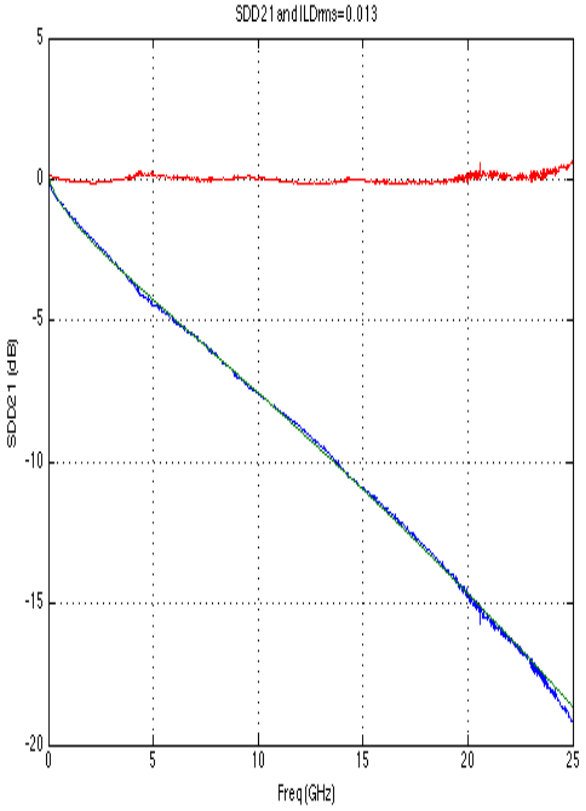
- Channels are
  - TE Quadra channel with 10 dB loss
  - TE 7” Quadra + 1.25” plug board+ 2” Meg6 Channel
  - TE 7” Quadra + 1.25” plug board + 2” FR4 Channel

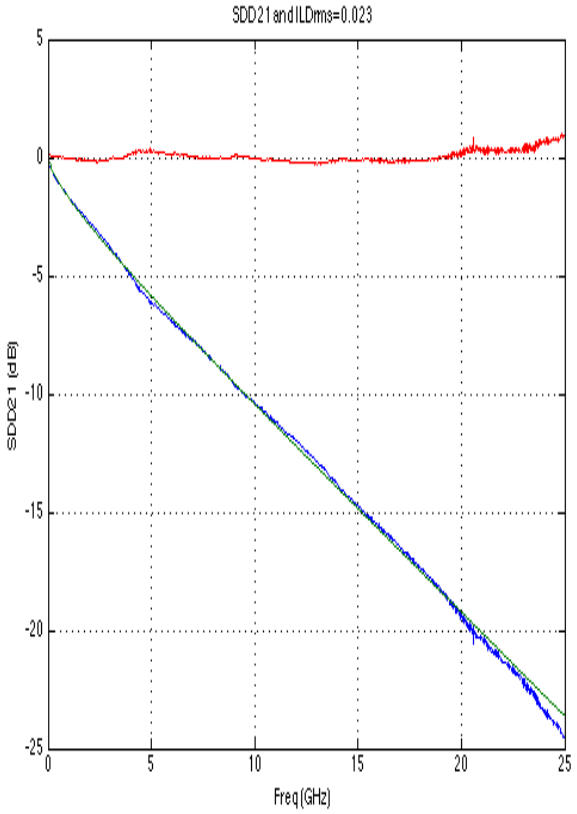


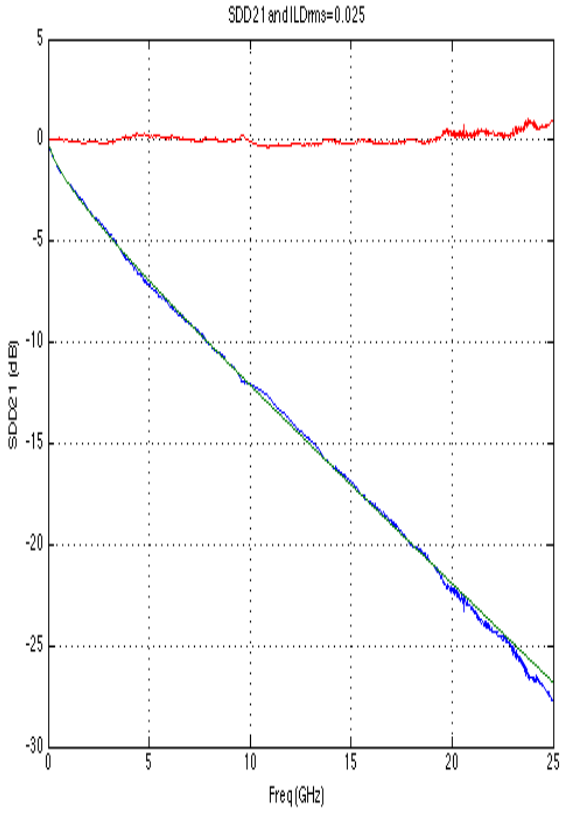


FR4 Channel ILD and Fit

- 10 dB channel has ILDrms=0.013 and a1/a0=0.23
- 13 dB channel has ILDrms=0.023 and a1/a0=0.59
- 15 dB channel has ILDrms=0.025 and a1/a0=0.46

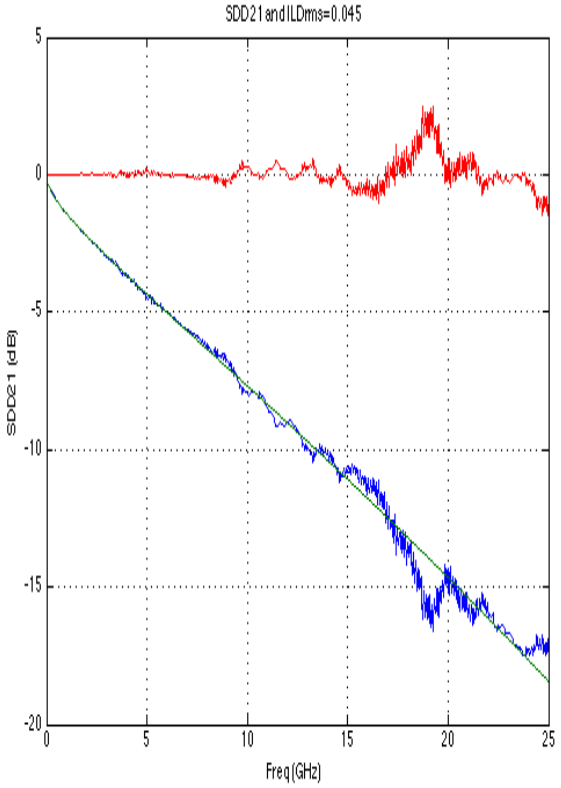


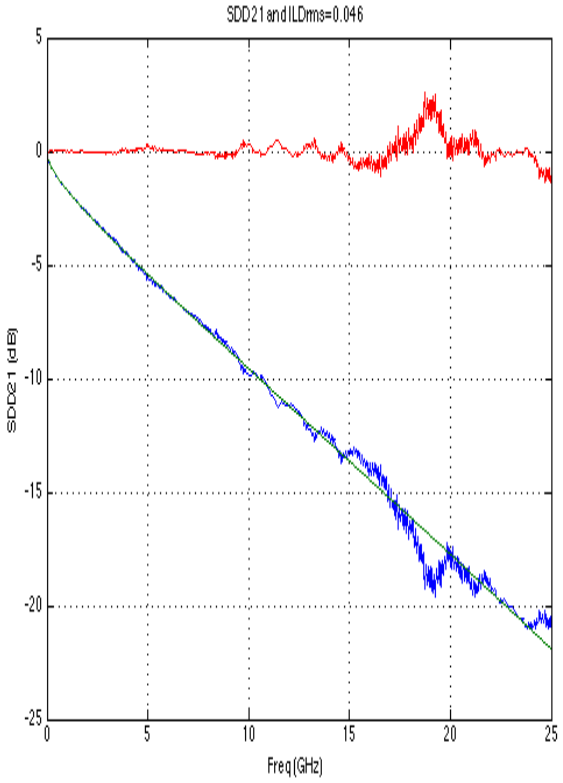


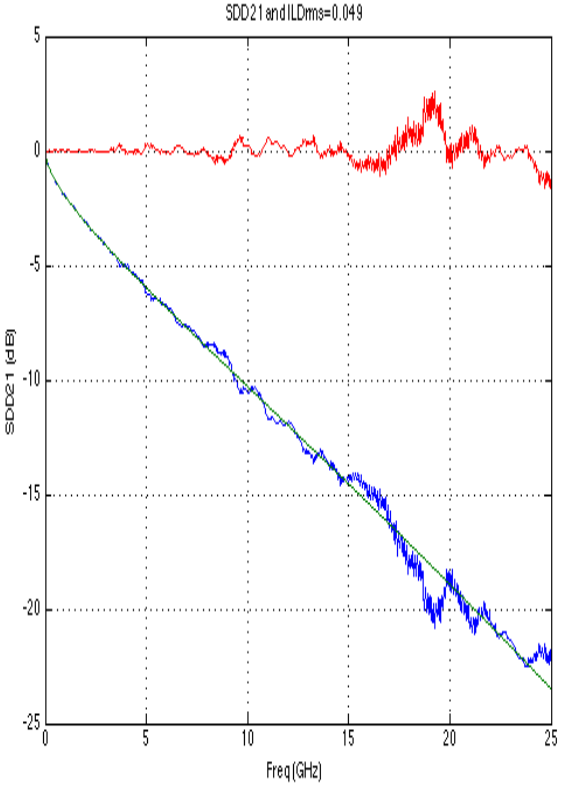


TE Quadra Channel ILD and Fit

- 10 dB channel has ILDrms=0.045 and a1/a0=0.45
- 12 dB channel has ILDrms=0.046 and a1/a0=0.62
- 13 dB channel has ILDrms=0.049 and a1/a0=0.34

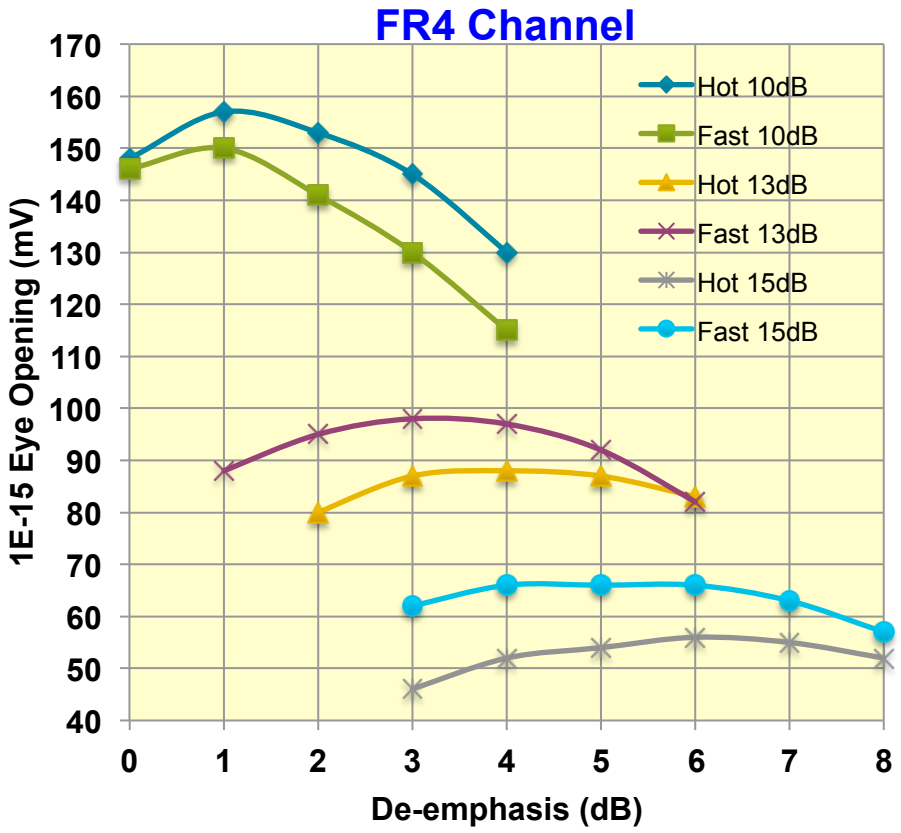


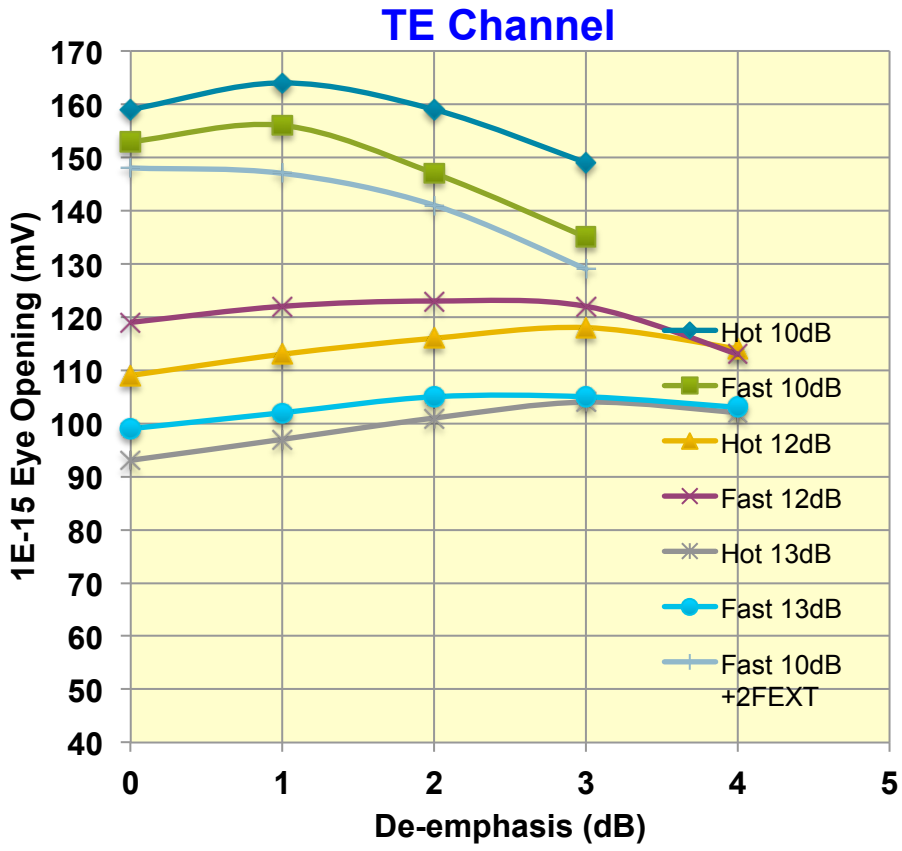




Summary of Eye Opening

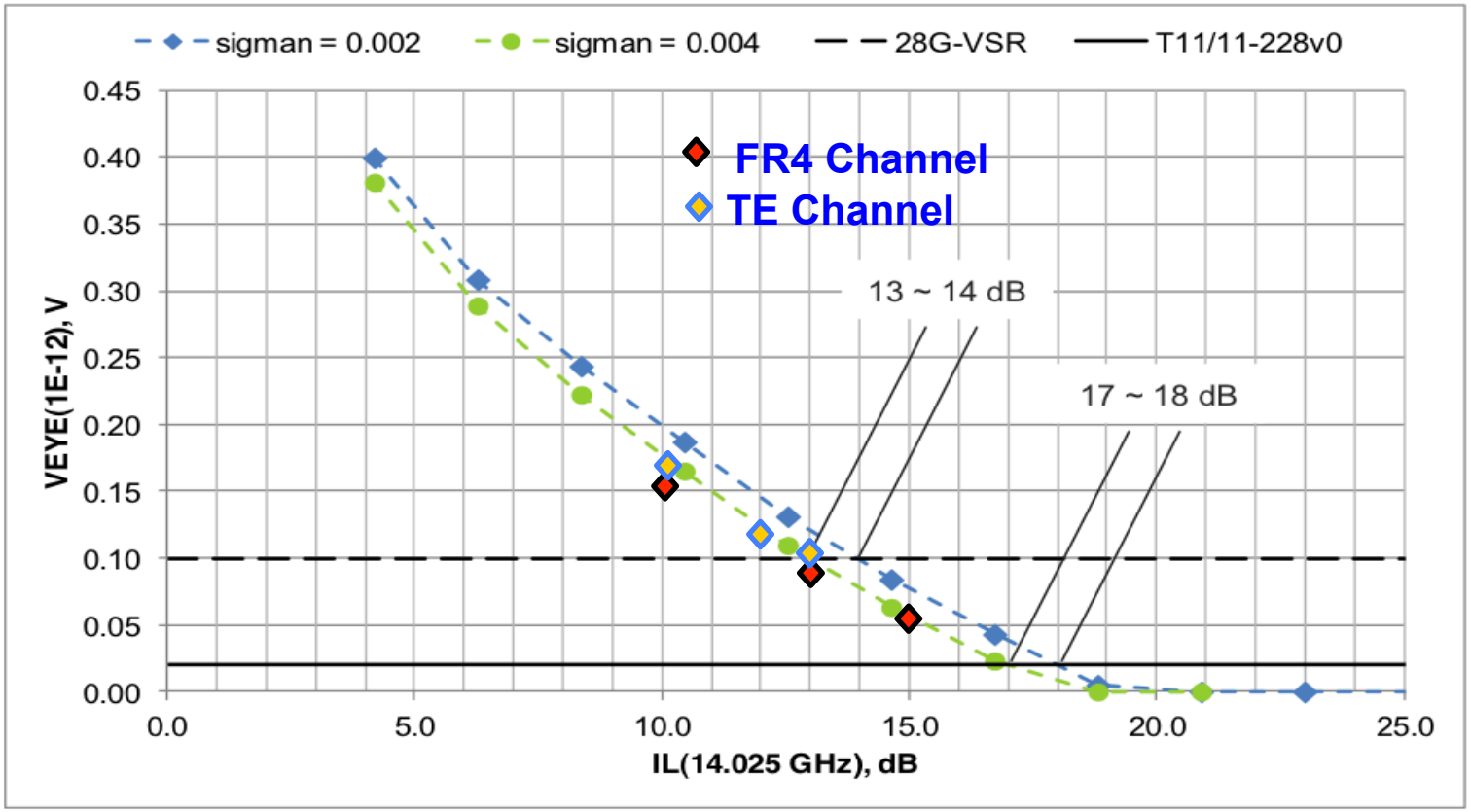
- Hot driver and fast driver have nearly similar far end performance!
- TE Quadra 10 dB channel has slightly better performance compare to channel with two long vias (~80 mils) and two short stub (~12 mils)
- Considering only 2 FEXT TE 10 dB channel ~ 6% VEC penalty





Results Matches Healy T11 VSR Simulations

Full results and assumption are available from T11 website http://www.t11.org/fd/11-448

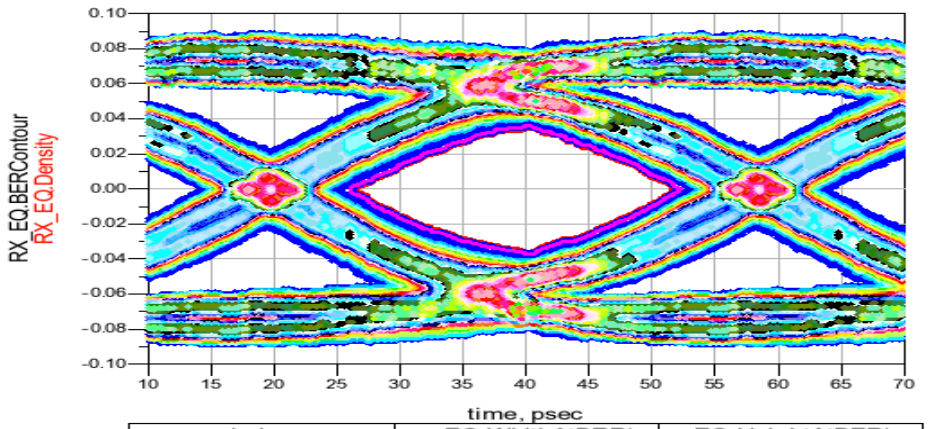


NOTE: Insertion loss includes device packages

Effect of Driver jitter and Rise Time on TP5

- Driver (600 mV p-p) Rise and fall time has the biggest impact on TP5

15 dB FR4 Ch CTE9 Post 5dB Fast Driver PJ=2 ps s=0.006 UI Tr=11.5 ps



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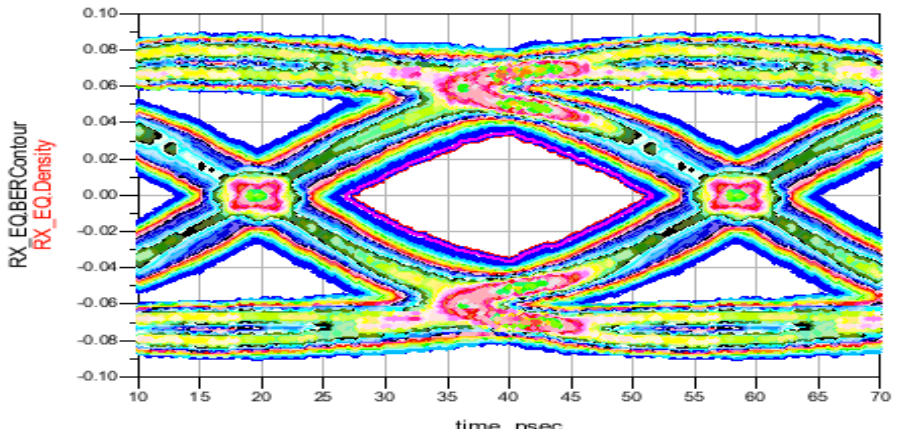
15 dB FR4 Ch CTE9 Post 5dB Fast Driver PJ=3.6 ps s=0.006 UI Tr=11.5 ps



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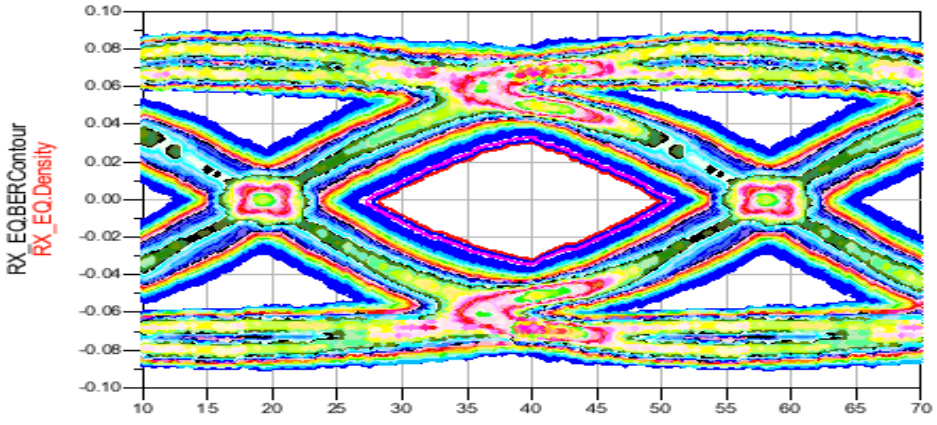
0.000	2.424E-11	0.068

15 dB FR4 Ch CTE9 Post 5dB Fast Driver PJ=3.6 ps s=0.01 UI Tr=11.5 ps



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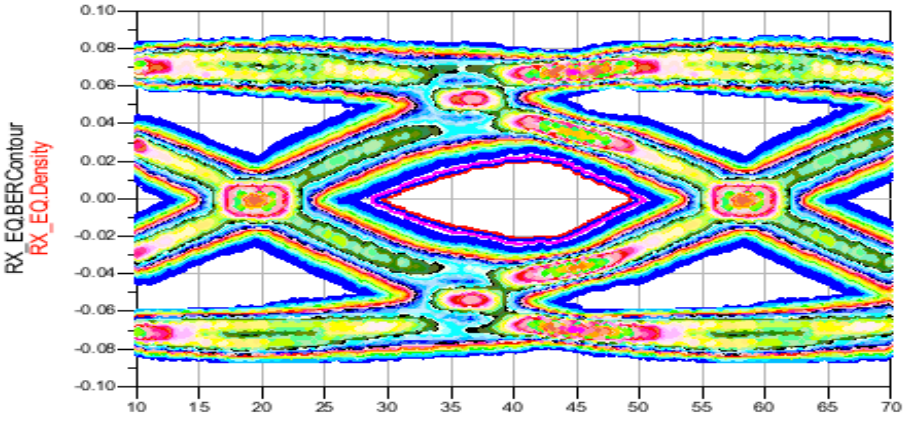
15 dB FR4 Ch CTE9 Post 5dB Driver PJ=3.6 ps s=0.01 UI Tr=17 ps



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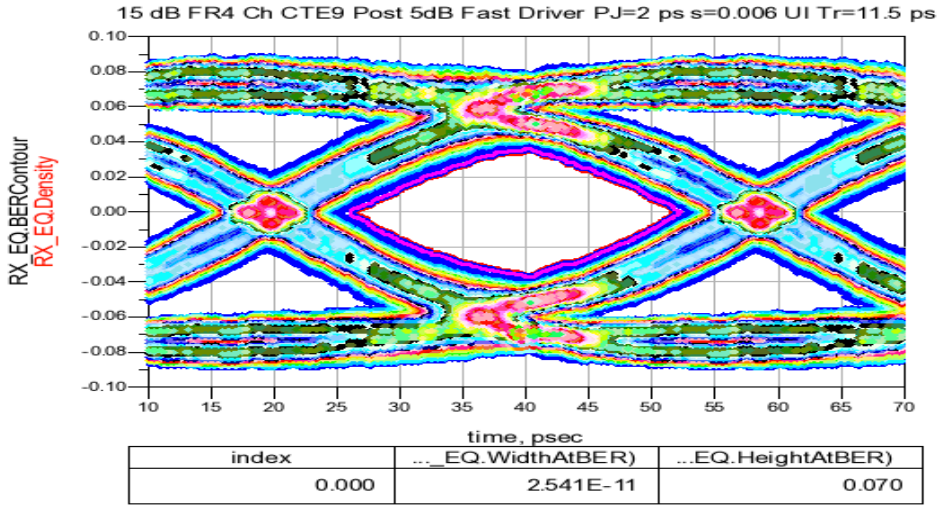
Effect of Driver Rise Time on TP5

- Low jitter driver (600 mV)as function of rise and fall time



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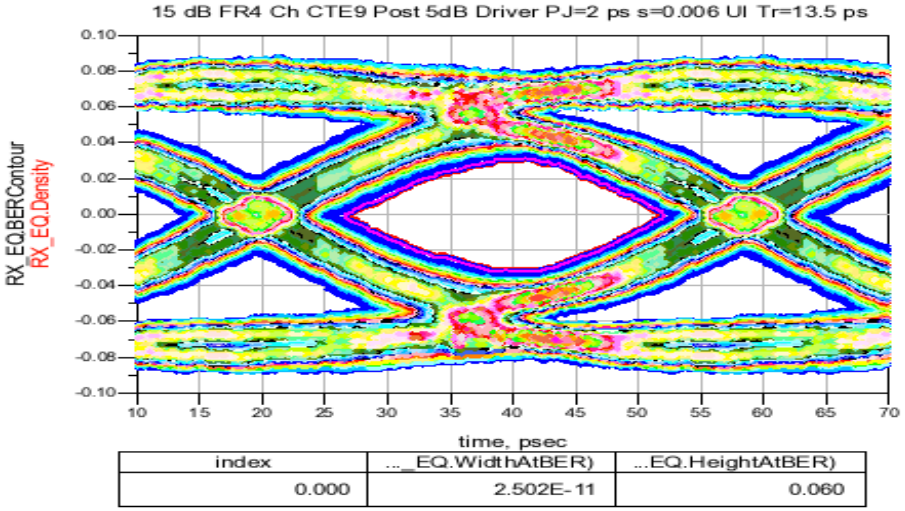

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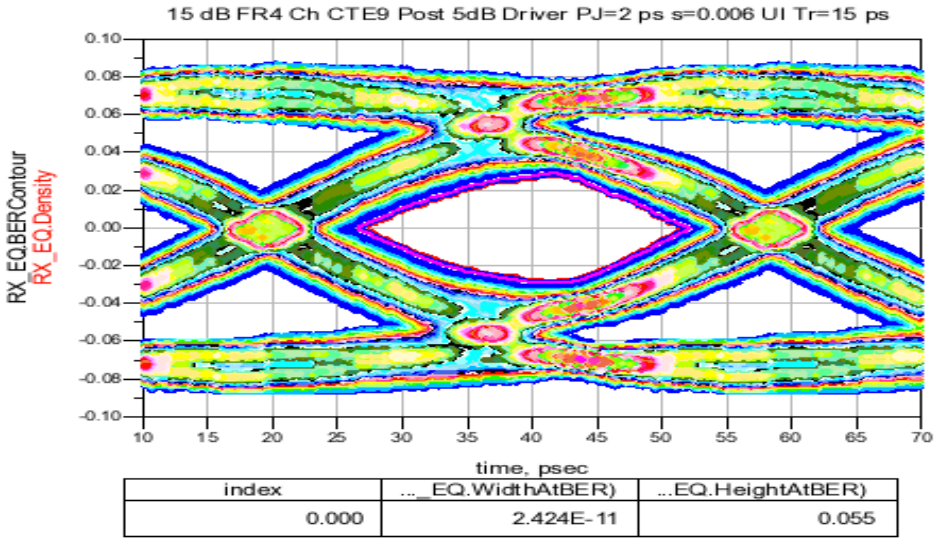

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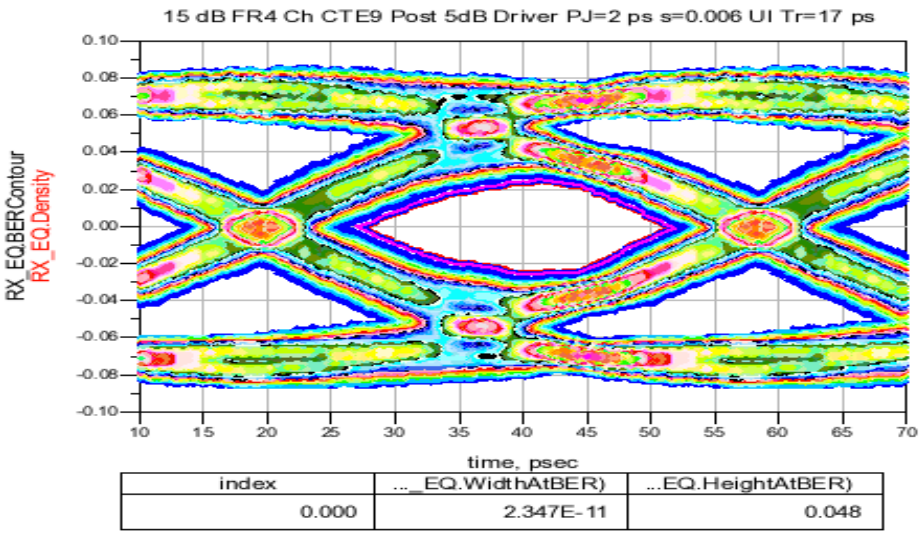

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How to deal with compliance

- Transmitter Normative
  - CAUI-4 test method at TP1a can be applied to TP0a
  - Apply statistical eye mask for compliance either at 1e-12 or 1E-15
  - Eye mask allows to trade off transmitter Tr/Tf, jitter, and amplitude to deliver similar TP5 eye for range of transmitter for given channel
    - COM does not provide trading off transmitter property for equal far end eye
    - BJ output waveform does capture amplitude aspect, indirectly the Tr/Tf, but jitter effect drop off due to average waveform
- Receiver Normative
  - Use CAUI-4 TP1a test method with software CTLE to determine hardware compliance
  - The same CTLE can be used on simulated channel to determine far end eye for compliance with commercial tools ADS, SiSoft based on actual driver AMI model
- Channel Informative
  - Define generic 15 dB loss but actual link performance will vary based on the channel impairment
  - As a group we can retrofit COM with generic transmitter model as a tool to qualify channels

Summary

- For CAUI-4 chip to chip two channels were investigated
  - FR4 channel with deep vias and short stubs
  - TE Quadra based channel
- Result shown here is far end eye excluding DC block and receiver package and parasitic as observed on the scope with reference CTLE with gain of 9 dB
  - The equalized eye opening at the actual slicer typically ~25% less due to the RX package, ESD, and DC blocks
  - Hot transmitter has comparable performance to fast transmitter having 25% less amplitude
  - As the channel loss increases >12 dB fast TX start performing better
  - Trading off transmitter Tr/Tf, jitter, and amplitude is well worth it
- CAUI-4 chip to chip could support up to 15 dB assuming TX FFE and RX CTLE having fast/low jitter or 800 mV driver and require improving receiver sensitivity
  - Current CAUI-4 chip to module TP1a limit is 100 mV
  - To support 13 dB channel TP5 eye opening will be ~ 90 mV
  - To support 15 dB channel TP5 eye opening will be ~ 60 mV.

Thank You