CAUI-4 Ad hoc

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Agenda

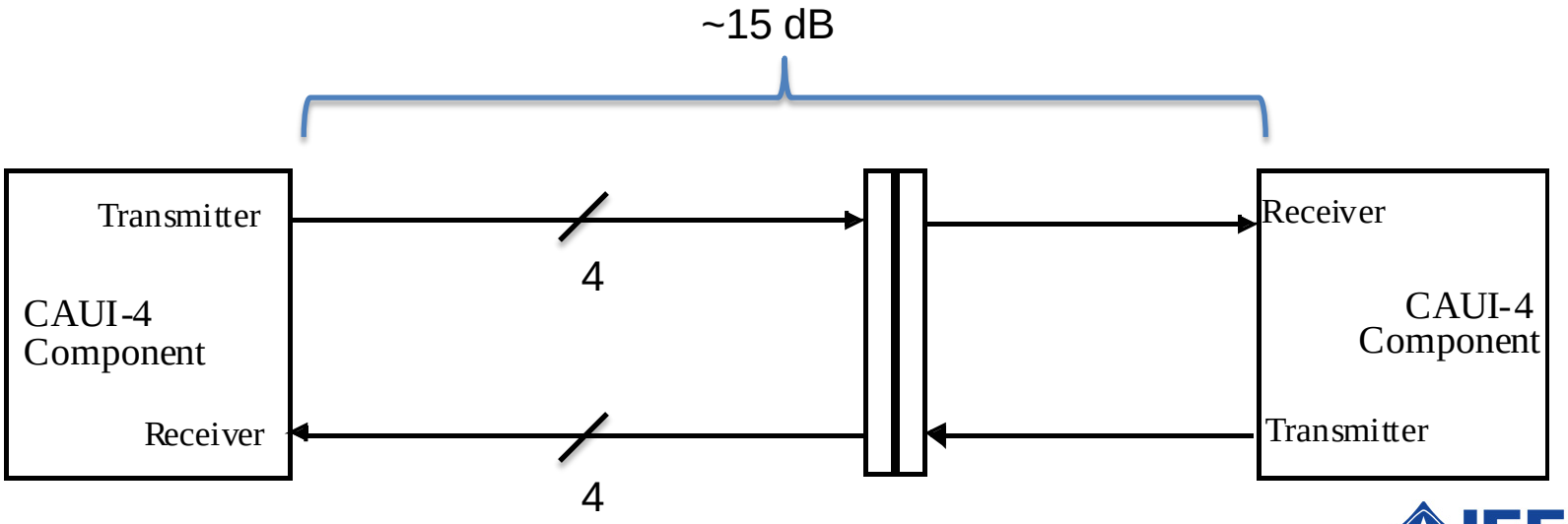
- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- **Adhoc objective: chip-chip baseline for March**
- Straw Poll Summary
- Review ghiasi_01_0313_caui
- Chip to chip draft baseline
  - Application space
    - Channel
    - Transmitter
    - Receiver
  - Areas of focus

Straw Poll

- I prefer to specify the transmitter for CAUI chip-chip using the methodology described in
  - A. 802.3ba CL 83A 3
  - B. 802.3bj CL93 / OIF CEI 28G SR 6
  - C. CAUI-4 chip-module (TP4) 1
  - D. CAUI-4 chip-module (with software channel) 2
- I prefer to specify the channel for CAUI chip-chip using the methodology described in
  - A. 802.3bj CL93 (COM) 10
  - B. OIF CEI 28G SR 1
- I prefer to specify the receiver / tolerance for CAUI chip-chip using the methodology described in
  - A. 802.3bj CL93 6
  - B. OIF CEI 28G SR 2
  - C. CAUI-4 chip-module 3

Application

- Chip to chip interface
  - Low power, low latency, AC coupled interface between ICs running at 4 x 25.78Gb/s
    - No FEC, No-DFE/or limited DFE (e.g., 1-tap or analog), no transmitter training
  - ~15 dB loss target with 1 connector (connector is optional)
    - Consistent with 25cm reach target
    - See http://www.ieee802.org/3/bm/public/nov12/palkert_02_1112_optx.pdf, http://www.ieee802.org/3/bm/public/nov12/ghiasi_03_1112_optx.pdf
    - Higher loss channels also under analysis to enable longer links



CAUI-4 chip to chip transmitter baseline

	KR4 (D1.4, TP0a)	CAUI-4 chip to chip Potential
Signaling rate, per lane	25.78125+/-100ppm	25.78125+/-100ppm
Differential peak-to-peak output voltage (max) with Tx disabled	30mV	30mVppd
Common Mode Voltage (max)	1.9V	1.9V
Common Mode Voltage (min)	0V	0V
Differential output return loss (min)	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=19GHz	RL(f)>= 6dB, 0.05<=f<=19GHz
Common-mode AC output voltage (max,rms)	12mV	12mV
Amplitude peak-to-peak (max)	1200mV	1200mV
Transition Time (20%-80%, min, no EQ)	8ps	8ps
Output Jitter (max) DJ RJ TJ	 0.15 (excluding DDJ) 0.15 0.28 (excluding DDJ)	 0.15 (with reference CTLE) 0.15 0.28 (BER TBD, with reference CTLE)
Output waveform	steady state voltage vf (max) 0.6 steady state voltage vf (min) 0.4 linear fit pulse peak (min) 0.8xvf normalized RMS linear fit error (max) 0.037	TBD (eye mask or other)
De-emphasis range	normalized coefficient step size (min) 0.0083 normalized coefficient step size (max) 0.05 precursor full scale range (min) 1.54 post cursor full scale range (min) 4	TBD (no Tx training or back channel)

CAUI-4 chip to chip channel baseline

Table 93–9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance	 C_d z_p C_p	TBD	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	TBD	 V V V
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient	$c(-1)$	TBD	—
Transmitter equalizer, post-cursor coefficient	$c(1)$	TBD	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	TBD	 dB dB dB
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.07	UI
Receiver additive Gaussian noise, RMS	σ_r	1	mV
Target detector error ratio	DER_0	TBD	—

93.9.1 Channel operating margin

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 93–9 shall be greater than or equal to 3 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

TBD

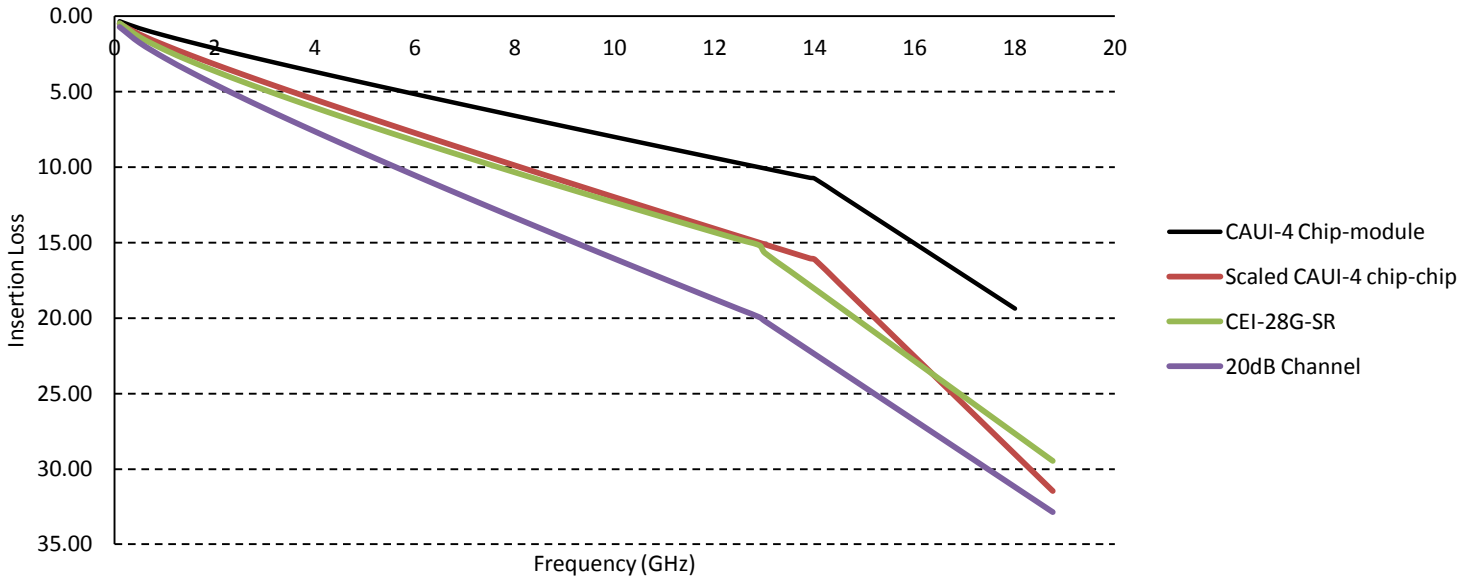
Modify to fixed setting or remove requirement

Modify to fixed setting

Increase the AC gain of CTLE?

1e-12 (or 1e-15) - TBD

CAUI-4 chip to chip informative channel characteristics



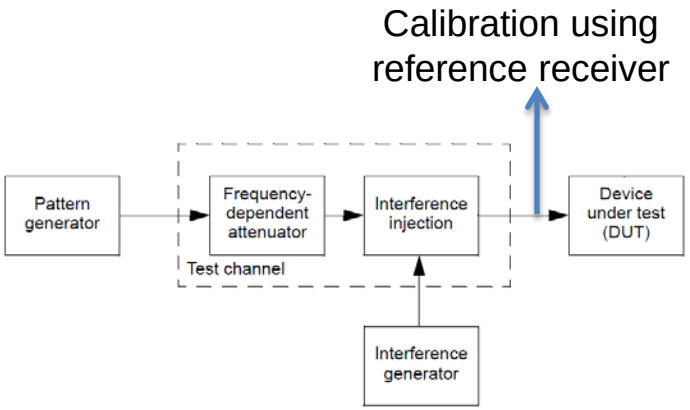
- Insertion Loss = 1.614 (0.075 + .537f^(0.5) + 0.566f) 0.01<=f<14
  1.614 (-18+2f) 14<=f<18.75
- Or insertion loss increase depending on simulation results with Ali's & Mike's channel (http://www.ieee802.org/3/bm/public/jan13/li_01_0113_optx.pdf)
- Return loss = TBD

CAUI-4 chip to chip receiver baseline

	KR4 (D1.4, TP5a)	MR	CAUI-4 chip to chip Potential
Differential Input Return loss (min)	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz
Differential to common mode input returnloss	RL(f) = 25-1.44f 0.05<=f<=6.95 15 6/95<f<=19		RL(f) = 25-1.44f 0.05<=f<=6.95 15 6.95<f<=19
Interference Tolerance	Table 93-7	Tx Jitter + SJ + channel (Table 11-13)	See table on next slide
Input amplitude (max)		1200	TBD

Receiver Interference Tolerance baseline

Parameter	Test values
Maximum BER*	TBD
Applied peak-to-peak sinusoidal jitter	5 x 105/f (100kHz<f<=10MHz) 0.05UI (10MHz<f<10 LB)
Applied broad band noise	TBD
Applied peak-to-peak random jitter	TBD
Minimum eye height after reference CTLE	TBD
Minimum eye opening after reference CTLE	TBD
Channel Insertion Loss at 12.89GHz	TBD
COM of ISI channel	TBD



* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Compliance points

- **See 93.8.2.1 Receiver test fixture from 802.3bj for TP5a**
- **See 93.8.1.1 Transmitter test fixture from 802.3bj for TP0a**

Minutes

- Reviewed patent policy
- Reviewed straw poll results
- Reviewed ghiasi_01_0313_caui
  - Discussion on big chip package loss could be more like 1.5dB
  - Could 6dB more CTLE and 6dB better sensitivity get the increased loss budget?
  - Eye mask
    - Don't want to constrain trade off on swing/rise-fall time
    - Action for Ali to build higher gain CTLE (~12-15dB)
  - Slide 14:
    - Normalize to include both package losses
  - Slide 15:
    - Clean up titles
- Reviewed baseline slides
  - Discussed future potential around DC coupling
  - Single ended output voltage range spec instead of common mode
- Changed interference test figure to 69A without feedback