CAUI-4 Ad hoc

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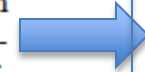
Agenda

- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- TBD for CAUI-4
  - Annex 83D:
    - COM value and parameters
    - Transmitter wave form specification (output jitter, waveform, de-emphasis)
  - Annex 83E
    - Brian Misek Presentation
    - Output total jitter (module and host)
    - Eye height (module and host)

COM TBD Summary

83D.4 CAUI-4 chip-chip channel characteristics

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 83D–5 shall be greater than or equal to TBD. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.
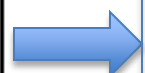
in 802.3bj:

3dB

Parameter	Symbol	Value	Units
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance	Cd	TBD	nF mm nF

Transmitter differential peak output voltage
     Victim
     Far-end aggressor
     Near-end aggressor
	A_v
	 A_f
	 A_n
		TBD	V
			 V
			 V

Transmitter equalizer, pre-cursor coefficient	$c(-1)$	TBD	— — —

Transmitter equalizer, post-cursor coefficient
     Minimum value
     Maximum value
     Step size
	$c(1)$	TBD	—
			 —
			 —

Continuous time filter, DC gain
     Minimum value
     Maximum value
     Step size
	g_{DC}	TBD	dB
			 dB
			 dB

C_d 2.5×10^{-4}
z_p 12
C_p 1.8×10^{-4}

A_v 0.4
A_f 0.4
A_n 0.6

$c(-1)$ -0.18 0 0.02

$c(1)$ -0.38 0 0.02

g_{DC} -12 0 1

COM CAUI-4 Considerations

- Consider having less spread between near end aggressor and victim
- Transmit equalizer
  - Transmitter planned to have 1 or 2 fixed settings
    - No Tx EQ, and Tx EQ enabled
    - Post cursor trades off with CTLE gain (therefore redundant)
    - Fixed pre-cursor can help for longer channels
- CTLE
  - Set gain as well as step size
  - CTLE in COM is defined as a two-pole, one-zero filter, where the poles are set at f_b (the Baud rate frequency) and $f_b/4$, and the zero is variable from $f_b/4$ and below. In this implementation, its effect is applied in the time domain, using a bilinear transform (function TD_CTLE).
  - May need higher order CTLE to enable better fit to insertion loss

TEMPORY COM update available

- Allows for 0 DFE

- Additional updates required to align with D2.1 of 802.3bj

- Will be posted

Chip-chip transmitter spec

Table 83D–1—CAUI-4 transmitter characteristics at TP1a

Parameter	Subclause Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
Maximum differential pk-pk output voltage when transmitter is disabled	83D.3.1.1	30	mV
Common-mode voltage (max)	83D.3.1.1	1.9	V
Common-mode voltage (min)	83D.3.1.1	0	V
Common-mode AC output voltage (max, RMS)	83D.3.1.1	12	mV
Amplitude peak-to-peak (max)	83D.3.1.1	1200	mV
Differential output return loss (min)	83D.3.1.2	Equation (83D–2)	dB
Common-mode output return loss (max)	83D.3.1.2	Equation (83D–3)	dB
Transition time (min, 20% to 80%)	83D.3.1.3	8	ps
Output Jitter (max) Random jitter[a] Deterministic jitter[b] Total jitter[c]	83D.3.1.4	0.15 with reference CTLE 0.15 0.28, with reference CTLE	UI
Output waveform	83D.3.1.5	TBD (eye mask or other)	
De-emphasis range	83D.3.1.6	TBD (no Tx training or back channel)	

[a]Random jitter at BER of 10^{-15}
[b]measured with reference CTLE per section TBD
[c]Total jitter at BER of 10^{-15}

Consider using 1/2dB reference CTLE used in 83E

Consider waveform measurement without emphasis if eye mask test

De-emphasis

	No De-emphasis	ON/OFF Setting	Multiple Setting
User control	Not needed	- Manual based on long/short channel	- Manual - (precise mechanism for setting could be assumed to be "system management function")
Spec	N/A	-Establish pre/post and tolerance -Far end eye mask based on reference channel (perhaps informative IL)	802.3bj / OIF CEI like

Need to iterate with COM parameters

Chip-module output jitter

OIF VSR starting point:

	Eye height@1E-15	Eye width@1E-15	Compliance point
Host	95mVppd	0.46UIpp	TP1a
Module	228mVppd	0.57UIpp	TP4