Validation of VSR Module to Host link

- **Work done for OIF and presented in OIF2013.170.4 to close comment on VSR draft 9.**

Problem Statement

- **Much work has been done to ensure the host to module signal is specified.**

- **Less work was done on the module to host.**

- **Adoption of eye targets has not changed as methodology has changed**

- **Resulting in Over Stress host Rx test**

- **There is needed a revisit of this part of the specification.**

Problem Statement Horizontal Stressor

- **2012.033.00 Hamid et all Define Test implemented in rev6**
- **Test was to have input at TP4a to be:**
  - RJ=.15UI, TJ=.28UI as in the informative Tx spec.
- **From 2011.270.01 Ghiasi did the baseline simulations that led to the summary below**
- **"Measured with PN31 or could be approximated with PN15**
  - TJ=0.34 UI @ BER 1E-15, J2=0.2 UI, and VECP=6 dB
  - Eye mask coordinate at 1E-15 X1=0.19 UI, X2=0.5 UI, Y1=120, Y2=300 mV"
- **Did not have CTLE applied to TP4.**
- **Applying CTLE will increase EH and as such more RJ is needed to close it back down**
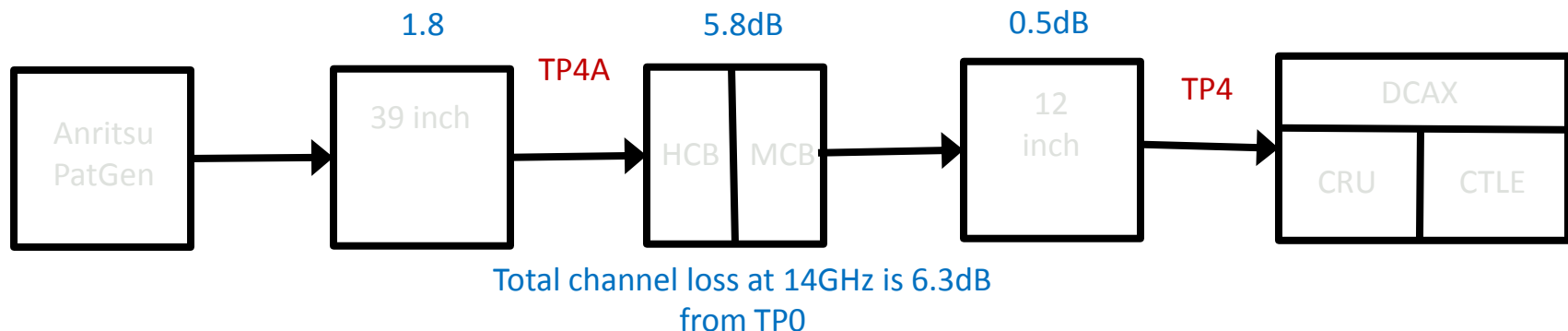
Problem Statement Vertical Stressor

- **VEC introduced in** oif2011.418.01.pptx

- **Measured with CTLE applied**

- **From Rev9: "At TP4 passing is defined as a single equalizer setting that meets the EH15, EW15 and VEC specifications"**

- **Comment to Rev8 Added VEC must be met and can be construed that the host test must meet it also.**

AvaGO
T E C H N O L O G I E S

Work Done Since Initial Comment

- **Identified Crosstalk impairment added to the module output but never verified the impact on TP4.**

- **Karl Muth did an excellent simulation on the Module Output at TP4 and Tp5. See OIF2013.198.04**

- **Lab measurements of TP4A, TP4 and TP5 completed.**

TP4A/TP4 Test Bench Setup

- **Anritsu Pattern Gen and 39 inch cable form "Module" TP0 signal at TP4A that is calibrated to Table 13-9**

- **TJ=280mUI, RJ=150mUI, SJ added as needed.**

- **Vamplitude=600mV**

	1.8		5.8dB		0.5dB		

Anritsu PatGen → 39 inch → **TP4A** HCB | MCB → 12 inch → **TP4** DCAX / CRU | CTLE

Total channel loss at 14GHz is 6.3dB
from TP0

Avago
TECHNOLOGIES

TP4A Test Bench Setup

- **Anritsu Pattern Gen and 39 inch cable form "Module" TP0 signal that is calibrated to Table 13-9**

- **TJ=280mUI, RJ=150mUI, SJ added as needed.**

- **Vamplitude=600mV**
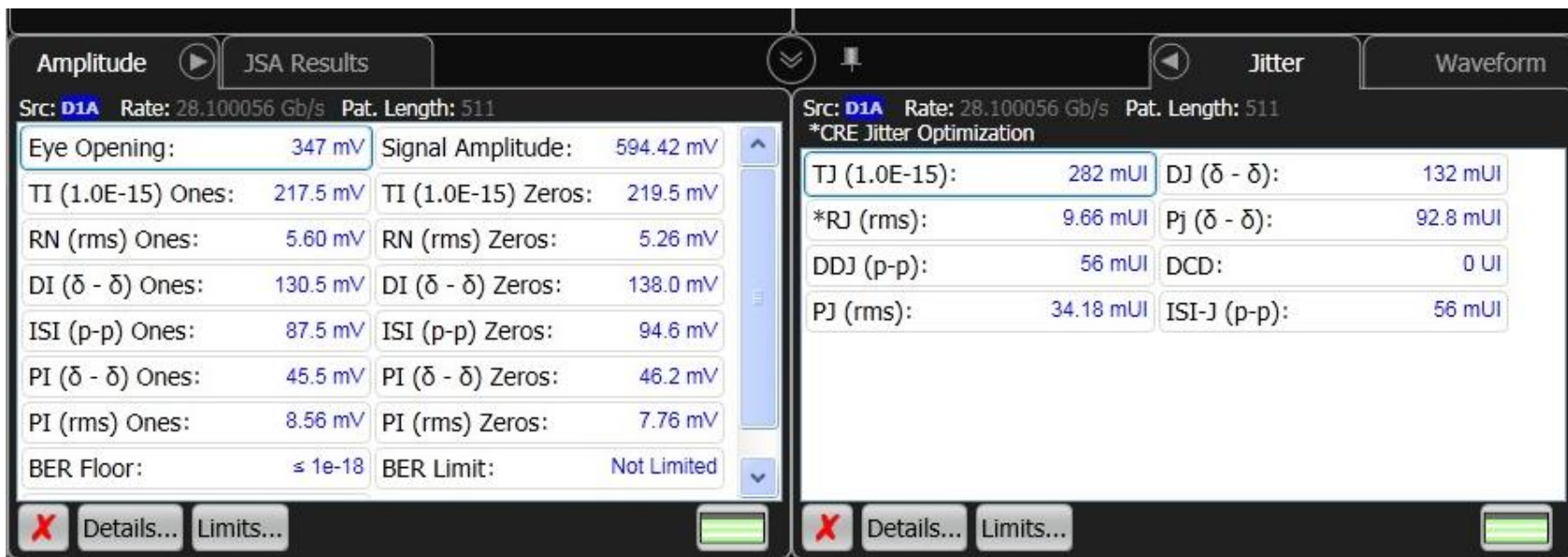
TP4 with 2dB of CTLE and TP0 stress

- **Channel Loss**

- **6.3dB**

- **Spec 5dB**

- **EW15=634mUI**

- **Spec 570mUI**

- **EH15=180mV**

- **Spec 228mV**

- **VEC= 4.9dB**

- **Spec 6.5dB**

TP4 with 2dB of CTLE and full stress

- **Channel Loss**

- **6.3dB**

- **Spec 5dB**

- **EW15=575mUI**

- **Spec 570mUI**

- **EH15=228mV**

- **Spec 228mV**

- **VEC= 4.7dB**

- **Spec 6.5dB**

- **Note: requires launch amplitude boost to meet EH15**
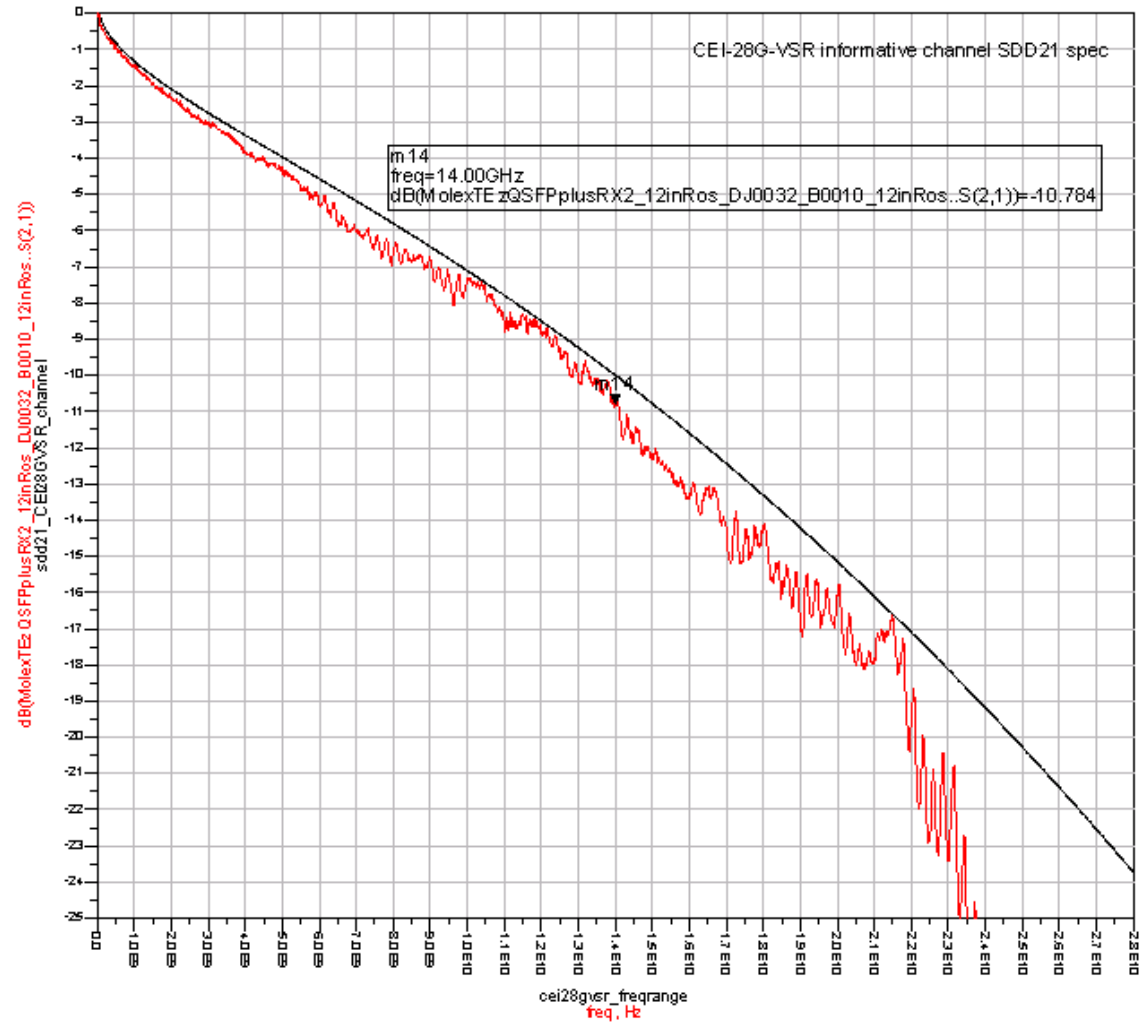
TP5 Test Bench Setup
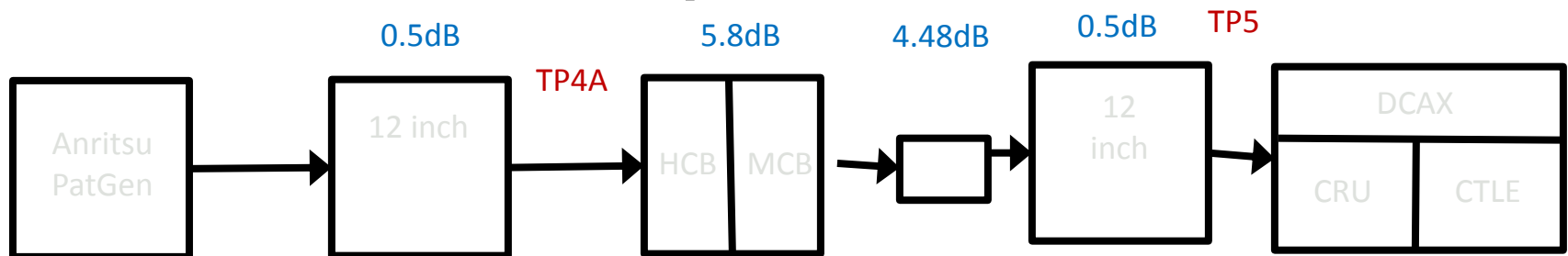
Total channel loss at 14 GHz is
10.78dB from TP0
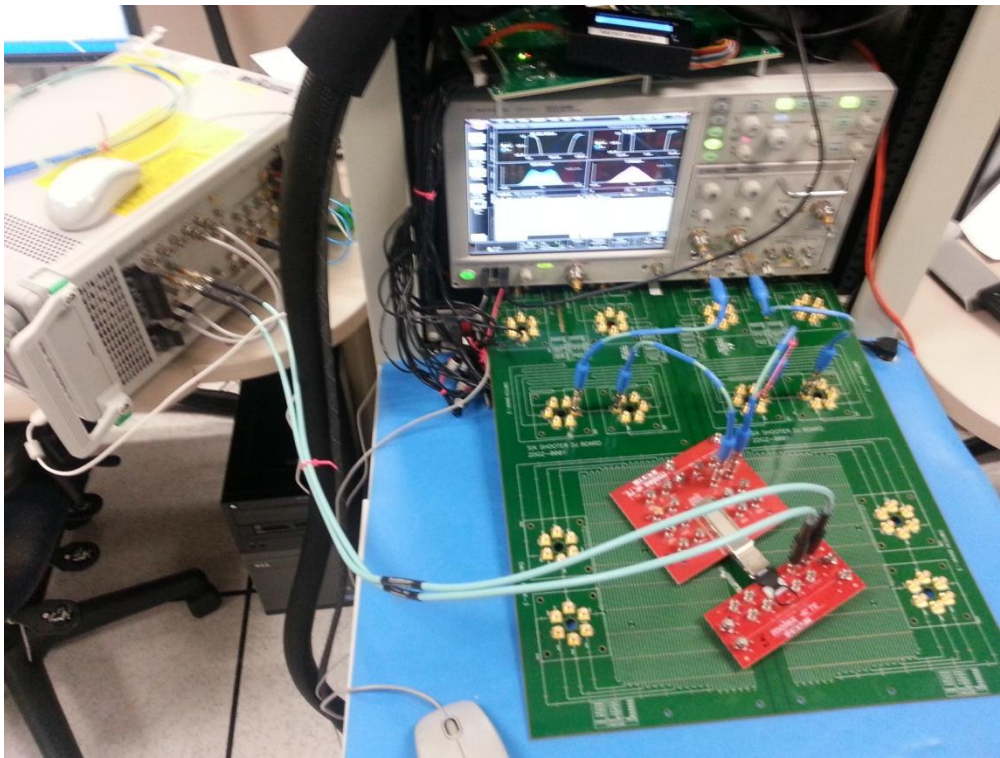
TP4-TP5 test channel

- **Channel Loss**

- **10.78dB**

- **Spec 10dB**

TP5 with 6dB of CTLE and full stress

- **Channel Loss**
  - 10.78dB
  - Spec 10dB
- **EW15=542mUI**
  - Target 460mUI
- **EH15=159mV**
  - Target 95mV

What if

- **EH15 is larger then spec. What is causing this?**

- Test point is 1.3 dB further into the channel then spec calls for.

- Additional RJ is modulated into vertical eye closure which require more amplitude.

- **What happens if we do not allow EH15 to be increased at TP4?**

TP4 with 2dB of CTLE and Jitter only stress

- **Channel Loss**
  - 6.3dB
  - Spec 5dB
- **EW15=566mUI**
  - Spec 570mUI
- **EH15=197mV**
  - Spec 228mV
- **VEC=4.37dB**
  - 6.5dB

TP5 with 6dB of CTLE and Jitter stress only

- **Channel Loss**
  - 10.78dB
  - Spec 10dB
- **EW15=534mUI**
  - Target 460mUI
- **EH15=134mV**
  - Target 95mV

Conclusions from Bench Measurements

- **Fully TP4 EW15 stressed eyes with additional amplitude cause compliant host receiver eye at TP5**

  - EW15=542mUI measured vs 460mUI spec.

- **Fully TP4 EW15 stressed eyes with no additional amplitude cause compliant host receiver eye at TP5**

  - EW15=534mUI measured vs 460mUI spec.

Conclusions from Muth Module Simulations

- **With out crosstalk, the module output was too relaxed as initially thought.**

- **Page 14 OIF2013.198.04**

  - Simulated EW=695mUI, EH=286mV, VEC=2.8dB

  - Spec   EW=570mUI EH=228, VEC=6.5dB

- **When 3.9mVrms of crosstalk added into the simulation and the module blocking cap and a reasonable package for the CDR**

- **Page 28 OIF2013.198.04 good package result**

  - Simulated EW=565mUI, EH=220mV, VEC=5.17dB

  - Spec EW=570mUI EH=228, VEC=6.5dB

Avago
TECHNOLOGIES

Recommendations

- **Change the crosstalk stress from 5.2 to 3.9mVrms to agree with the rest of the spec having the max launch amplitude be 900mV for VSR not the 1200mV that was used for copper cables and was the basis for the 5.2mV in the spec.**

- **Change VEC to a max of 5.5dB**

- **Add text to line page 21 line 19 that states**

- **" A compliant host stress is one that meet EW15, EH15 and has a VEC in the range of 4 to 5.5 dB."**