CAUI-4 Ad hoc

Ryan Latchman, MACOM

Agenda

- Patent Policy: This meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Presentations:
  - 83D proposed modifications
    - Continuous jitter tolerance SJ curve
    - CTLE for COM
  - 83E proposed modifications
    - Adaptive CTLE option
  - Comments from D3.0
- Next meeting: TBD

83D Proposed Modification

- Continuous jitter tolerance SJ curve added to interference tolerance test per 88-13

Table 83D–4—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.2.2	Equation (93-3)	dB
Differential to common mode input return loss	93.8.2.2	Equation (93-5)	dB
Interference tolerance	83D.3.3.1	Table 83D–6	—
~~Jitter tolerance[a]~~	~~93.8.2.4~~	~~Table 93-7~~	~~—~~

[a]When referencing 93.8.2.4 the following modifications are required: Test transmitter shown in Figure 93-12 meets 83D.3.1 specifications, test channel meets the requirements of the interference tolerance test channel using Test 2 values from Table 83D–6, bit error ratio better than 10^{-15} for the receiver jitter tolerance test.

Removed separate Jitter Tolerance Test row

83D.3.3.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 83D–6. The interference tolerance test uses the method described in Annex 93C as specified by 93.8.2.3, with the following exceptions:

a) The parameters in Table 83D–6 replace the parameters in Table 93-6.

b) The transmitter taps are set via management to the optimal transmitter equalizer settings described in 83D.3.1.1.

c) Sinusoidal jitter is added to the test transmitter by modulating the clock source.

Added SJ as one of the differences between 83D and 93

83D Proposed Modification

- Continuous jitter tolerance SJ curve added to interference tolerance per 88-13

Table 83D–6—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Bit error ratio[ab]	—	10^{-15}	—	10^{-15}	—
Applied pk-pk sinusoidal jitter	Table 88-13		Table 88-13		
Insertion loss at 12.89 GHz[c]	—	20	—	10	dB
Coefficients of fitted insertion loss[d]					
a_0	-1	2	-1	1	dB
a_1	0	2.937	0	0.817	dB/GHz$^{1/2}$
a_2	0	1.599	0	0.801	dB/GHz
a_4	0	0.03	0	0.01	dB/GHz^2
RSS_DFE4	0.05	—	0.025	—	—
COM including effects of broadband noise	—	2	—	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3
[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard
[c]Measured between TPt and TP5 (see Figure 93C-4)
[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz

Applied SJ per 88-13

83D Proposed Modification

- COM CTLE for DFE based Rx

Table 83D–7—Channel Operating Margin parameters *(continued)*

Parameter	Symbol	Value	Units
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	~~Table 83D–8~~ –12 0 1	dB
Continuous time filter, zero frequency	f_z	~~Table 83D–8~~ $f_b/4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	~~Table 83D–8~~ $f_b/4$ f_b	GHz

Table 83D–8—Reference CTLE coefficients

g_{DC}	f_{p1}	f_{p2}	f_z
-1	18.6	14.1	9.385
-2	18.6	14.1	8.937
-3	15.6	14.1	8.018
-4	15.6	14.1	7.861
-5	15.6	14.1	7.75
-6	15.6	14.1	7.67
-7	15.6	14.1	7.609
-8	15.6	14.1	7.566
-9	15.6	14.1	7.531
-10	15.6	14.1	7.503
-11	15.6	14.1	7.483
-12	15.6	14.1	7.466

83E Proposed Modification

83E.3.1.6 Host output eye width and eye height

Host output eye width is greater than 0.46 UI. Host output eye height is greater than 95 mV. Figure 83E–9 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 83E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.1.6.1. The recommended CTLE peaking value (which is also used for host output eye measurements) is provided to the module via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

Added text on use of recommended CTLE peaking

83E.3.4.2.1 Module stressed input test procedure

Two levels of frequency dependent attenuation are used for the module stressed input test: high loss, and low loss. For the high loss case, frequency dependent attenuation is added such that from the output of the pattern generator to TP1a is 10.25 dB loss at 12.89 GHz. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. For the low loss case, discrete frequency dependent attenuation is removed such that from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. In both the low loss and high loss cases, the module under test is provided with the reference CTLE setting used to meet eye width and eye height requirements via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). The module under test ~~is evaluated with~~ shall meet the BER requirement as described in Table 83E–7 using three *Recommended_CTLE_value* values for both the high loss test and low loss test. These are: a) the CTLE setting used to meet eye width and eye height requirements, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2. Modules may optionally elect not to use the *Recommended_CTLE_value*.

Explicit requirement to meet +/-1dB (add PICS)

Explicit optional use of Recommended_CTLE_value

83E PICS Proposed Modification

83E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83E.1	Four independent data paths in each direction	M	Yes [ ]
ADR	Adaptive receiver	83E.3.4.2.1	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

Add option to PICS

Comment 20196 on D2.2

83E.3.4.1 Input bit error ratio

The CAUI-4 module input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.4.2.

- Discuss potential wording proposals:

  "The CAUI-4 module input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.4.2."

  To

  "The module CAUI-4 receiver is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.4.2."

  Or

  ""The CAUI-4 module input characteristics and stressed electrical input signal are defined by 83E.3.4.2 at a bit error ratio (BER) of 10-15."

Verify references to 802.3bm

- Add comment to update output jitter subclause reference in table 83D-1 to 93.8.1.7

Table 83D–1—CAUI-4 transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	93.8.1.2	25.78125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
Common-mode AC output voltage (max, RMS)	93.8.1.3	12	mV
Differential output return loss (min)	93.8.1.4	Equation (93-3)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93-4)	dB
Output waveform[a] Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 93.8.1.5.2 93.8.1.5.2 93.8.1.5.2 83D.3.1.1 83D.3.1.1	 0.6 0.4 0.71 x v_f Table 83D–2 Table 83D–3	 V V V — —
Signal-to-noise-and-distortion ratio (min)	93.8.1.6	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak[b] Effective total uncorrelated jitter, peak-to-peak[bc]	92.8.3.9 Update to 92.8.3.8	 0.035 0.1 0.26	 UI UI UI

[a]The state of the transmit equalizer is controlled by management interface.
[b]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.9.2 except that the range for fitting $CDFL_i$ and $CDFR_i$, as defined in 92.8.3.9.2 c), shall be from 10^{-4} to 2.5×10^{-3}
[c]Effective total uncorrelated jitter, peak-to-peak is specified to a 10^{-15} probability

Minutes

- Attendees:
  - Mike Dudek, Qlogic
  - Ali Ghiasi, Ghiasi Quantum
  - Adam Healey, Avago
  - Peter Anslow, Ciena
  - Dan Dove, Dove Networking
  - Ryan Latchman, MACOM
  - Adee Ran, Intel
  - John Petrilla, Avago
  - Jonathan King, Finisar
- Minutes
  - Patent policy
  - Reviewed proposed changes to D3.0
    - Updated text to address comment 20196 on D2.2 still in development
      - Two proposals included on slide 8, additional discussion required before next meeting
- Next meeting: 10am PT Friday June 6th