CAUI-4 Ad hoc

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Agenda

- Patent Policy: The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-to-module discussion
- Chip-to-chip discussion

Chip to module

- Module input compliance test:
  - add low loss test remove frequency dependent attenuator
  - Total loss between limiter and TP1a is the mated MCB / HCB loss
    - 2.86 to 4.6dB loss at 12.89GHz
    - Keep same EH/EW targets
- Host output compliance test:
  - 2) Apply respective reference receiver CTLE to captured signal. Any single CTLE setting which meets both eye width and eye height requirements is acceptable for the module compliance . For host compliance, the CTLE peaking in the reference receiver shall be set at one of three values. These are: a) the recommended CTLE peaking value provided by the host, b) the value 1 dB higher if present in Table 83E-2 and c) the value 1 dB lower if present in Table 83E-2. Any of the three CTLE settings that meets both the eye width and eye height defined in Table 83E-1 is acceptable.

    The recommended CTLE peaking value is provided to the module via the variable *Recommended_CTLE_value.* If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.88c).
- Next: mechanism for host to provide recommended CTLE value
  - Discussing with SFF and CFP MSA in attempt to ensure alignment
    - SFF QSFP: 0 – 10dB using 4 bits register (address 234/5) – Fibre Channel range
    - CFP MSA 7 bits with fine control
  - Assign MDIO registers per Clause 45

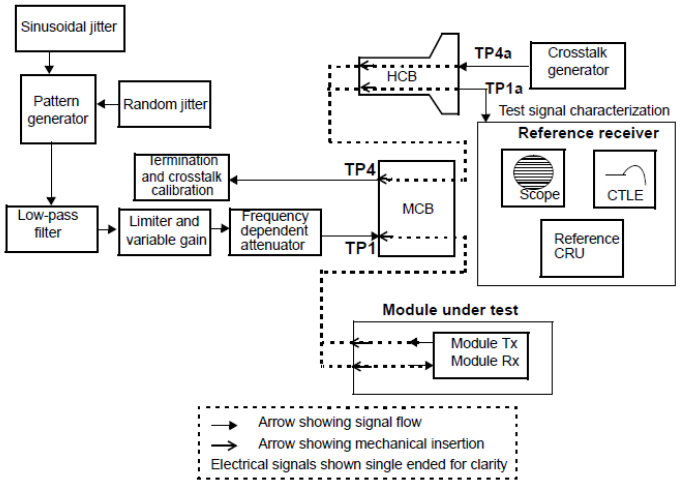


Figure 83E–15—Example module stressed input test

MDIO

45.2.1 PMA/PMD registers

Change the identified reserved row in Table 45-3 (as modified by IEEE Std P802.3bj-201x) and insert a new row for register 1.169 immediately below the changed row as follows:

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.167 through 1.~~169~~168	Reserved	
1.169	CAUI-4 chip-to-module recommended CTLE	45.2.1.88c

Insert 45.2.1.88c after 45.2.1.88b (as inserted by IEEE Std P802.3bj-201x) as follows:

45.2.1.88c CAUI-4 chip-to-module recommended CTLE register (Register 1.169)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–67c. The value stored in this register corresponds to the CTLE peaking value (see 83E.3.1.6.1) recommended by the host (and used in the evaluation of host output compliance). The module may optionally use this information to adjust its CTLE setting.

Table 45–67c—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.169.15:6	Reserved	Value always 0, writes ignored	RO
1.169.5:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	RO
1.169.0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read only

Reference CTLE

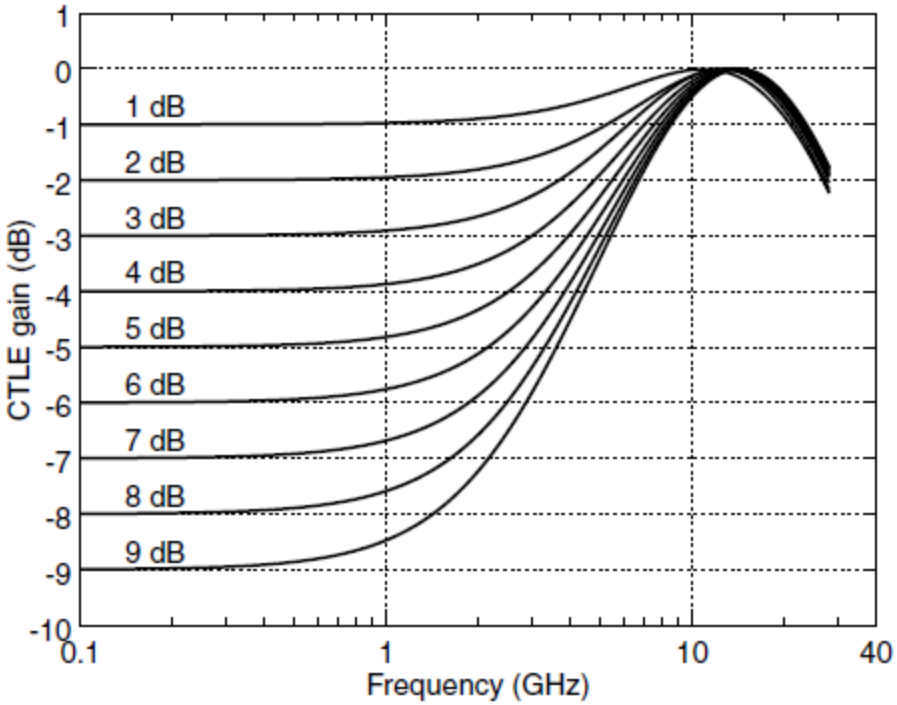
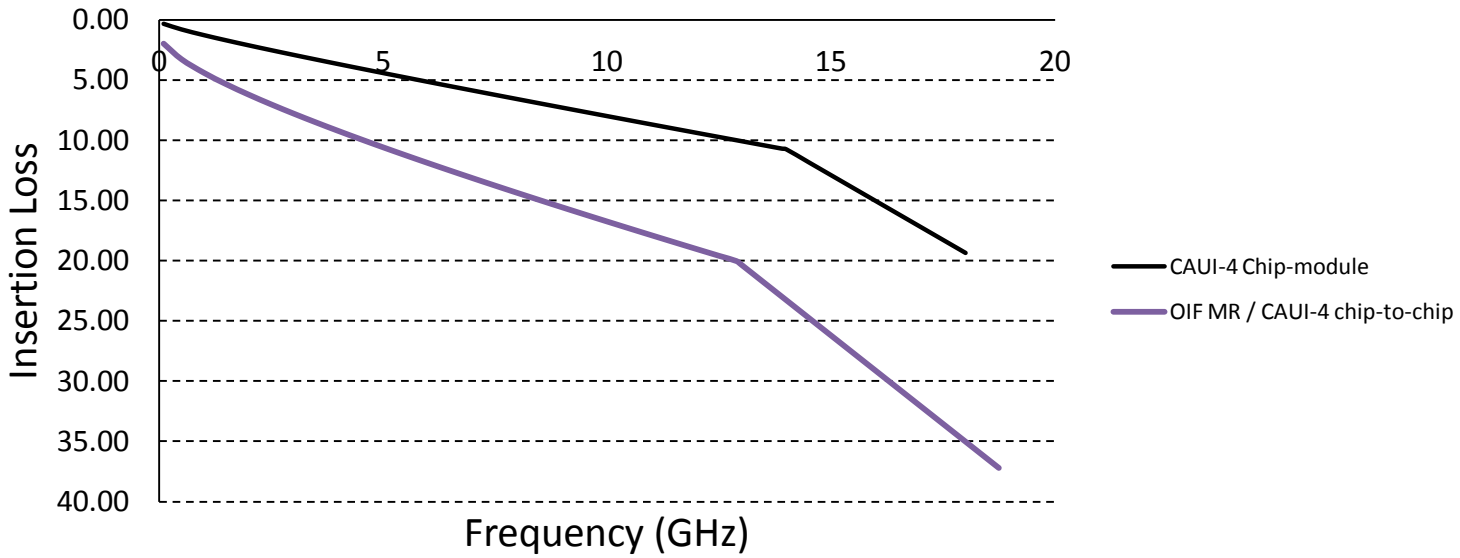


Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic

Chip-chip

- 20dB informative loss budget (COM normative with DFE updates)



Chip to Chip Discussion

- COM:
  - Mechanism available in COM to restrict channels which may result in a receiver having MTTFPA
    - Limit tap magnitudes, number of taps
    - See mellitz_01_101413_CAUI

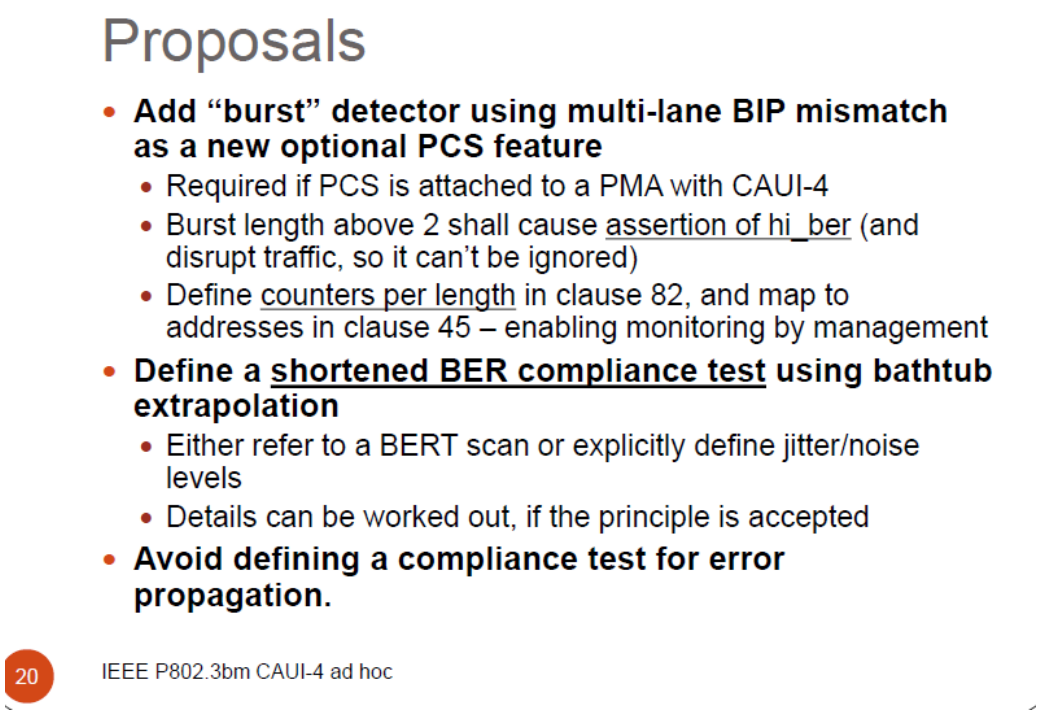
Table 83D–7—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Transmitter package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_{dt} z_{pt} C_{bt}	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Receiver package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_{dr} z_{pr} C_{br}	 0 0 0 update	 nF mm nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient	$c(-1)$, $c(0)$, $c(1)$	Table 83D–8	 — — —
Transmitter equalizer, post-cursor coefficient	$c(-1)$, $c(0)$, $c(1)$	Table 83D–9	 — — —
Continuous time filter, DC gain	*CTLE*	Table 83D–6	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 Av A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	
Transmitter signal to noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	~~0~~ 5	UI
Normalized DFE coefficient magnitude limit	b_{max}	~~1~~ 0.3	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2×10^{-4}	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—

mellitz_01_101413_CAUI

Chip to Chip Discussion

- Mechanism to monitor MTTFPA issue in field which takes into account entire link
  - New optional feature in PCS that detects bursts and cause an assertion of hi_ber
  - Changes to clause 82 and 45
    - ran_01_101413_CAUI
      - » (updated proposal will be made at next CAUI meeting)



Proposals

- **Add "burst" detector using multi-lane BIP mismatch as a new optional PCS feature**
  - Required if PCS is attached to a PMA with CAUI-4
  - Burst length above 2 shall cause assertion of hi_ber (and disrupt traffic, so it can't be ignored)
  - Define counters per length in clause 82, and map to addresses in clause 45 – enabling monitoring by management
- **Define a shortened BER compliance test using bathtub extrapolation**
  - Either refer to a BERT scan or explicitly define jitter/noise levels
  - Details can be worked out, if the principle is accepted
- **Avoid defining a compliance test for error propagation.**

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Next Meeting

- December 9th 9am PT
- Chip to chip:
  - Transmitter update
  - Receiver interference tolerance test
  - CL82 and CL45 changes for chip to chip
- Chip to module:
  - Start reviewing potential Annex 83E changes
  - CL45 changes

Minutes

- Attendees
  - Jeffery Maki, Juniper
  - Adee Ran, Intel
  - John Petrilla, Avago
  - Domenico De Simone Alcatel Lucent
  - Mauro Zontini Alcatel Lucent
  - Sam Sambasivan ATT
  - Ed Ulrichs Source Photonics
  - Peter Anslow Ciena
  - Richard Mellitz Intel
  - Charles Moore, Avago
  - Rick Rabinovich, Alcatel Lucent
  - Mike Dudek Qlogic
  - Vinu Arumugham, Cisco
  - Ali Ghiasi
  - Mike Li, Altera
  - David Brown Semtech
- Chip-module
  - Implementation should include text that module must pass input stress with reference CTLE value established from test signal calibration +/- 1dB
  - Module may optional use this information
  - Question raised on symmetric SJ template (does the SJ template need to change)
    - Further presentation material requested
- Chip-chip
  - Informative loss: use similar loss equation as MR assuming 100GbE bit rate (COM is normative spec)
  - Updated MTTFPA resolution to be proposed at next CAUI-4 ad hoc meeting