CAUI-4 Chip – Module Draft Baseline

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CAUI-4 Host Transmitter

	CR4 (D1.2, TP2)	VSR (7.2, TP1a)	CAUI-4 Chip-Module Potential
Signaling rate, per lane, Gb/s	25.78125 +/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak output voltage (max) with Tx disabled	35mV		35mV
Common Mode Voltage Range	0 - 1.9V	-0.3V (min) to 2.8V (max)	-0.3V (min) to 2.8V (max)
Differential output return loss (min)	SDD22>= 12-0.5f for 0.01<=f<=8 SDD22>= 5.65-9.71$\log_{10}$(f/14)	SDD22 < -11dB for 0.05<f<fb/7 SDD22 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD22>= 12-0.5f for 0.01<=f<=8 GHz SDD22>= 5.65-9.71$\log_{10}$(f/14) for 8<f<= 25 GHz
Common-mode AC output voltage (max,rms)	30mV	17.5mV	17.5mV
Amplitude peak-to-peak (max)	1200mV	900mV	900mV
Output total jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	0.54UIpp @ 10^{-15} Measured using CTLE	0.52UIpp @ 10^{-12} Measured using reference CTLE
Eye height peak-to-peak (min)		100mVppd @ 10^{-15} Measured using ref CTLE	106mVppd @10^{-12} Measured using ref CTLE
Differential termination mismatch (max)		10%	10%
Common to differential mode conversion (max)		SDC22 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC22 < -15 dB for fb/2<f<fb	SDC22 < -25 + 20*(f/25.78) dB for 0.05<f<12.89 GHz SDC22 < -15 dB for 12.89<f<25.78 GHz
Transition time (min, 20/80%)		10ps	10ps

CAUI-4 Module Receiver

	VSR (7.2, TP1)	CAUI-4 Chip-Module Potential
Bit Error Ratio	10^{-15} or better per lane	10^{-12} or better
Signaling rate, per lane, Gbps	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	35.65ps - 51ps	38.787879ps
Differential peak-to-peak input amplitude tolerance	900mVppd	900mVppd
Differential termination mismatch (max)	10%	10%
Differential input return loss (max)	SDD11 < -11dB for 0.05<f<fb/7 SDD11 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD11>= 12-0.5f for 0.01<=f<=8 GHz SDD11>= 5.65-9.71$\log_{10}$(f/14), for 8<f<= 25 GHz
Common to differential mode conversion (max)	SDC11 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC11 < -15 dB for fb/2<f<fb	SDC11 < -25 + 20*(f/25.78) dB for 0.05<f<12.89 SDC11 < -15 dB for 12.89<f<25.78 GHz

CAUI-4 Module Transmitter

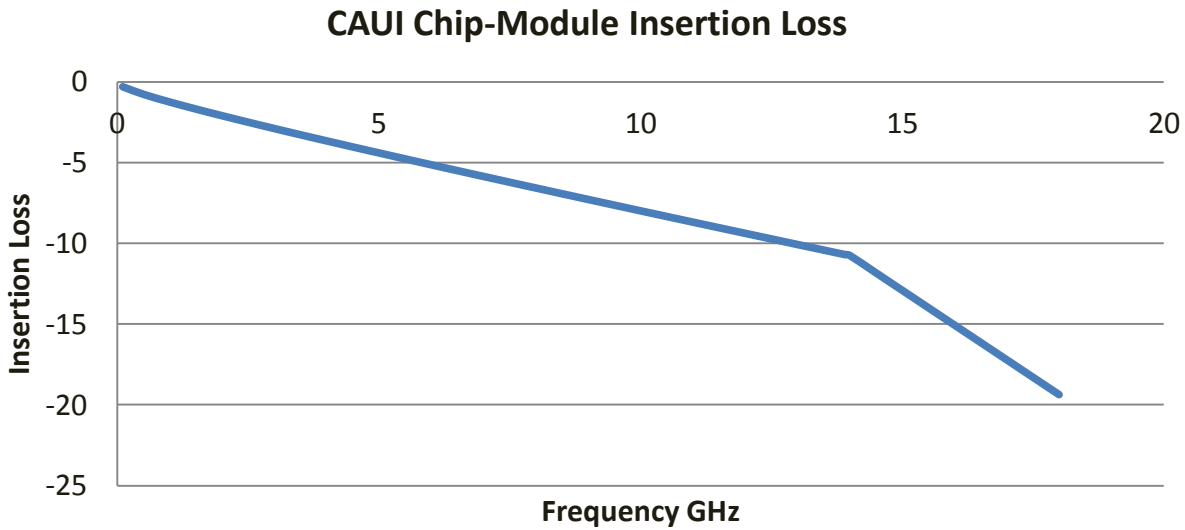
	VSR (7.2, TP4)	CAUI-4 Chip-Module Potential
Signaling rate, per lane, Gbps	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	35.65ps - 51ps	38.787879ps
Differential voltage peak-to-peak (max)	900mV	900mV
Common-mode noise (rms, max)	17.5mV	17.5mV
Differential termination mismatch (max)	10%	10%
Differential output return loss (max)	SDD22 < -11dB for 0.05<f<fb/7 SDD22 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD22>= 12-0.5f for 0.01<=f<=8 GHz SDD22>= 5.65-9.71$\log_{10}$(f/14), for 8<f<= 25 GHz
Common mode to differential conversion return loss (max)	SDC22 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC22 < -15 dB for fb/2<f<fb	SDC22 < -25 + 20*(f/25.78) dB for 0.05<f<12.89 GHz SDC22 < -15 dB for 12.89<f<25.78GHz
Transition time 20/80 (min)	9.5ps	9.5ps
Vertical eye closure (max)	6.5dB	6.5dB
Output Total Jitter (max)	0.43UI at 10^{-15}	0.41UI at 10^{-12}
Eye height peak-peak (min)	240mV at 10^{-15}	246mV at 10^{-12}

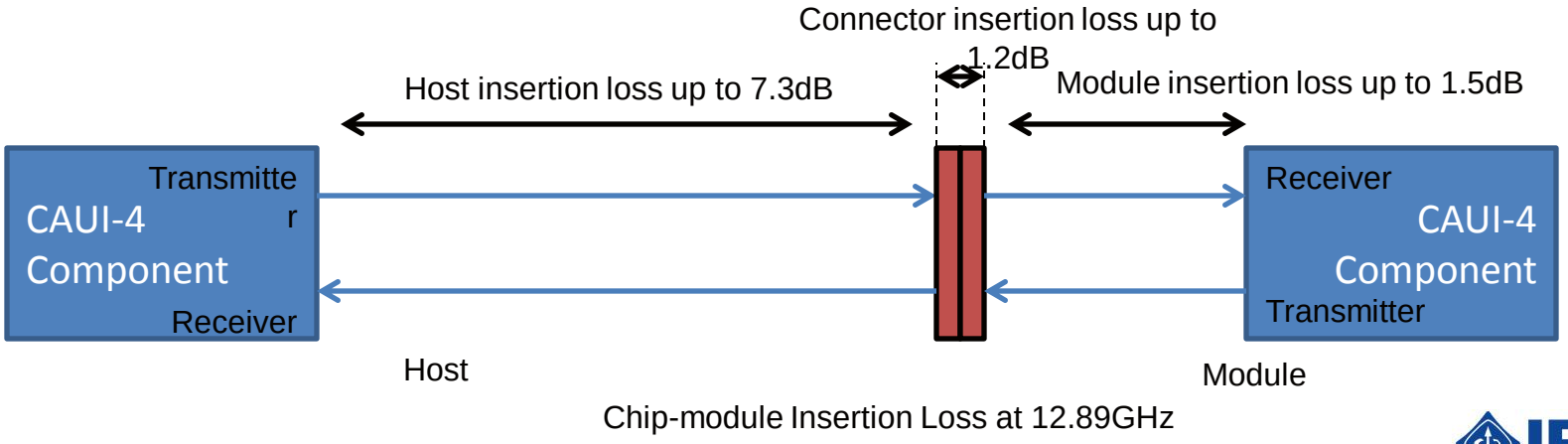
CAUI-4 Host Receiver

	CR4(1.2TP3)	VSR (7.2, TP4a)	CAUI-4 Chip-Module Potential
Bit Error Ratio	10^{-12} or better	10^{-15} or better per lane	10^{-12} or better
Signaling rate, per lane, Gbps	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak input amplitude tolerance / overload differential voltage pk-pk	1200mVppd (max)	900mVppd (min)	900mVppd
Differential input return loss (min)	SDD11>= 12-0.5f for 0.01<=f<=8 SDD11>= 5.65-9.71$\log_{10}$(f/14), for 8<f<= 25 GHz	SDD11 < -11dB for 0.05<f<fb/7 SDD11 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD11>= 12-0.5f for 0.01<=f<=8 SDD11>= 5.65-9.71$\log_{10}$(f/14) for 8<f<= 25 GHz
Differential to common mode input return loss (min)	10, 0.01≤ f ≤ 25 GHz	SDC11 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC11 < -15 dB for fb/2<f<fb	10, 0.01≤ f ≤ 25 GHz
Stress receiver test (min)	See 92.8.4.2	See Section 1.3.10.2.1	
Differential termination mismatch (max)		10%	10%

CAUI-4 Channel Insertion loss

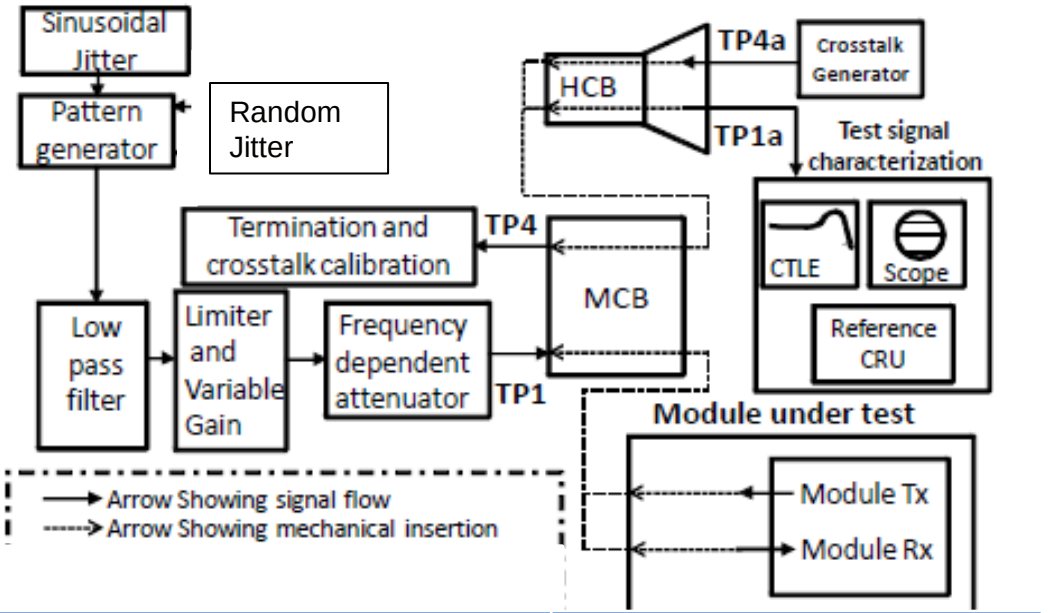
$$Insertion_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f \le 18.75 \end{cases} \text{ (dB)} \qquad (92\text{–}4)$$





Chip-module Insertion Loss at 12.89GHz

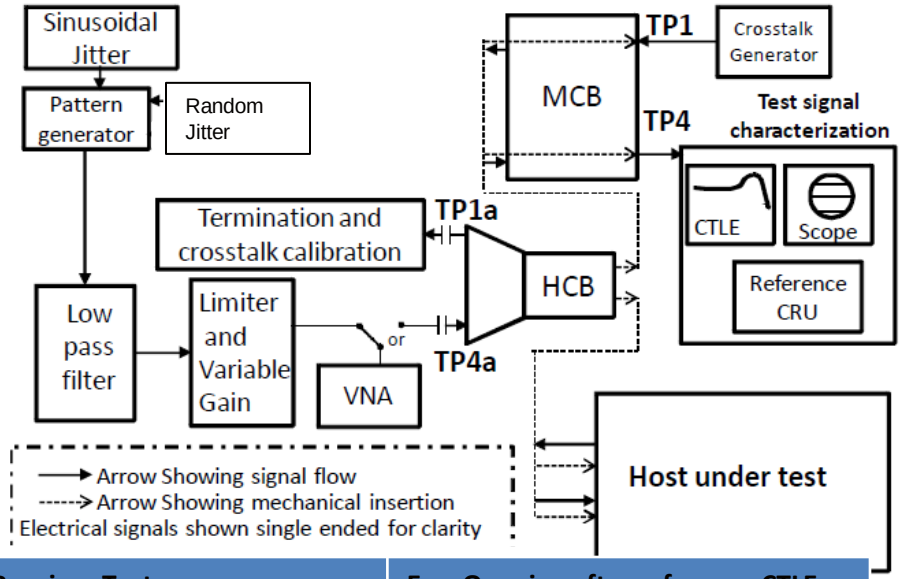
Module Stress Receiver Test



Module Stress Receiver Test	Eye Opening after reference CTLE
Minimum Total Input Jitter Tolerance	0.51UIpp 10^{-12}
Applied peak-peak sinusoidal jitter	5 x 10^5/f (100kHz<f<=10MHz) 0.05UI (10MHz<f<10 LB)
Eye Height	106mVpp

- Reference CRU and reference software CTLE used to calibrate the stressed receiver test signal at TP1a using a PRBS9 pattern.
- The crosstalk source is asynchronous to the main pattern generator. The crosstalk pattern is PRBS31. Target value: 900mVppd amplitude, 9.5ps 20-80% rise/fall). All lanes active.
- Module input test signal: DJ is added to a clean pattern by adding SJ, low pas filtering and limiting function. Variable gain is used to adjust amplitude. RJ is added such that the output of the limiting function approximates TJ = 0.28UIpp, RJ = 0.15UIpp, DCD = 0.035UIpp
-Frequency dependent attenuator is added such that the output of the limiter to TP1a is 10.25dB loss at 12.89GHz
-Eye height and eye width are measured using software CTLE with optimal peaking setting (maxim eye width * eye height
- RJ and variable gain is adjusted to result in the minimum eye height and eye width

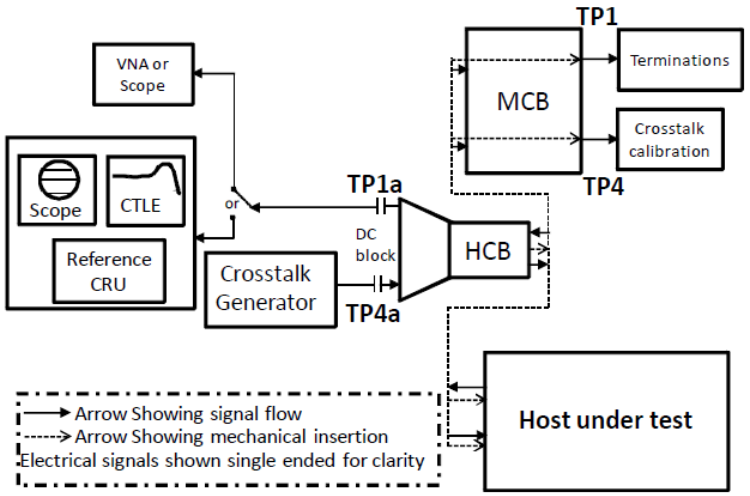
Host Stress Receiver Test

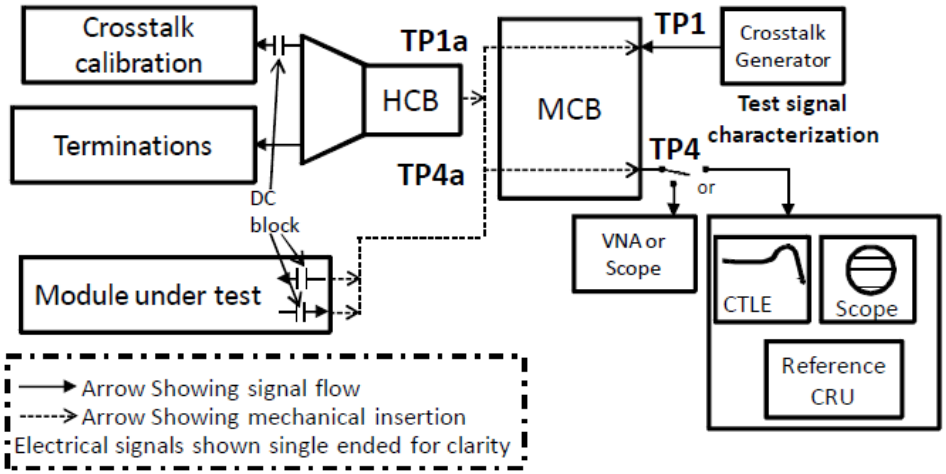


Host Stress Receiver Test	Eye Opening after reference CTLE
Minimum Total Input Jitter Tolerance	0.41UIpp 10^{-12}
Applied peak-peak sinusoidal jitter	5 x 10^5/f (100kHz<f<=10MHz) 0.05UI (10MHz<f<10 LB)
Eye Height	246mVpp

- Reference CRU and reference software CTLE used to calibrate the stressed receiver test signal at TP4 using a PRBS9 pattern.
- The crosstalk source is asynchronous to the main pattern generator. The crosstalk pattern is PRBS31. Target value: 900mVppd amplitude, 10ps 20-80% rise/fall). All lanes active.
-Host input test signal: DJ is added to a clean pattern by adding SJ, low pas filtering and limiting function. Variable gain is used to adjust amplitude. RJ is added such that the output of the limiting function approximates TJ = 0.28UIpp, RJ = 0.15UIpp, DCD = 0.035UIpp
-Eye height and eye width are measured using software CTLE with optimal peaking setting (maxim eye width * eye height
- RJ and variable gain is adjusted to result in the minimum eye height and eye width

Host / Module Output Waveform Test

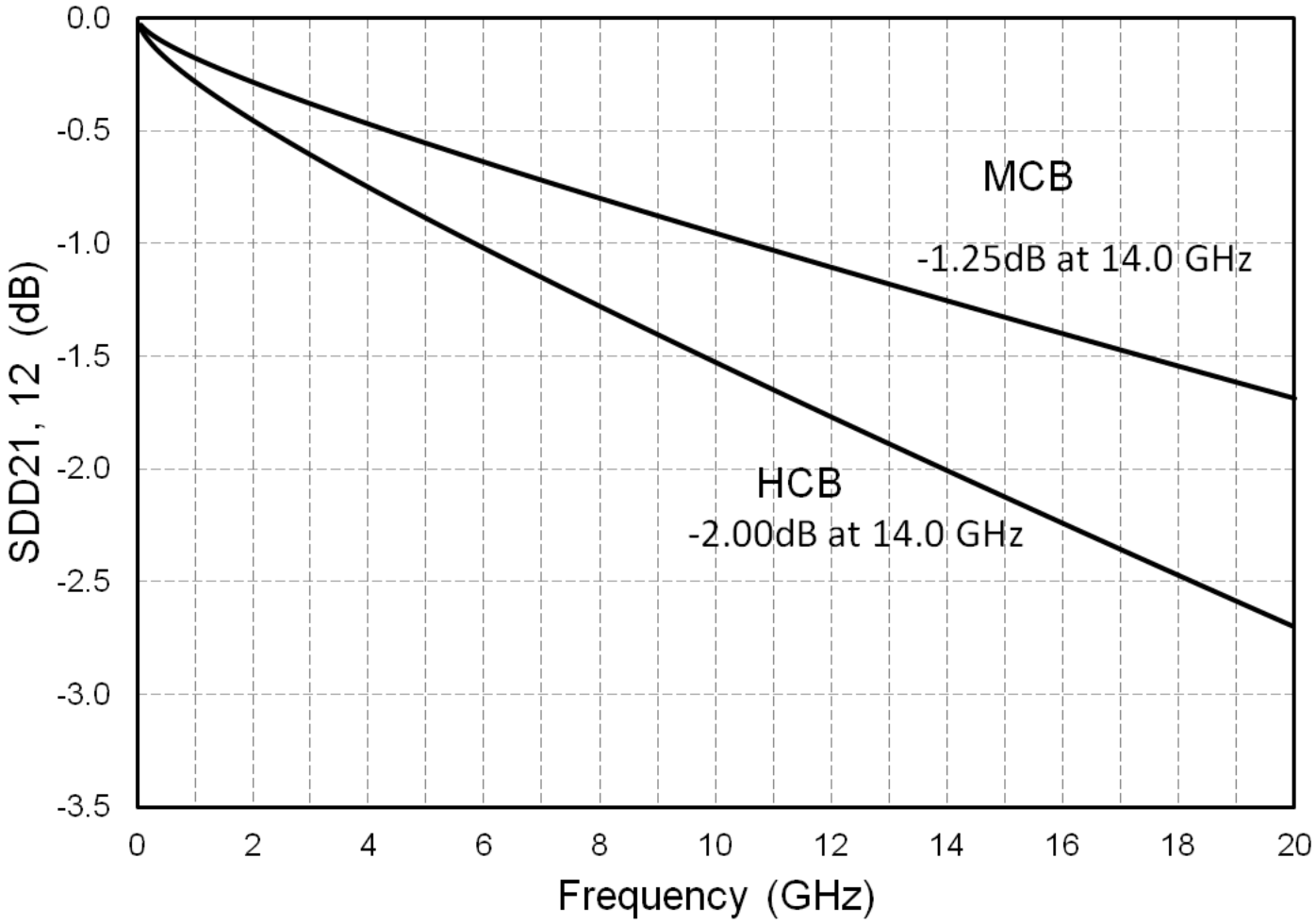




- The total jitter (TJ) of a signal is defined as the range (the difference between the lowest and highest values) of sampling times around the signal transitions for which the BER at these sampling times is greater than or equal to 10^{-12}. Total Jitter shall be less than [see spec]
- Use PRBS9 for channel under test
  - enables capturing waveform and reference CTLE
  - capture 4 million bits with 3 samples per bit to allow for post processing
- Dual-Dirac mathematical model to extrapolate to 10^{-12}

Compliance Boards

Same as CR4



Appendix: TJ Derivation for Host Tx (1/3)

Assumptions:

- DJ, RJ, and DN, RN are the same as CEI-28G VSR
- BER for CEI-28G VSR is at 1e-15, and for 802.3bm c2m is at 1e-12
- Dual-Dirac model for jitter and noise

Starting Eqs for TJs: namely $TJ_0(1e\text{-}15)$ and $TJ_1(1e\text{-}12)$

$$TJ_0 = DJ_0 + 2Q_0RJ_0 \qquad (1)$$

$$TJ_1 = DJ_0 + 2Q_1RJ_0 \qquad (2)$$

(2) - (1), and do re-arrangement, we will have

$$TJ_1 = TJ_0 + 2(Q_1 - Q_0)RJ_0 \qquad (3)$$

Using $TJ_0 = 0.54\text{UI}, Q_0(1e-15) = 7.941, RJ_0 = (0.15/2Q_0)$ UI, from CEI – 28G VSR, and $Q_1(1e-12) = 7.035$, we get

$$TJ_1 = 0.5229 \approx 0.52 \text{ UI} \qquad (4)$$

Appendix: EH Derivation for Host Tx (2/3)

Assumptions:

- DJ, RJ, and DN, RN are the same as CEI - 28G VSR
- BER for CEI - 28G VSR is at 1e -15, and for 802.3bm c2m is at 1e -12
- Dual - Dirac model for jitter and noise

Starting Eqs for EHs: namely $EH_0(1e\text{-}15)$ and $EH_1(1e\text{-}12)$

$$EH_0 = V_{pp} - TN_0 = V_{pp} - (DN_0 + 2Q_0 RN_0) \qquad (1)$$

$$EH_1 = V_{pp} - TN_1 = V_{pp} - (DN_0 + 2Q_1 RN_0) \qquad (2)$$

(2) - (1), and do re - arrangement, we will have

$$EH_1 = EH_0 - 2(Q_1 - Q_0)RN_0 \qquad (3)$$

Using $EH_0 = 100$ mv, $Q_0(1e-15) = 7.941$, $RN_0 = 3$ mv, from CEI – 28G VSR, and $Q_1(1e-12) = 7.035$, we get

$$EH_1 = 105.436 \text{ mv} \approx 106 \text{ mv} \qquad (4)$$

Appendix: TJ, EH Derivations for Module Tx (3/3)

- Similar methods were used for TJ and EH derivations for module Tx