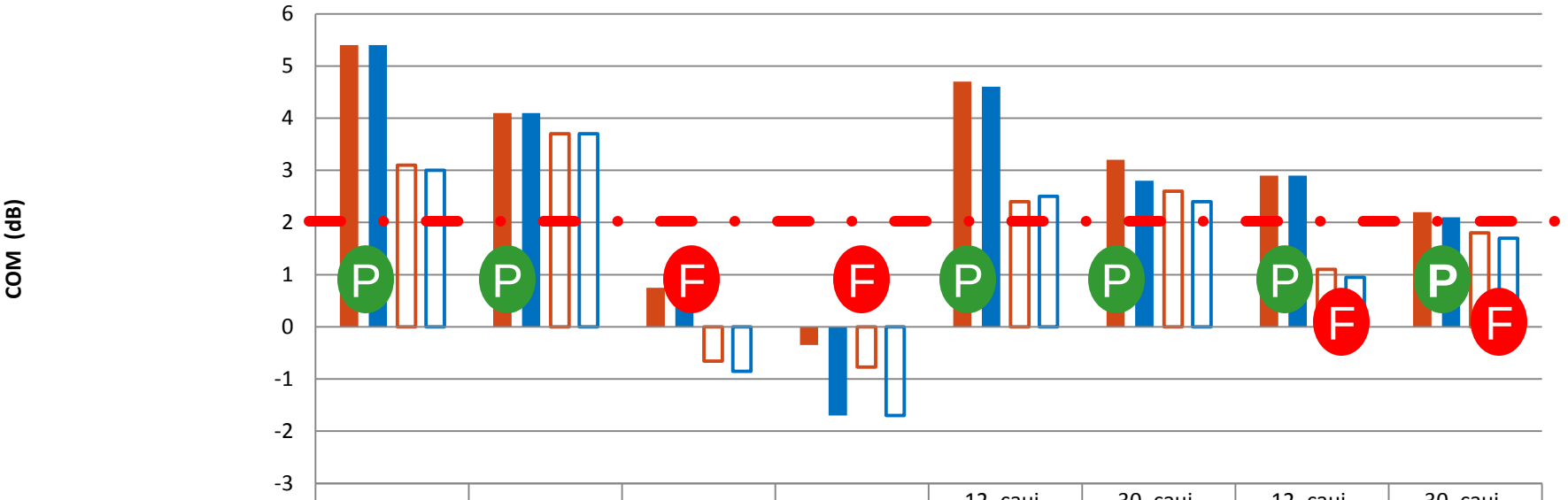
# Limiting DFE Affect on Burst Error Probability

Richard Mellitz, Intel Corporation
Adee Ran, Intel Corporation

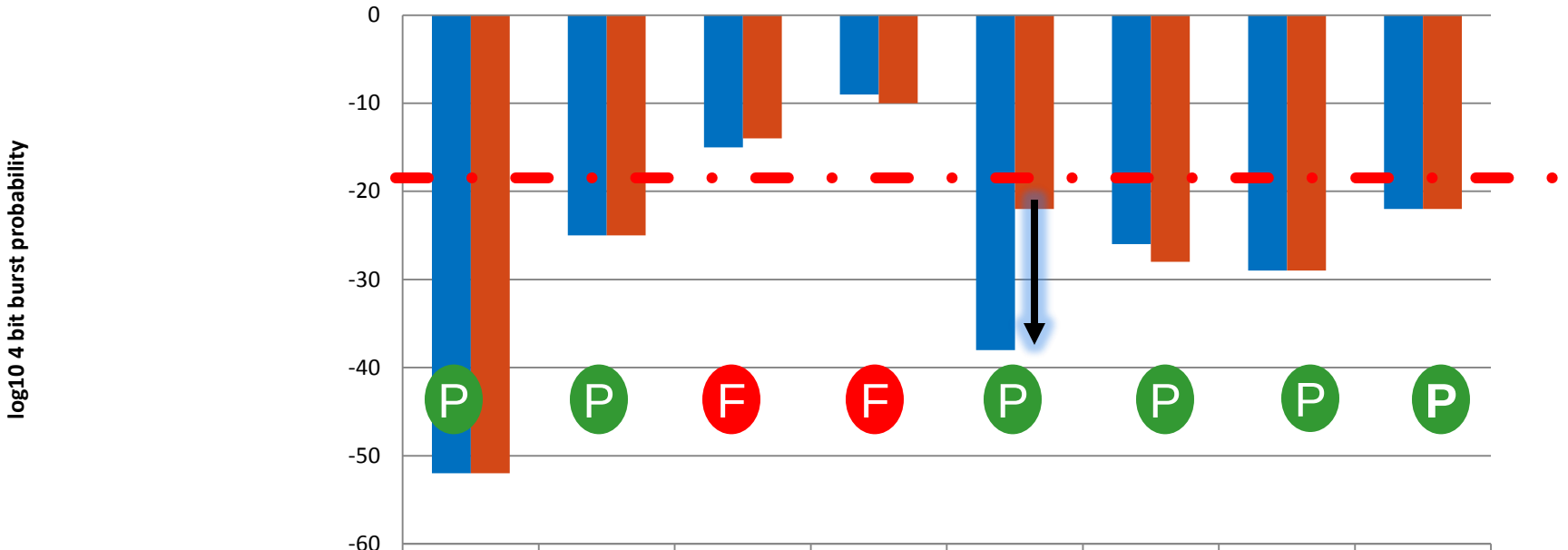
Follow up to: mellitz_01_093013.pdf

# Little affect on COM from limiting DFE tap size from 1 to 0.3 for these channels




| | 12_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 12_Hirose_IT5_20dB-channel_J9-L9_thru | 30_Hirose_IT5_20dB-channel_J9-L9_thru | 12_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 12_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 30_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru |
|---|---|---|---|---|---|---|---|---|
| COM_dB_B_limit_1p0_dfe5 | 5.4 | 4.1 | 0.75 | -0.35 | 4.7 | 3.2 | 2.9 | 2.2 |
| COM_dB_B_limit_0p3_dfe5 | 5.4 | 4.1 | 0.59 | -1.7 | 4.6 | 2.8 | 2.9 | 2.1 |
| COM_dB_B_limit_1p0_dfe3 | 3.1 | 3.7 | -0.66 | -0.77 | 2.4 | 2.6 | 1.1 | 1.8 |
| COM_dB_B_limit_0p3_dfe3 | 3 | 3.7 | -0.85 | -1.7 | 2.5 | 2.4 | 0.95 | 1.7 |

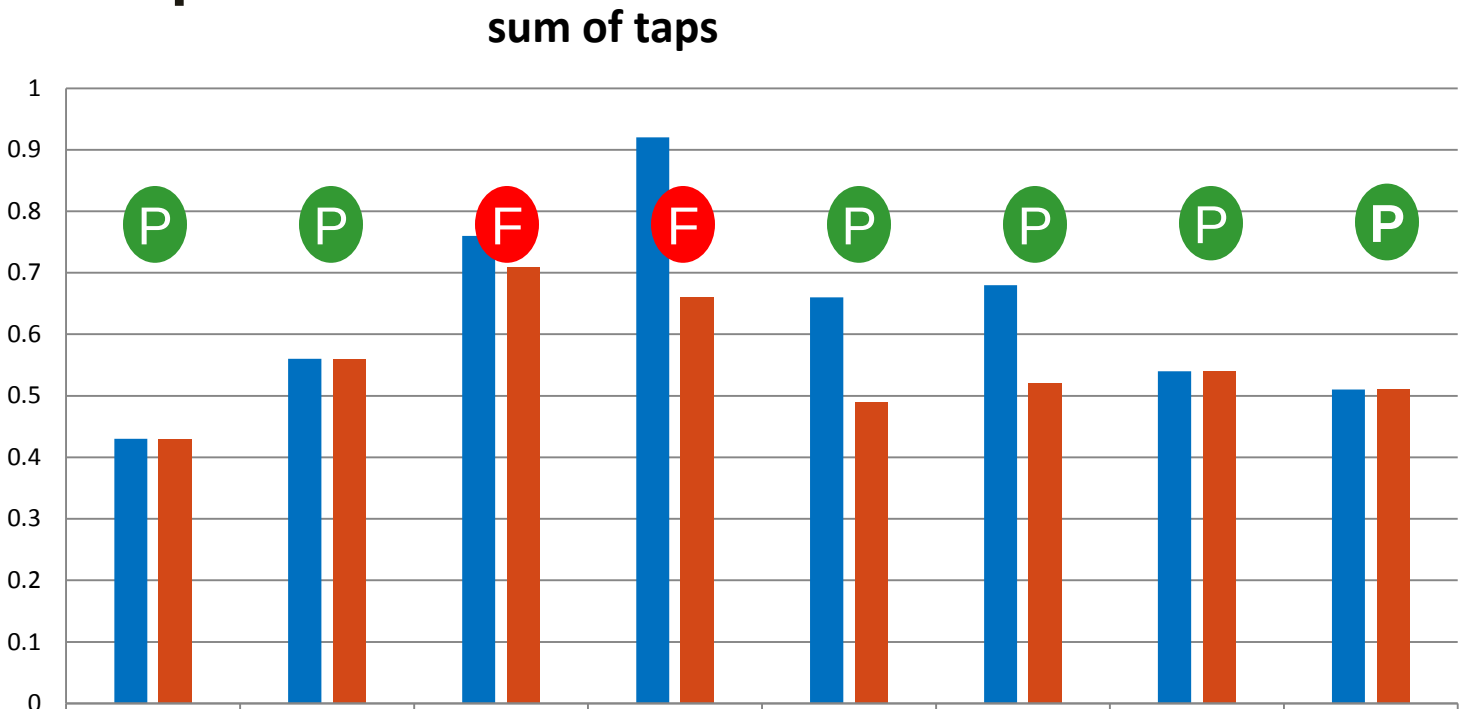
# DFE 0.3 limit* improves 4 bit burst probability




| | 12_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 12_Hirose_IT5_20dB-channel_J9-L9_thru | 30_Hirose_IT5_20dB-channel_J9-L9_thru | 12_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 12_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 30_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru |
|---|---|---|---|---|---|---|---|---|
| Log10_P4_burst_B_limit_0p3_dfe5 | -52 | -25 | -15 | -9 | -38 | -26 | -29 | -22 |
| Log10_P4_burst_B_limit_1p0_dfe5 | -52 | -25 | -14 | -10 | -22 | -28 | -29 | -22 |

* Largest DFE taps used for calculating burst probabilities

# SUM of DFE taps sometimes change as result of the DFE tap limit




| | 12_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 12_Hirose_IT5_20dB-channel_J9-L9_thru | 30_Hirose_IT5_20dB-channel_J9-L9_thru | 12_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 30_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 12_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 30_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru |
|---|---|---|---|---|---|---|---|---|
| SUM_B_limit_1p0_dfe5 | 0.43 | 0.56 | 0.76 | 0.92 | 0.66 | 0.68 | 0.54 | 0.51 |
| SUM_B_limit_0p3_dfe5 | 0.43 | 0.56 | 0.71 | 0.66 | 0.49 | 0.52 | 0.54 | 0.51 |

# DFE tap setting

| channel | DFE1_B_limit_1p0_dfe5 | DFE2_B_limit_1p0_dfe5 | DFE3_B_limit_1p0_dfe5 | DFE4_B_limit_1p0_dfe5 | DFE5_B_limit_1p0_dfe5 | DFE1_B_limit_0p3_dfe5 | DFE2_B_limit_0p3_dfe5 | DFE3_B_limit_0p3_dfe5 | DFE4_B_limit_0p3_dfe5 | DFE5_B_limit_0p3_dfe5 | sum B limit 1 | sum B limit 0.3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 0.05 | -0.18 | -0.03 | -0.13 | 0.04 | 0.05 | -0.18 | -0.03 | -0.13 | 0.04 | 0.23 | 0.23 |
| 30_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 0.29 | -0.12 | -0.06 | -0.06 | -0.03 | 0.29 | -0.12 | -0.06 | -0.06 | -0.03 | 0.33 | 0.33 |
| 12_Hirose_IT5_20dB-channel_J9-L9_thru | 0.44 | -0.09 | -0.08 | -0.10 | 0.06 | 0.29 | -0.15 | -0.11 | -0.11 | 0.05 | 0.47 | 0.37 |
| 30_Hirose_IT5_20dB-channel_J9-L9_thru | 0.67 | -0.03 | -0.14 | -0.06 | -0.02 | 0.30 | -0.23 | -0.11 | -0.02 | 0.00 | 0.69 | 0.39 |
| 12_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 0.38 | -0.11 | -0.04 | -0.13 | 0.00 | 0.14 | -0.18 | -0.01 | -0.12 | 0.03 | 0.42 | 0.26 |
| 30_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 0.55 | -0.01 | -0.04 | -0.05 | -0.03 | 0.30 | -0.15 | -0.03 | -0.03 | -0.01 | 0.55 | 0.34 |
| 12_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 0.30 | -0.04 | 0.02 | -0.10 | 0.09 | 0.30 | -0.04 | 0.02 | -0.10 | 0.09 | 0.33 | 0.33 |
| 30_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 0.35 | -0.07 | -0.04 | -0.03 | 0.02 | 0.30 | -0.10 | -0.06 | -0.04 | 0.01 | 0.36 | 0.32 |

| | DFE1_B_limit_1p0_dfe3 | DFE2_B_limit_1p0_dfe3 | DFE3_B_limit_1p0_dfe3 | DFE1_B_limit_0p3_dfe3 | DFE2_B_limit_0p3_dfe3 | DFE3_B_limit_0p3_dfe3 | sum B limit 1 | sum B limit 0.3 |
|---|---|---|---|---|---|---|---|---|
| 12_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 0.47 | 0.10 | 0.11 | 0.30 | 0.05 | 0.09 | 0.49 | 0.32 |
| 30_caui-4_chip2chip_oneboard_15dB_92_ohm_target_board_MEG6_Thru | 0.29 | -0.09 | 0.01 | 0.29 | -0.09 | 0.01 | 0.30 | 0.30 |
| 12_Hirose_IT5_20dB-channel_J9-L9_thru | 0.45 | 0.01 | -0.01 | 0.30 | -0.09 | -0.05 | 0.45 | 0.32 |
| 30_Hirose_IT5_20dB-channel_J9-L9_thru | 0.61 | 0.02 | -0.07 | 0.30 | -0.23 | -0.11 | 0.61 | 0.39 |
| 12_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 0.45 | 0.06 | 0.07 | 0.30 | -0.04 | 0.06 | 0.46 | 0.31 |
| 30_caui-4_chip2chip_oneboard_meg6_long_20dB_92_ohm_target_board_MEG6_Thru | 0.35 | -0.12 | -0.01 | 0.30 | -0.15 | -0.03 | 0.37 | 0.34 |
| 12_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 0.40 | 0.10 | 0.07 | 0.30 | 0.08 | 0.06 | 0.42 | 0.32 |
| 30_caui-4_chip2chip_twoboards_meg6a_13p39dB_92_110_ohm_target_board_meg6_Thru | 0.39 | -0.03 | -0.02 | 0.30 | -0.05 | -0.02 | 0.39 | 0.31 |

# Summary

- Limiting the tap magnitudes has been shown (with the channels evaluated) to avert error propagation.
- Now all we need is to measure the likelihood of long bursts in an operating system