CAUI-4 Consensus Building, Specification Discussion

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Agenda

- Patent Policy:
  - The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- VSR Update
- Chip-Module specs
- Chip-Chip specs
- Path forward

CAUI-4 Chip - Module Spec Discussion

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CAUI-4 Chip-module host transmitter considerations

- Comparing CR4 with VSR
  - 802.3bj D1.2 TP2 vs VSR 7.2, TP1a

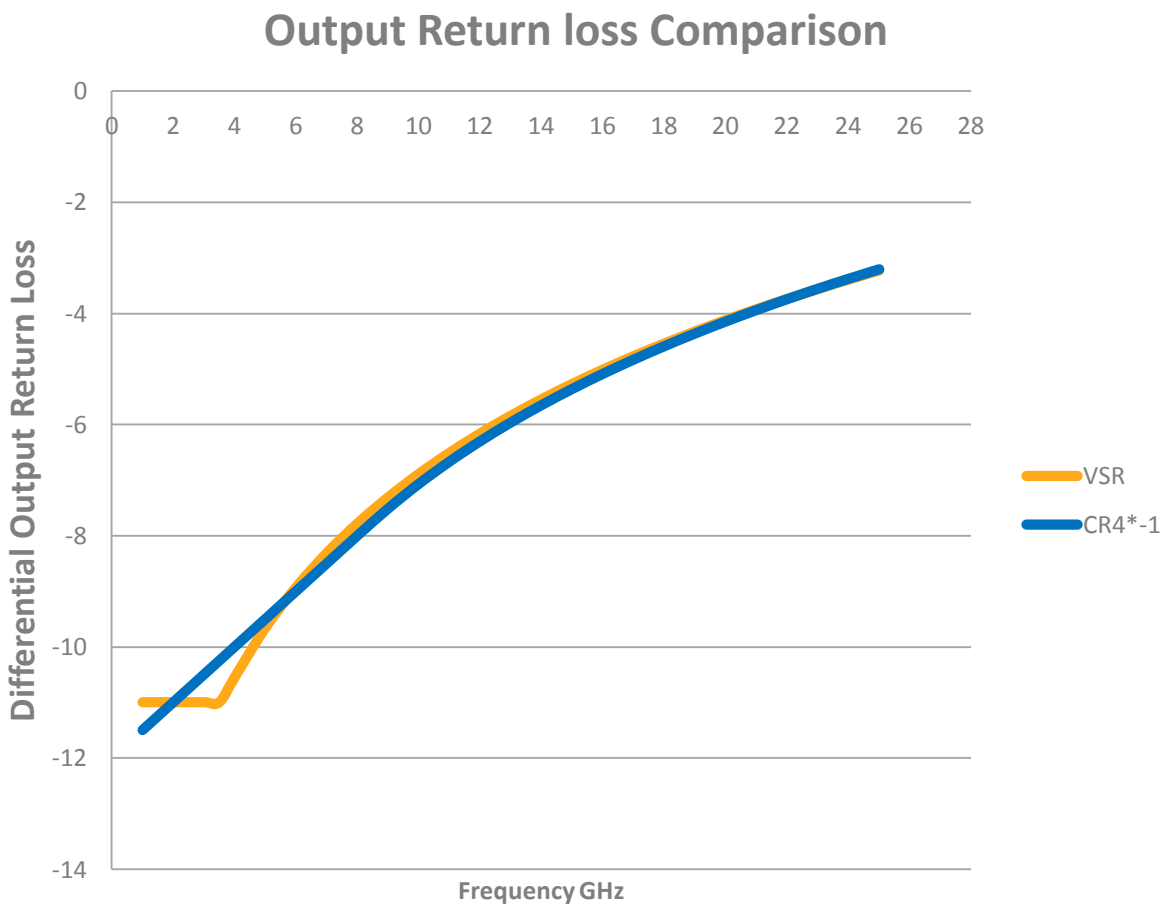
	CR4 (D1.2, TP2)	VSR (7.2, TP1a)	CAUI-4 Chip-Module Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak output voltage (max) with Tx disabled	35mV		35mV
Common Mode Voltage (max)	1.9V	-0.3V (min) to 2.8V (max)	
Differential output return loss (min)	SDD22>= 12-0.5f for 0.01<=f<=8 SDD22>= 5.65-9.71$\log_{10}$(f/14)	SDD22 < -11dB for 0.05<f<fb/7 SDD22 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD22>= 12-0.5f for 0.01<=f<=8 SDD22>= 5.65-9.71$\log_{10}$(f/14)
Common-mode AC output voltage (max,rms)	30mV	17.5mV	17.5mV
Amplitude peak-to-peak (max)	1200mV	900mV	900mV

CAUI-4 Chip-module host transmitter considerations

- Different methodologies used to specify jitter, Tx waveform
  - Need to agree on methodology before setting numbers

	CR4 (D1.2, TP2)	VSR (7.2, TP1a)	CAUI-4 Chip-Module Potential
Transmitter steady state voltage	0.34 (min) - 0.6V (max)		
Linear fit pulse (min)	0.52 x Transmitter steady state voltage		
Transmitted wave form Max RMS normalized error (linear fit), “e” abs coefficient step size (min.) abs coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 0.037 0.0083 0.05 1.54 4		
Far end transmit output noise (max)	2mV (low loss channel) 1mV (high loss channel)		
Output jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	0.54UIpp @ 10^{-15} Measured using CTLE	0.54UIpp @ 10^{-12} Measured using reference CTLE
Amplitude peak-to-peak (min)		100mVppd Measured using CTLE	100mVppd @10^{-12} Measured using reference CTLE
Differential termination mismatch (max)		10%	
Common to differential mode conversion (max)		SDC22 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC22 < -15 dB for fb/2<f<fb	
Transition time (min, 20/80%)		10ps	10ps

Output Returnloss Comparison



CAUI-4 chip-module channel Insertion loss

92.8.3.5 Insertion loss TP0 to TP2 or TP3 to TP5

Transmitter measurements and tests defined in Table 92–5 are made at TP2 or TP3 using the test fixture of Figure 92–13, or its equivalent. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is given by Equation (92–4). Note that the insertion loss from TP0 to TP2 or from TP3 to TP5 is 10 dB at 12.8906 GHz.

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f \le 18.75 \end{cases} \text{ (dB)} \qquad (92\text{–}4)$$

for 0.01 GHz ≤ f ≤ 18.75 GHz

where

f	is the frequency in GHz
$Insertion\_loss(f)$	is the insertion loss at frequency f

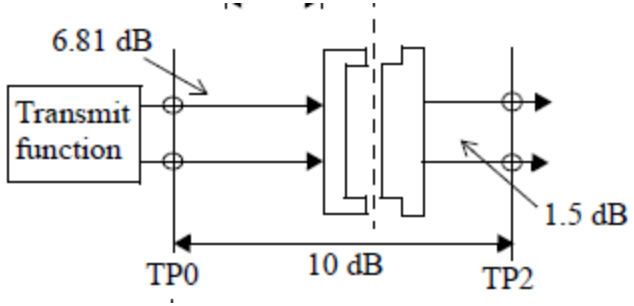
The maximum insertion loss of TP0 to TP2 or TP3 to TP5 is illustrated in Figure 92–5.

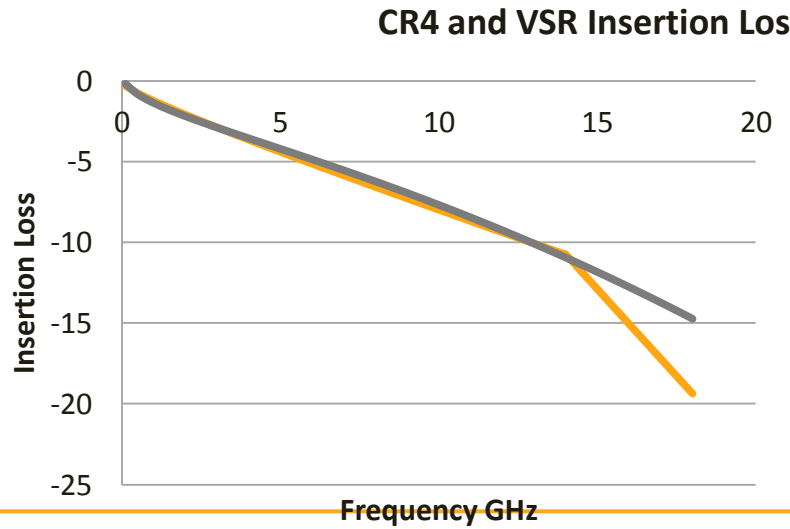
92A.4 Transmitter and receiver differential printed circuit board trace loss

The maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is determined using Equation (92A–1) and illustrated in Figure 92A–1. Note that the maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 6.81 dB at 12.9806 GHz. The maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss TP0 to TP2 or TP3 to TP5 given in 92.8.3.5 and an assumed mated connector loss of 1.69 dB.

$$IL_{PCB}(f) \le IL_{PCBmax}(f) = 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \text{ (dB)} \qquad (92A\text{–}1)$$

for 0.01 GHz ≤ f ≤ 18.75 GHz.





CAUI-4 Chip-module module receiver considerations

	VSR (7.2, TP1)	CAUI-4 Chip-Module Potential
Bit Error Ratio	10^{-15} or better per lane	10^{-12} or better
Signaling rate, per lane	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	35.65ps - 51ps	38.787879ps
Differential peak-to-peak input amplitude tolerance	900mVppd	900mVppd
Differential termination mismatch (max)	10%	
Differential input return loss (max)	SDD11 < -11dB for 0.05<f<fb/7 SDD11 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD11>= 12-0.5f for 0.01<=f<=8 SDD11>= 5.65-9.71$\log_{10}$(f/14)
Common to differential mode conversion (max)	SDC11 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC11 < -15 dB for fb/2<f<fb	SDC11 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC11 < -15 dB for fb/2<f<fb
Stress receiver test (min)	See Section 1.3.10.2.1	

Module Stress Receiver Test used in 28G VSR

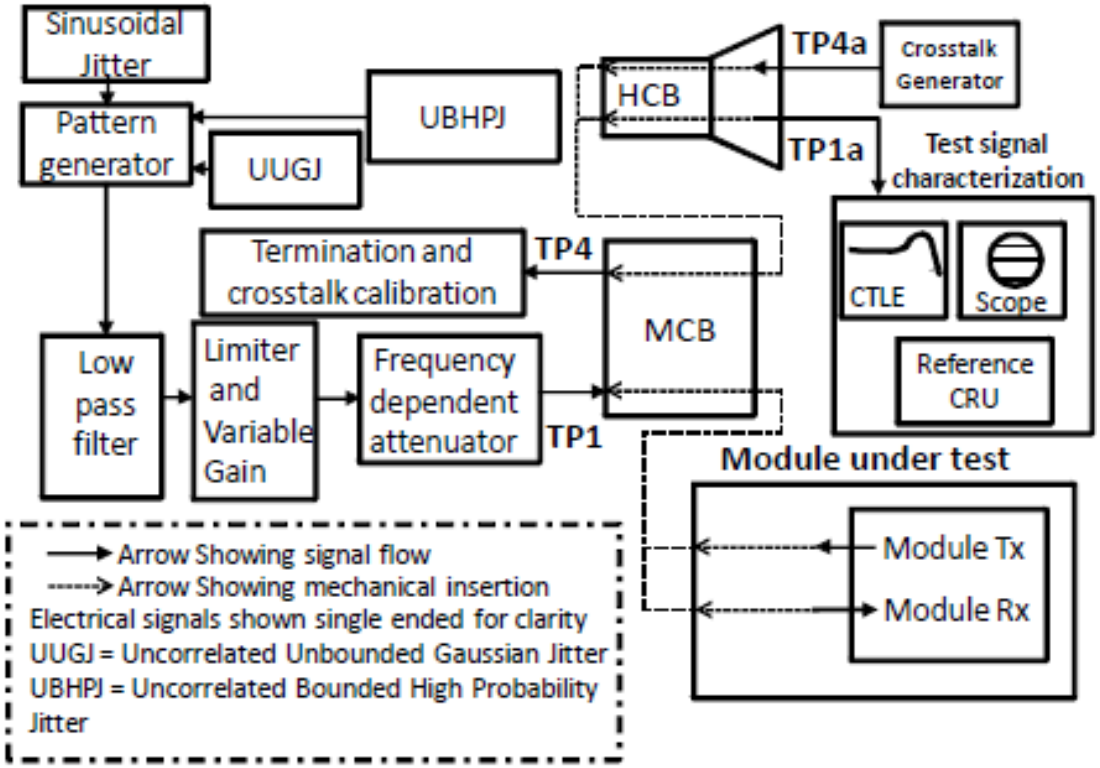


Figure 1-10.Module input stressed receiver test set up

CAUI-4 Chip-module module transmitter considerations

- Use similar specification methodology as host transmitter

	VSR (7.2, TP4a)	CAUI-4 Chip-Module Potential
Signaling rate, per lane	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	35.65ps - 51ps	38.787879ps
Differential voltage peak-to-peak (max)	900mV	900mV
Common-mode noise (rms, max)	17.5mV	17.5mV
Differential termination mismatch (max)	10%	
Differential output return loss (max)	SDD22 < -11dB for 0.05<f<fb/7 SDD22 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD22>= 12-0.5f for 0.01<=f<=8 SDD22>= 5.65-9.71$\log_{10}$(f/14)
Common mode to differential conversion return loss (max)	SDC22 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC22 < -15 dB for fb/2<f<fb	
Transition time 20/80 (min)	9.5ps	9.5
Vertical eye closure (max)	6.5dB	TBD
Eye width at 10^{-15} probability (min)	0.57UI	0.57UI at 10^{-12}
Eye hight at 10^{-15} probability (min)	240mV	240mV at 10^{-12}

CAUI-4 Chip-module host receiver considerations

	CR4(1.2TP3)	VSR (7.2, TP4a)	CAUI-4 Chip-Module Potential
Bit Error Ratio	10^{-12} or better	10^{-15} or better per lane	10^{-12} or better
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak input amplitude tolerance / overload differential voltage pk-pk	1200mVppd (max)	900mVppd (min)	900mVppd
Differential input return loss (min) / Differential return loss (max)	12-1.24(f)^0.5, 0.01≤ f ≤ 10.31 6.3-13log10(f/13.75), 10.31≤ f ≤ 25	SDD11 < -11dB for 0.05<f<fb/7 SDD11 < -6.0 + 9.2*log(2f/fb) dB for fb/7<f<fb	SDD11>= 12-0.5f for 0.01<=f<=8 SDD11>= 5.65-9.71$\log_{10}$(f/14)
Differential to common mode input return loss (min) / Common mode to differential conversion loss (min)	10, 0.01≤ f ≤ 25 GHz	SDC11 < -25 + 20*(f/fb) dB for 0.05<f<fb/2 SDC11 < -15 dB for fb/2<f<fb	
Stress receiver test (min)	See 92.8.4.2	See Section 1.3.10.2.1	
Differential termination mismatch (max)		10%	

Mode conversion Comparison

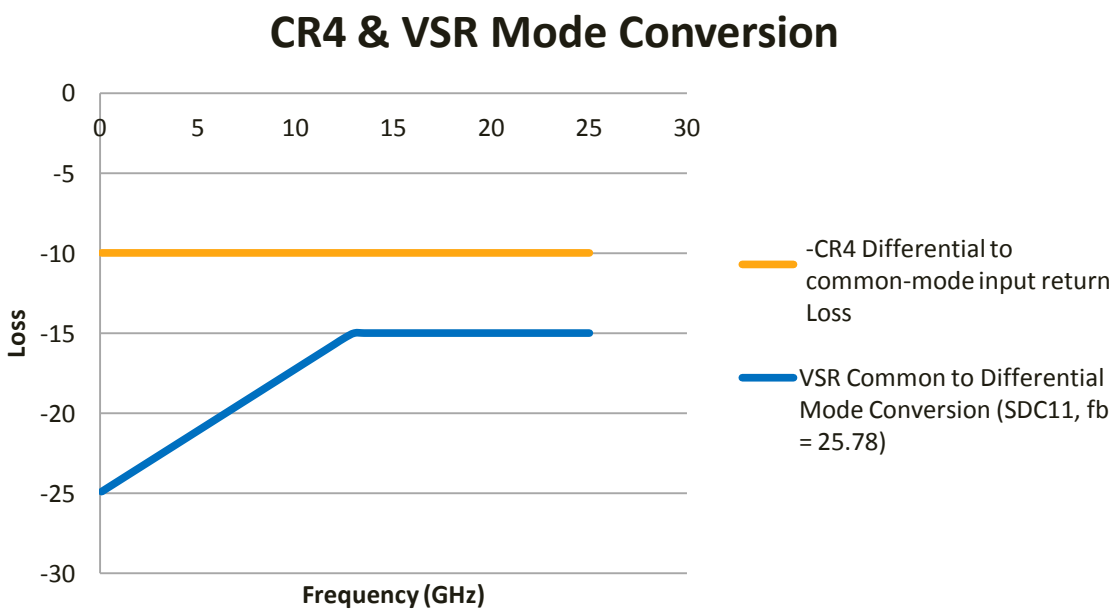
Table 92–7—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Bit error ratio	92.8.4.4	10^{-12} or better	
Signaling rate, per lane	92.8.4.5	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.5	38.787879	ps
Differential peak-to-peak input amplitude tolerance (max)	72.7.2.4	1200	mV
Differential input return loss (min)[a]	92.8.4.1	Equation (92–5)	dB
Differential to common-mode input return loss	92.8.4.2	10 min from 0.01 GHz to 25 GHz	dB

[a]Relative to 100 Ω differential.

SCD11, SDC11 < -25+20*(f/fb) dB for 0.05<f<fb/2

SCD11, SDC11 < -15 dB for fb/2<f<fb



Host Stress Receiver Test used in 28G VSR

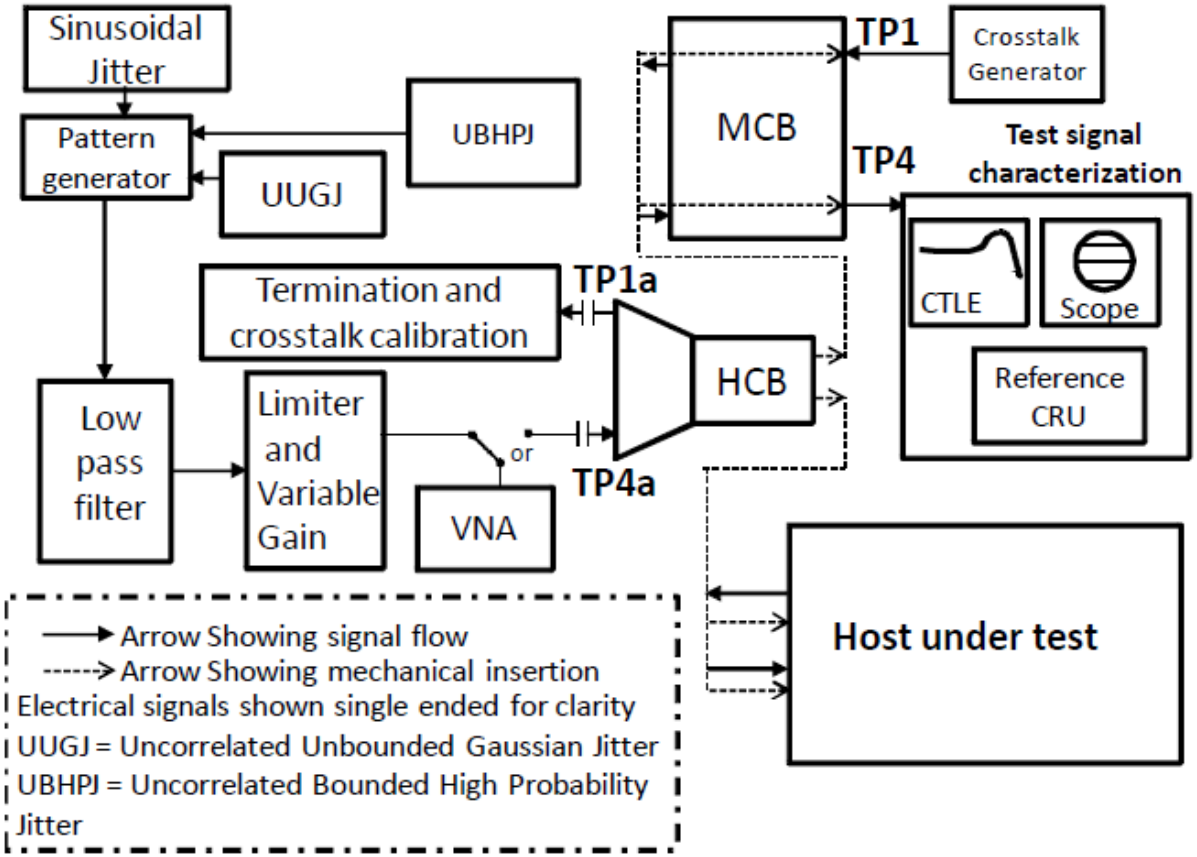


Figure 1-9.Host input test set up

CAUI-4 Chip – Chip Spec Discussion

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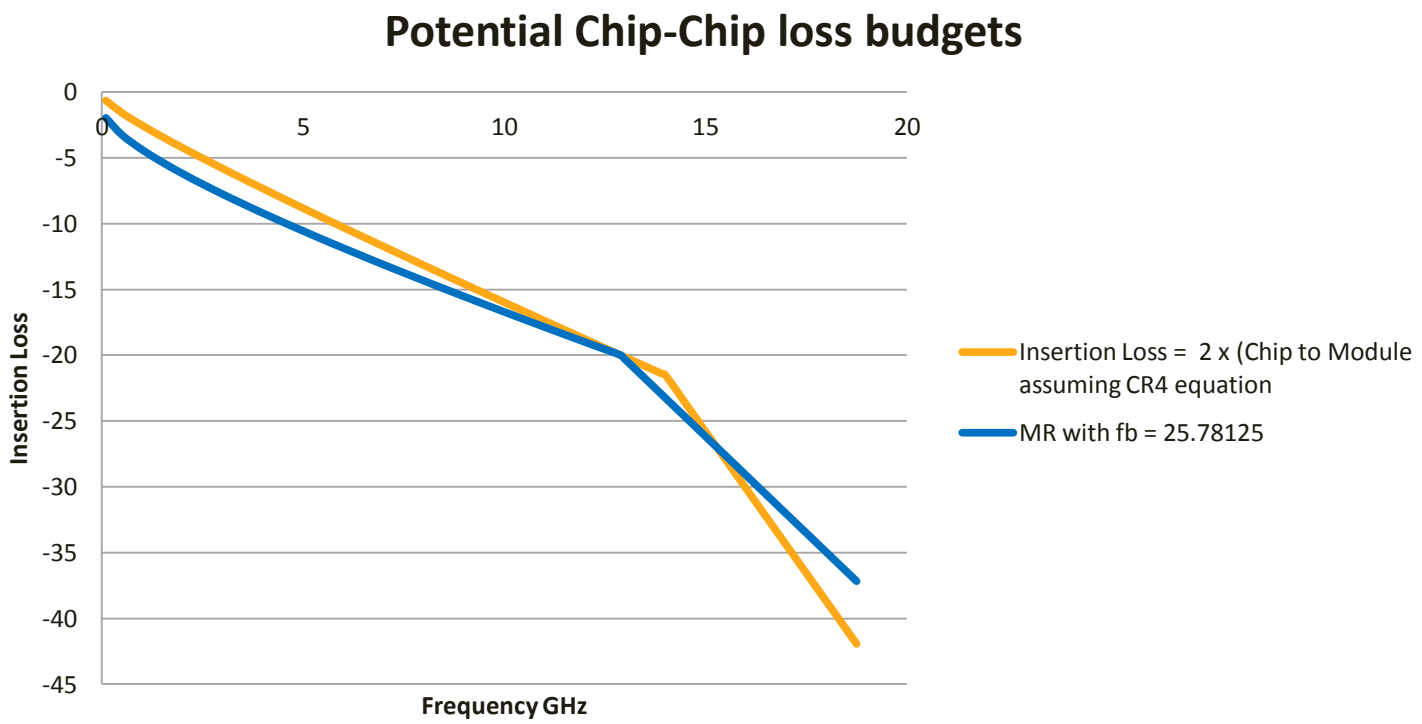
Chip-Chip Considerations

- Target: low power, simple chip-chip specification to allow communication over TBD loss with one connector
  - Similar to Annex 83A in 802.3ba
    - 25cm or ~10 inches over PCB
    - If we apply 1.7dB loss / inch we get 17dB + Connector (~1dB)
      - Meg6_HighSR-Narrow (kochuparambil_01_0112)
  - Compare to OIF SR / MR
    - SR: 15.4dB
    - MR: ~20dB
  - ghiasi_02_0912_optx mentions 30cm
    - 18-20dB loss budget
- Potential differences with KR4:
  - Lower loss budget supports lower power, smaller receiver design
  - Reduced latency & complexity
    - No FEC
    - No in-band transmitter training
      - Adaptive Rx (SFP+)
      - Assume “system management”

CAUI-4 Chip-Chip Channel Considerations



CAUI-4 Chip-Chip transmitter considerations

- Comparing KR4 with MR

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	
Unit Interval	38.787879ps	35.65ps - 51ps	
Differential peak-to-peak output voltage (max) with Tx disabled	30mV		
Common Mode Voltage (max)	1.9V	1.7V (max)	
Common Mode Voltage (min)	0V	-0.1V	
Differential output return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=13GHz	-6dB , f<10GHz -4dB, 10G<f<25.78125GHz	
Common-mode AC output voltage (max,rms)	12mV	12mV	
Amplitude peak-to-peak (max)	1200mV	1200mV	
Amplitude peak-to-peak (min)		800mV	

CAUI-4 Chip-Chip transmitter considerations

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Transmitter steady state voltage	0.4 (min) - 0.6V (max)		
Linear fit pulse (min)	0.8 x Transmitter steady state voltage		
Transmitted wave form Max RMS normalized error (linear fit), “e” abs coefficient step size (min.) abs coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 0.037 0.0083 0.05 1.54 4		
Far end transmit output noise (max)	2mV (low loss channel) 1mV (high loss channel)		
Output jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	TUUGJ = 0.15UIpp T_UBHPJ = 0.15UIpp T_DCD = 0.035UIpp TJ = 0.28UIpp	
Differential Resistance		80 ohms min, 100ohms typ, 120 ohms max	
Transition time (min, 20/80%)	8ps	8ps	

CAUI-4 Chip-Chip Receiver considerations

- Comparing KR4 with MR

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Differential Input Return loss (min)	RL(f) >= -10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	
Common mode input return loss (min)	RL(f) >=6dB, 0.05<=f<=13GHz	6dB , f<10GHz -4dB, 10G<f<25.78125GHz	
Differential to common-mode return loss (min)	TBD		
Input Differential Voltage (max)		1200	
Differential Impedance		80ohms min, 100ohms typical, 120ohms max	
Input Impedance Mismatch (max)		10%	
Input common mode voltage		-200mV (min), 1800mV (max)	

Path Forward

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Next Call: CAUI-4 Chip-Chip

- Confirm desired channel characteristics
- Formulate Transmitter / Receiver Characteristics
  - Leverage KR4 compliance points TP0a, TP5a
- Develop appropriate stress methodology