PSM4 Technology & Relative Cost Analysis Update

Jon Anderson, Oclaro
Kiyo Hiramoto, Oclaro

IEEE P802.3bm TF, Phoenix, AZ, January 21-24, 2013

Supporters

- Chris Bergey, Luxtera
- Tom Palkert, Luxtera
- John Petrilla, Avago Technologies
- Brian Welch, Luxtera

Introduction

- This presentation provides an update on the 4x 25 Gb/s parallel single mode (PSM4) technology identified in anderson_01_0112 which is proposed as a PHY solution for the 500m single mode objective.
- Furthermore, an update on the PSM4 transceiver relative cost analysis given in anderson_01_0112 is provided. This update is based on PSM4 optical baseline specifications given in 100G PSM4 Link Model Results Comparison, John Petrilla, Dec. 2012, presented at the Dec. 4, 2012 IEEE P802.3bm SMF Ad Hoc conference call.
- Conclusion: Our analysis indicates ~60% cost reduction in optical transceiver is achievable with the proposed PSM4 approach, compared with the current 100GBASE-LR4, for < 500m short reach SMF application.

Outline

- PSM4 optical transmitter, receiver and transceiver technologies overview
- Key PSM4 technology, assembly and test factors providing cost reduction relative to 100GBASE-LR4 technology
- PSM4 transceiver relative cost analysis
- Summary

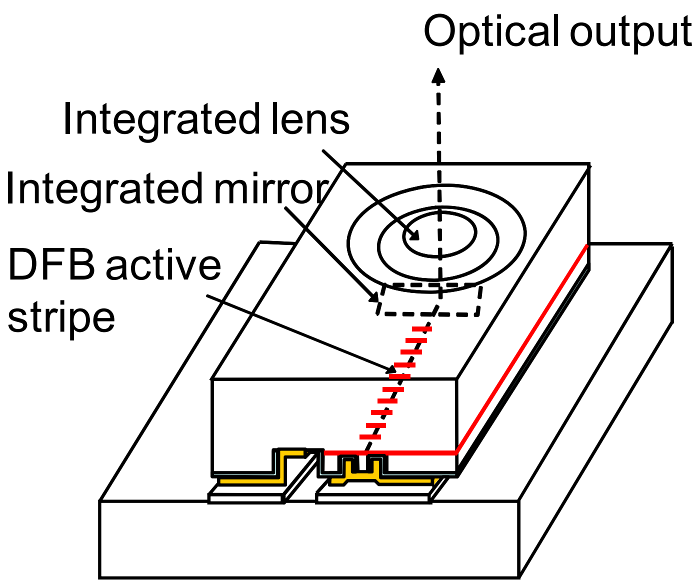
Objectives and Approaches

Objectives	Challenges	Approaches
Low cost	Component # reduction	O-Mux/DeMux free (parallel fiber)
		TEC free (uncooled LD)
	Component & Assembly cost reduction	Passive alignment - Relaxed tolerances by spec relaxation - Lens integrated LD/PD
		Reduce test time: - No wavelength testing - Wafer level testing - Wafer level burn-in
Low power Consumption (Pc)	Low current LD/Driver	Spec relaxation Reach/ER/mask
Compactness	Surface mount	Surface emitting LD/PD

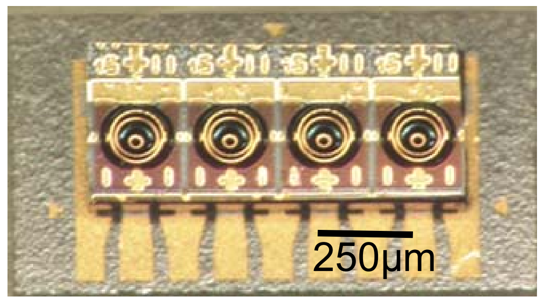
Lens Integrated Surface Emitting Laser (LISEL)

- 1.3μm operation with low Ith (~15 mA @85°C)
- High speed (25Gb/s) up to 100 °C
- Surface emitting/ Flip-chip mount
- 2km error free transmission demonstrated

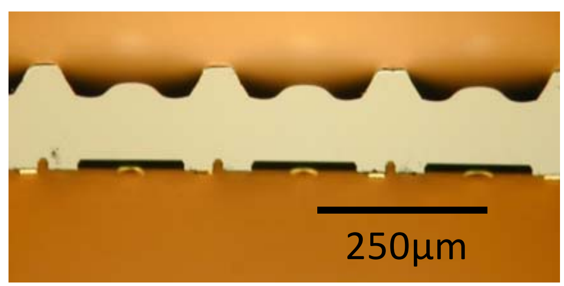
Structure of LISEL

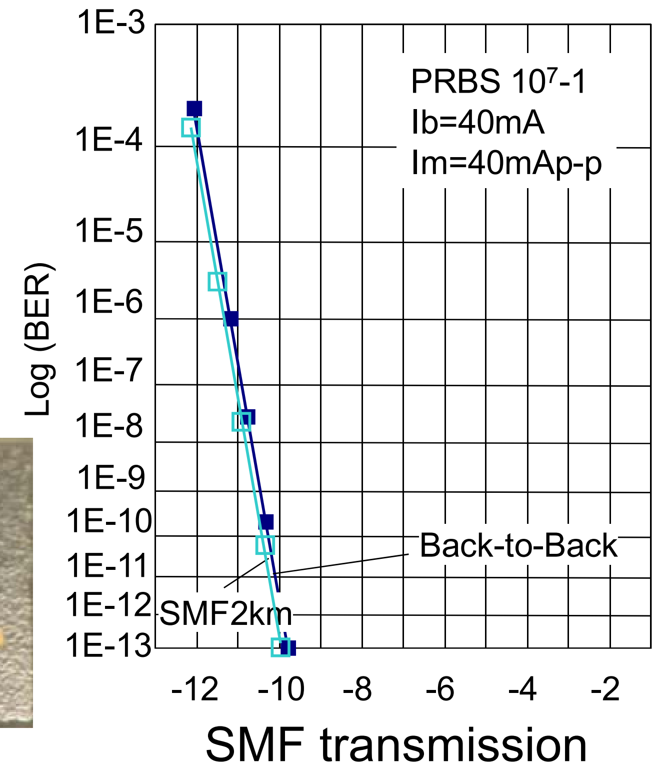


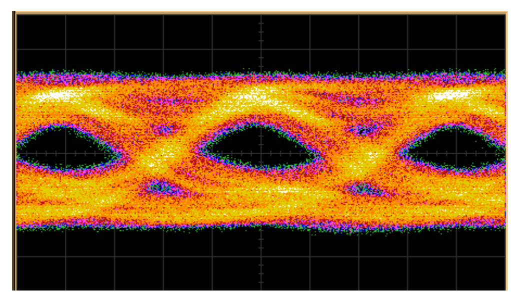
4ch-LISEL array



Cross section







Eye pattern
(Back-to-Back)

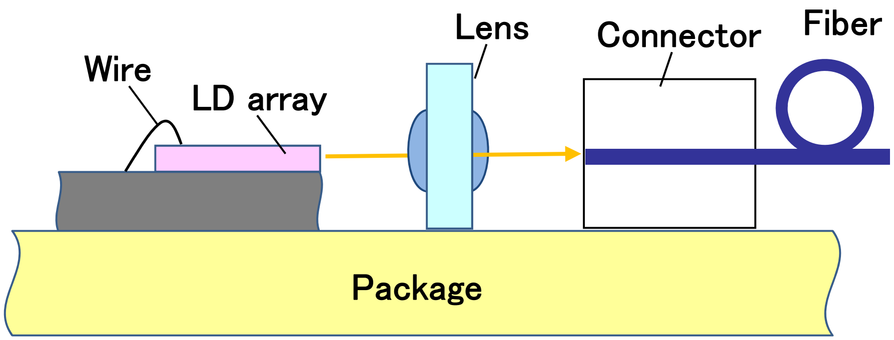
Ref: K. Adachi et al., J. Lightwave Tech. 29, 2899 (2011)

A part of this work was performed under management of the PETRA supported by NEDO.

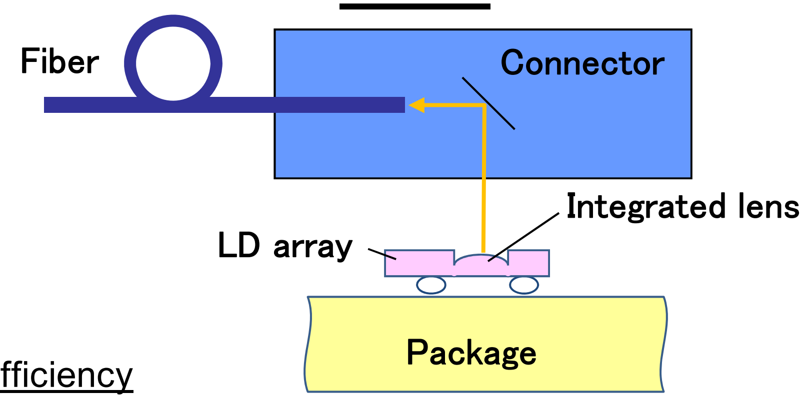
Lens Integrated Surface Emitting Laser (LISEL)

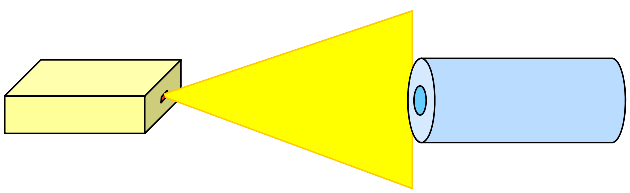
■ **Use of lens-integrated optical devices enables lower cost by excluding lens and by reducing assembly cost with high coupling efficiency**

Edge emitting LD (EELD)

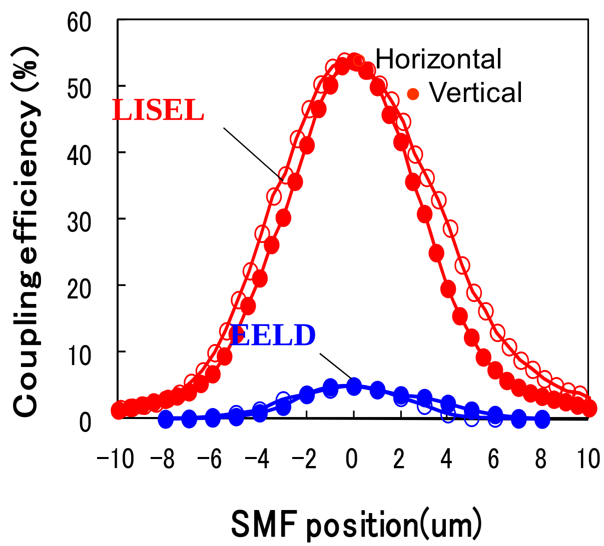


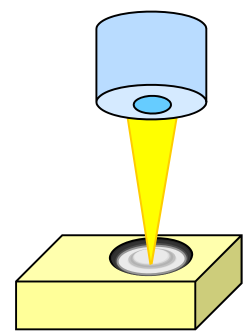
LISEL





Coupling efficiency

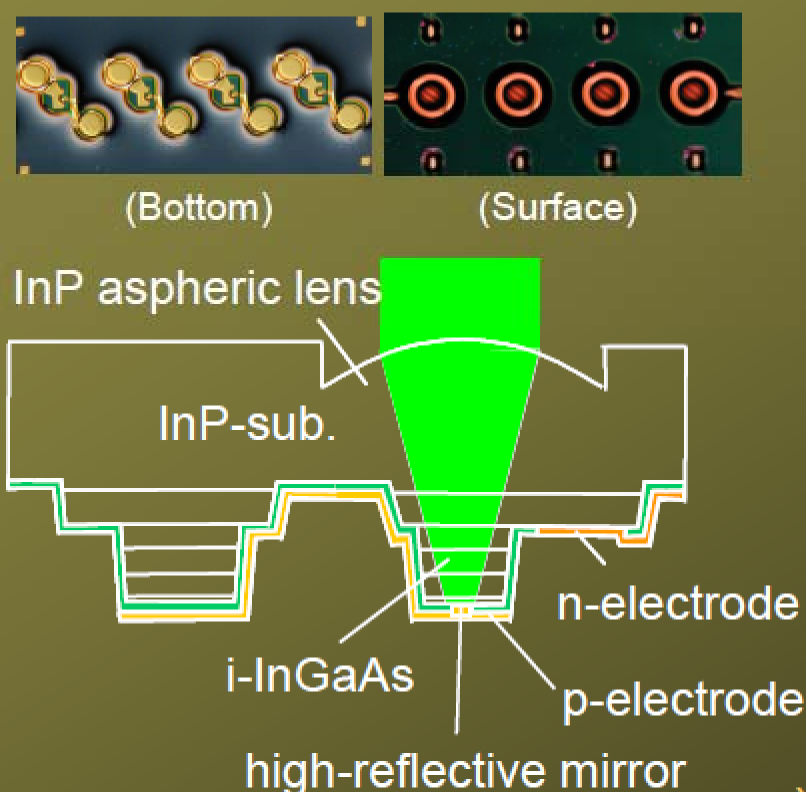


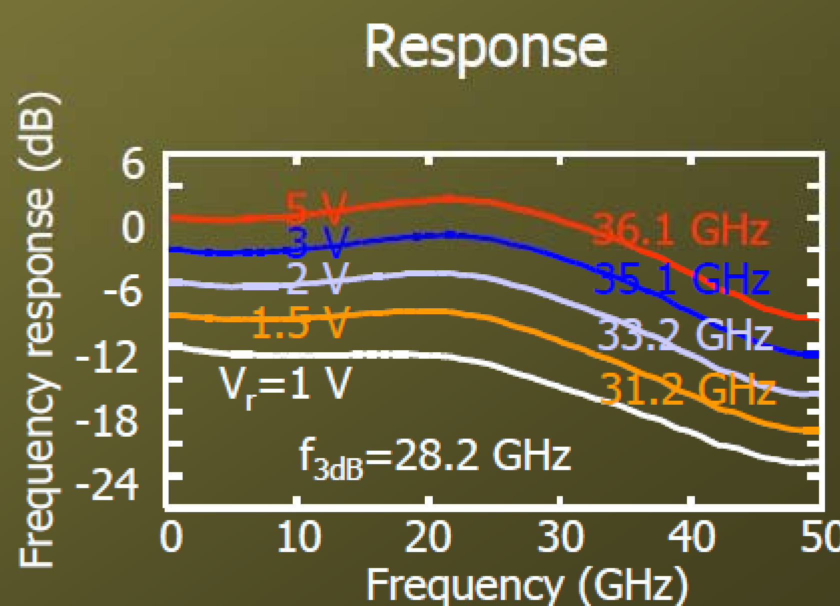


anderson_01_0113_optx

Lens Integrated Photodiode (LIPD)

- High speed: ~35GHz ------ Small area p-i-n
- High responsivity: >0.8A/W --- High reflect. mirror
- Wide align. tolerance: >20μm -- Lens integration

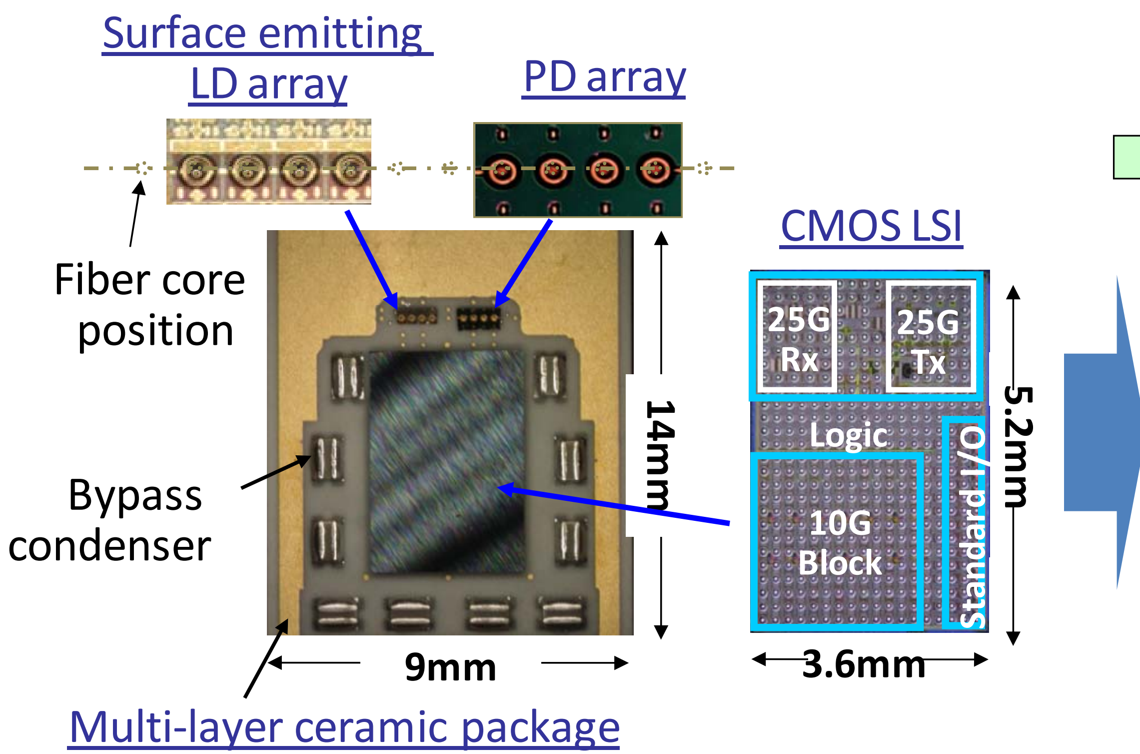


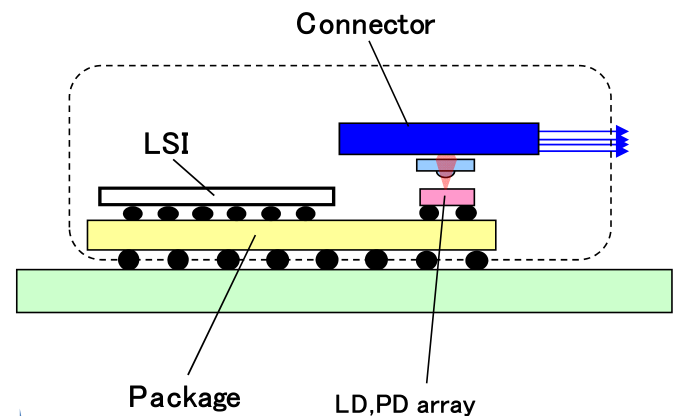


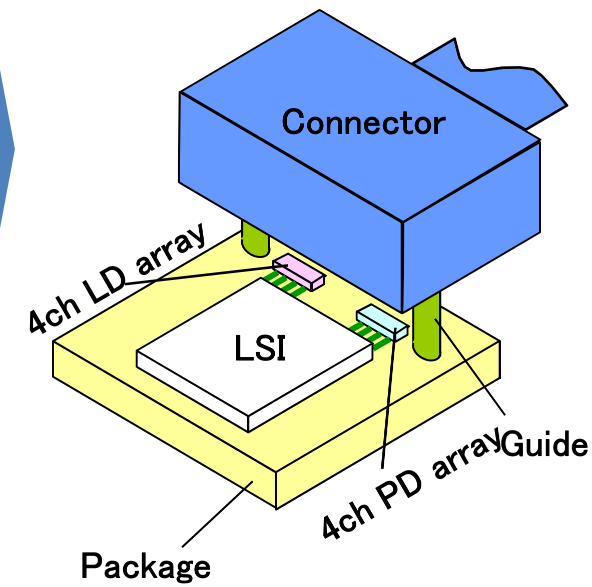
Y. Lee, et al., IEICE Trans. Electron. **E94-C**,p. 116 (2010)

PSM4 transceiver

- Surface mount with passive alignment enables low cost module.
- Use of lens-integrated optical devices reduces components and assembly costs in transceiver design.







Ref: T. Takemoto et al., ECOC 2011, Th.12.B.5 (2011).

A part of this work was performed under management of the PETRA supported by NEDO.

Key factors in PSM4 technology for providing cost reduction relative to 100GBASE-LR4.

Factor	Key Differentiation
Reduced Component Count	▪ **No O-Mux/DeMux** ▪ **No TEC** ▪ Integrated lens in LD, PD devices ▪ Single chip LD array, PD array
Reduced Component Cost	▪ **Spec relaxation, increased yield** ▪ **Relaxed alignment tolerances** ▪ **1-chip CMOS quad CDR with laser driver array** ▪ **Wide spectral range increases LD array yield** ▪ **Small sized OSA package w/o O-Mux/DeMux**
Reduced Assembly Cost	▪ **Relaxed tolerances enabling passive optical alignment** ▪ **Low assembly cost w/o O-Mux/DeMux** ▪ SMT for optical components
Reduced Test Cost	▪ **Wide spectral range eliminates wavelength test** ▪ **On-wafer laser, PD testing and burn-in**

PSM4 Transmitter Optical Sub-Assembly (TOSA) cost analysis, relative to 100G-LR4 and SR4.

100G PMD	Fiber Type	Reach	TOSA		LDD	O-mux	Optic Coupling	Total Rel. Cost
			LD	TEC				
LR4	SMF	10km	Cooled DML	Req	SiGe	Req	Active	1
PSM4	SMF	500m	Surface Emitting DML	NR	CMOS 1-chip CDR	NR	Passive*	0.2
SR4	MMF	100m	VCSEL	NR	CMOS	NR	Passive	<0.2

NR: Not Required

* Design Target

PSM4 Receiver Optical Sub-Assembly (ROSA) cost analysis, relative to 100G-LR4 and SR4.

100G PMD	Fiber Type	Reach	ROSA	TIA	O-demux	Optic Coupling	Total Rel. Cost
			PD				
LR4	SMF	10km	PIN	SiGe	Req	Active	1
PSM4	SMF	500m	PIN	CMOS 1-chip CDR	NR	Passive*	0.35
SR4	MMF	100m	PIN	CMOS	NR	Passive	<0.35

NR: Not Required

* Design Target

PSM4 transceiver cost analysis, relative to 100GBASE-LR4 and SR4.

Component	100G-LR4	100G-PSM4	100G-SR4
TOSA + LDD + O-mux	1	0.2**	< 0.2**
ROSA + TIA + O-demux	1	0.35	<0.35
CDR IC	1	1	1
MISC: DC-DC, uC, packaging Assembly & Test	1	1	1
Total	1	0.43	< 0.43

* Transceiver Relative Cost Model based past product development experience. Actual cost model varies by PMD type, transceiver design, generation and manufacturing process.

** Decrease including results from reduced parameter set testing.

Summary

- An update on the 4x 25 Gb/s parallel single mode (PSM4) technology and relative cost analysis has been presented.
- Relative cost analysis indicates ~60% optical transceiver cost reduction in a short reach 500m SMF link is achievable with the PSM4 approach, compared with the current 100GBASE-LR4.

End of Presentation

Thanks!