

PAM8 Baseline Proposal

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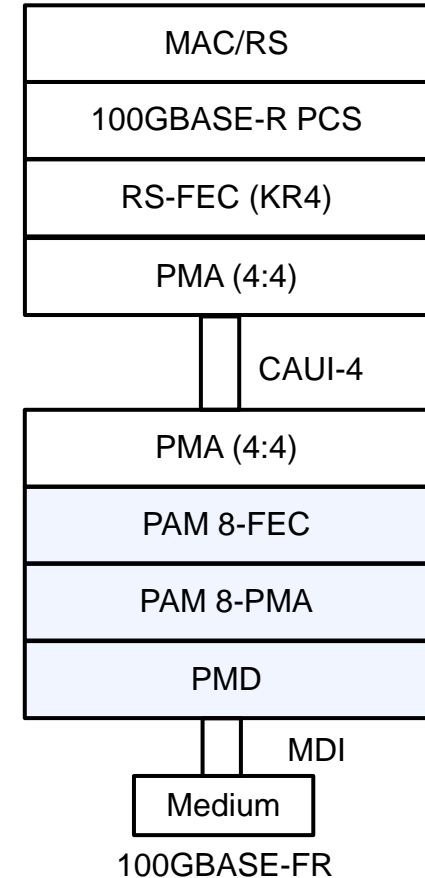
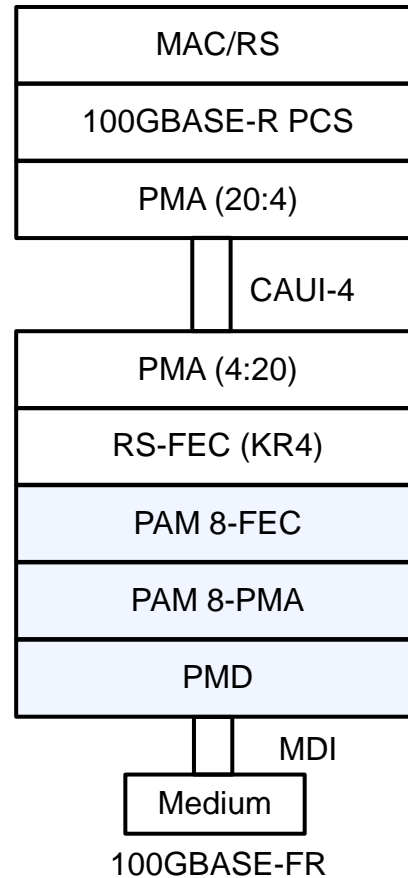
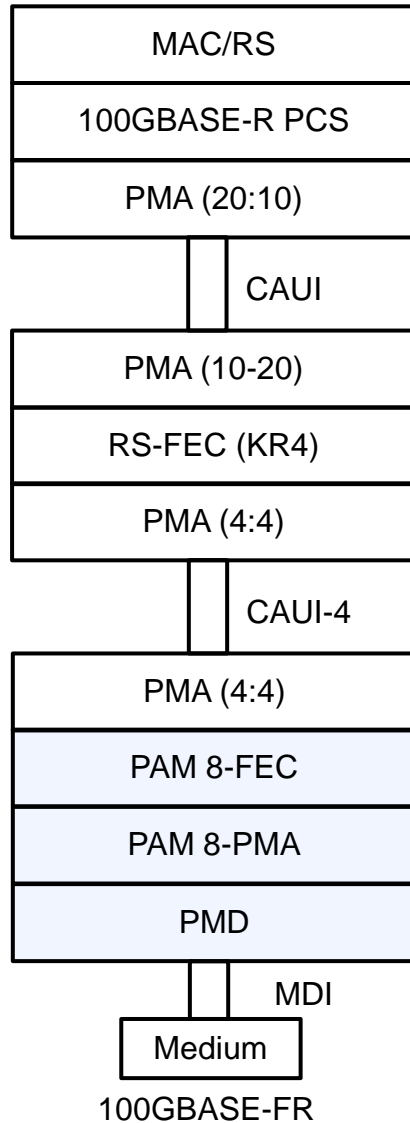
Supporters

- Dave Lewis, JDSU
- Beck Mason, JDSU
- Torben Nielsen, Acacia
- Dan Stevens, Fujitsu Semiconductor

Introduction

- One of P802.3bm adopted objectives :
 - *“Define a 100 Gb/s PHY for operation up to at least 500m of SMF”*
- PAM PMD has been discussed as a cost-efficient solution in previous meetings.
- PAM8 PMD is proposed here
 - Single laser, Externally Modulated
 - Link budget up to 4 dB
 - Link reach 500 m
 - ✓ Longer reach may be feasible.
- Link transmit and receive characteristics and illustrative link budget are presented

802.3 Architecture Options



 = New Functionality

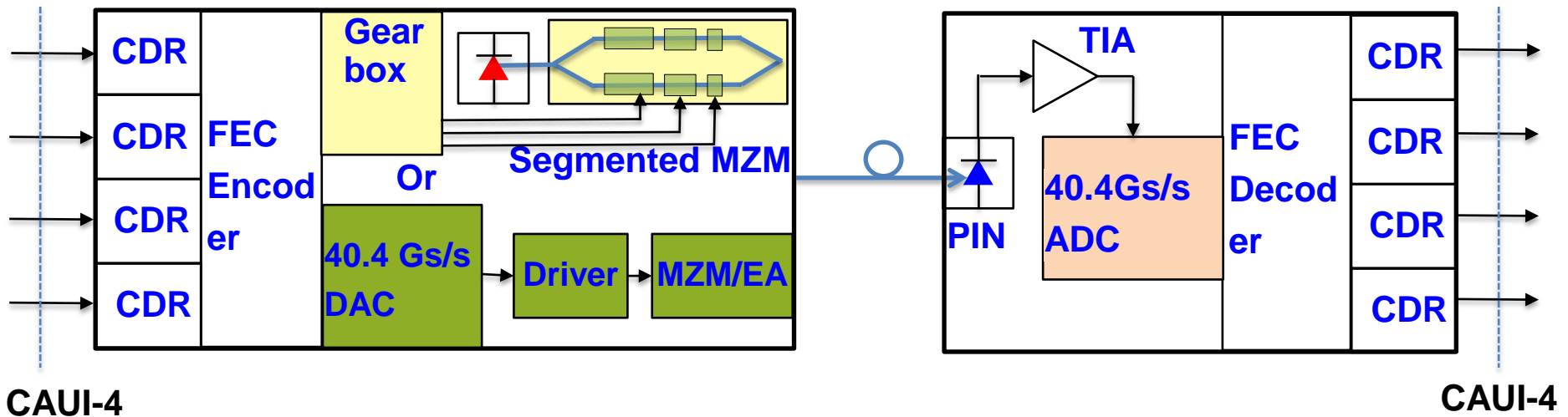
PAM 8-FEC: PAM 8 FEC and Mapping

PAM 8-PMA: PAM 8 Physical Media Attach (Serdes)

100GBASE-FR: 500m, SMF, Single Lambda

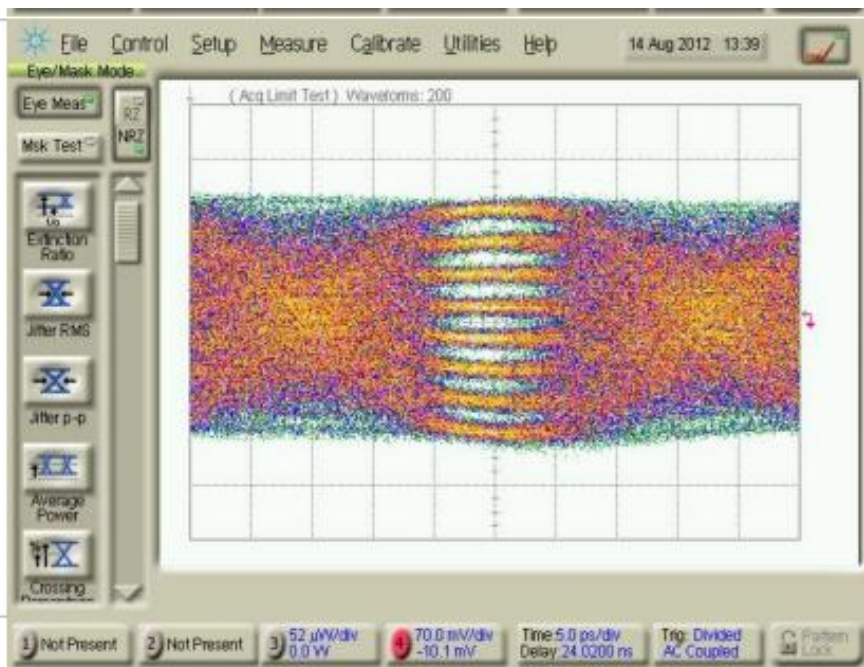
PAM-8 Block Diagram

- Showing segmented modulator and traditional MZM/EA



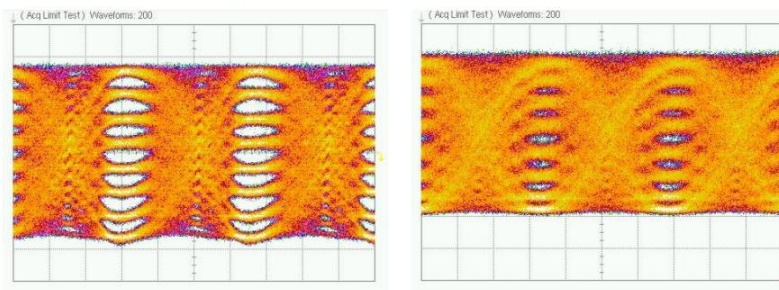
PAM8 Measurements

32 Gbaud, 8 PAM electrical eye, using DAC



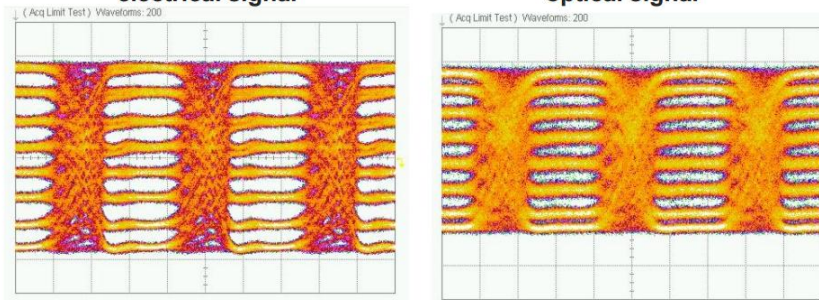
http://www.ieee802.org/3/bm/public/sep12/lewis_01_0912_optx.pdf

electrical signal 28 Gbaud optical signal



10 Gbaud

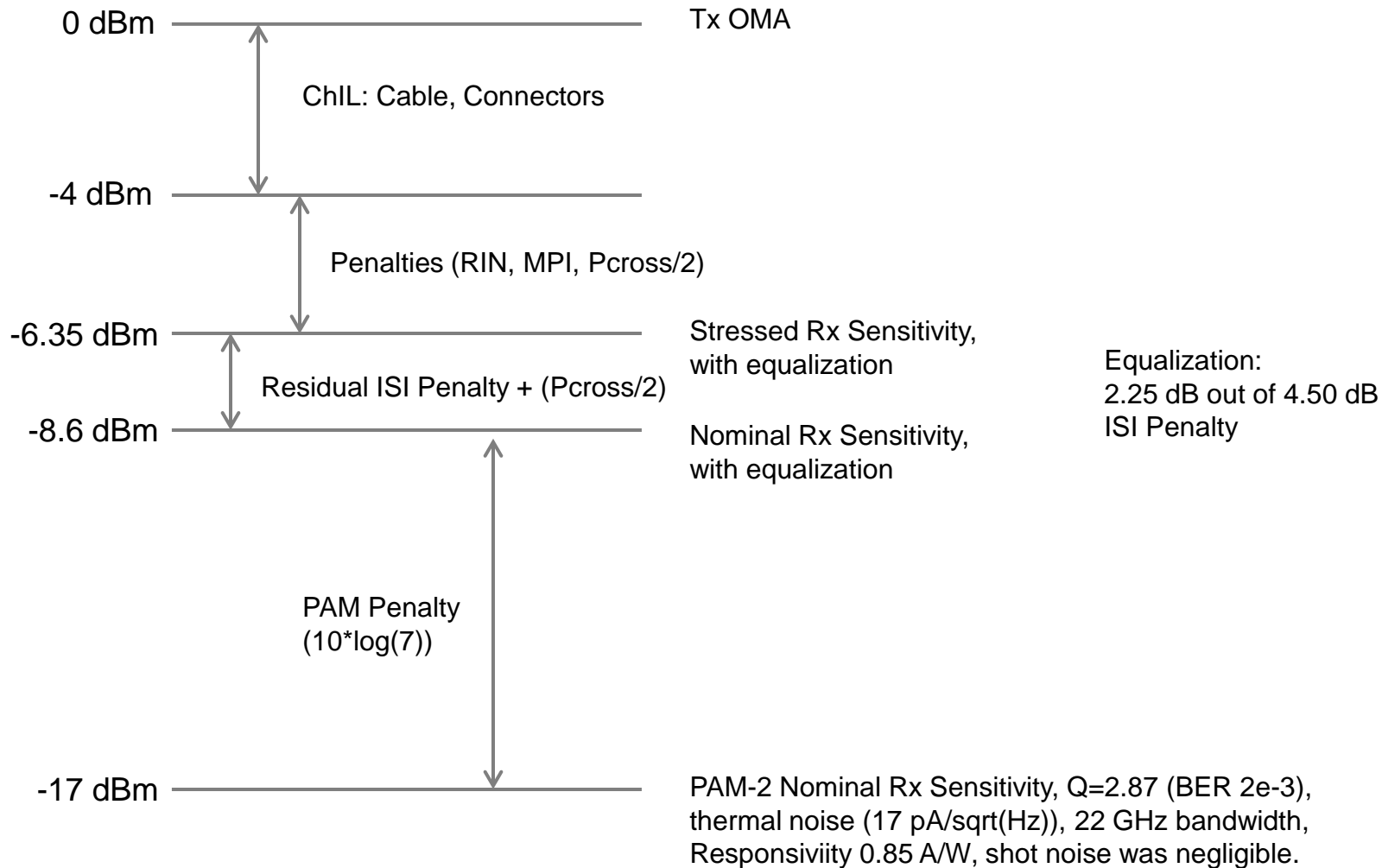
electrical signal optical signal



http://www.ieee802.org/3/100GNGOPTX/public/jul12/schell_01_0712_optx.pdf

- PAM-8 measurements results have been presented at .bm
- EML is used as light source and external modulator

PAM-8 Link Budget



Transmitter Characteristics

Parameter		Unit
Electrical Baud Rate (per Lane)	25.78125	
Optical Baud Rate (per Lane)	40.4296875	GBd
Modulation	PAM-8	
Center Wavelength, min	1300	nm
Center Wavelength, max	1320	nm
OMA, min	0	dBm
Extinction Ratio, min	6	dB
RIN	-142	dB/Hz
Transmitter reflectance	-35	dB

Transmitter Output Jitter

Parameter	Limit	Test Pattern Condition	Unit
TWDP ¹	2	PRBS15	dBo
Qsq (linear)	32	68.6.7	NA
DCD	0.035	Clock 8 ones/8 zeros	UI
Effective Random Jitter (1σ) ^{1,2}	0.015	PN15 PAM-2	UI
Effective Deterministic Jitter (p-p) ^{1,2}	0.15	PN15 PAM-2	UI

1. Waveforms and jitter are captured with reference CDR having loop BW of $F_{\text{baud}}/40430$

2. Effective random jitter and deterministic jitter is the Dual-Dirac fitted parameters from $Q=2$ to $Q=5$ with minimum of 64 kbits of samples or equivalent edges

Transmitter Testing

- Use a modified version of the Transmitter Waveform and Dispersion Penalty method (Clause 68.6.6)
- Computes penalty for deterministic impairments
 - Capture digitized transmitter output (for example, on scope)
 - Average over several cycles of PRBS to remove noise
 - Compute SNR for an ideal matched filter receiver with ideal rectangular PAM constellation (reference SNR)
 - Process waveform through a channel model and reference receiver
 - Compute semi-analytic BER assuming a given level of receiver noise
 - Convert to equivalent SNR for ideal waveform and ideal receiver
 - Penalty is difference between equivalent SNR and reference SNR
- Set a maximum limit on TWDP

Receiver Characteristics

Parameter		Unit
Rate	40.4296875 Gs/s	GBd
Modulation	PAM-8	
Wavelength Range	1302 – 1322	nm
Rx Avg. Power (max)	2	dBm
Rx reflectance	-35	dB

Parameter	Limit	Test Pattern Condition	Unit
Stressed Rx Sensitivity (OMA)	-6.35	PN31	dBo
Rx Sensitivity unstressed (OMA) ¹	-8.6	PN31, PAM-2	dBo
Receiver CDR tracking unstressed	(1, 75)	PN31, PAM-2	(UI, kHz)
Receiver CDR tracking unstressed	(0.2, 375)	PN31, PAM-2	(UI, kHz)

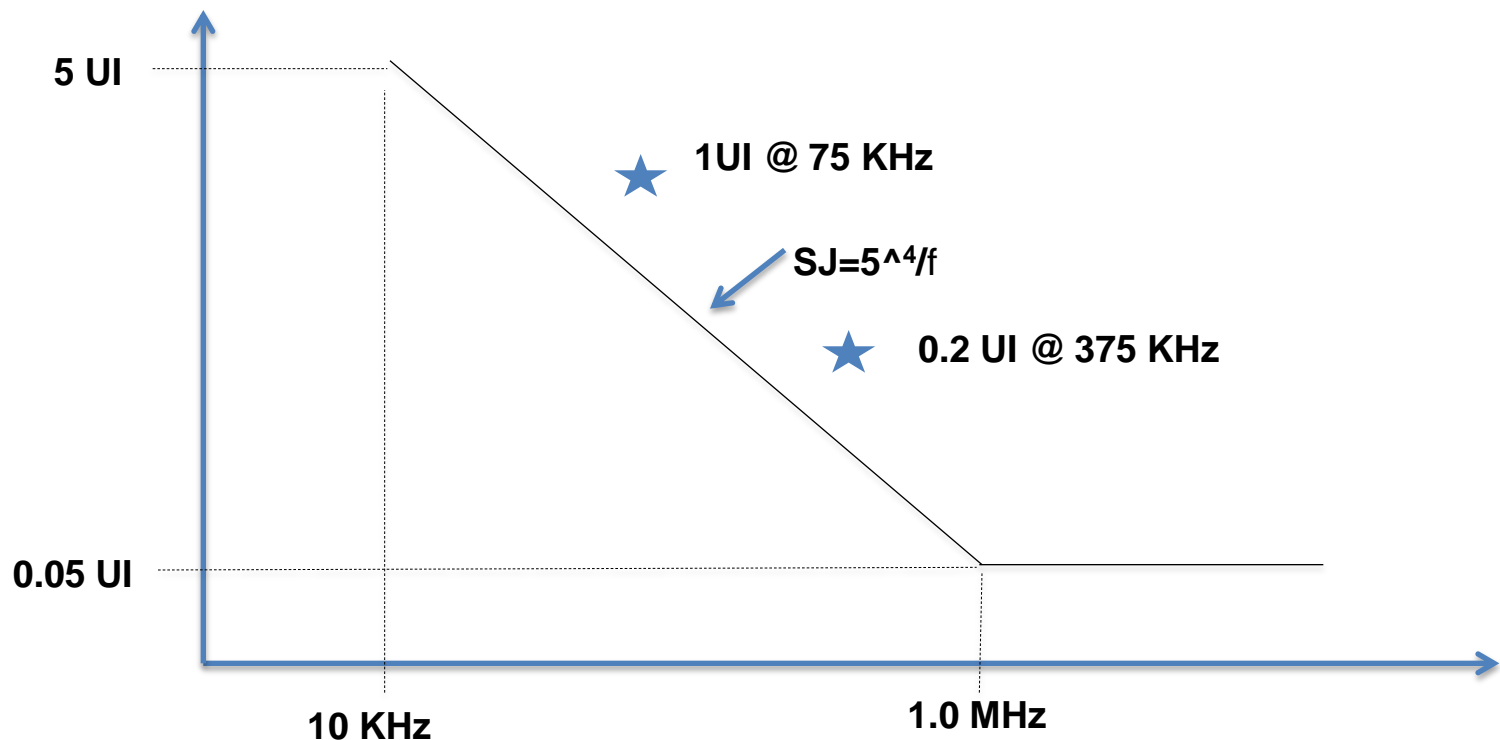
1. Tested with reference transmitter operating in PAM-2 mode with Q = 2.87, adjusted for PAM Penalty

SJ Tolerance Mask

- Receiver is tested unstressed with PAM-2 signal similar to 10Gbase-LRM assuming TX golden CDR having response as shown and slope of $5e4/f$

1 UI @ 75 KHz (~ 1.5 the TX CDR would allow)

0.2 UI @ 375 KHz (~ 1.5x the TX CDR would allow)



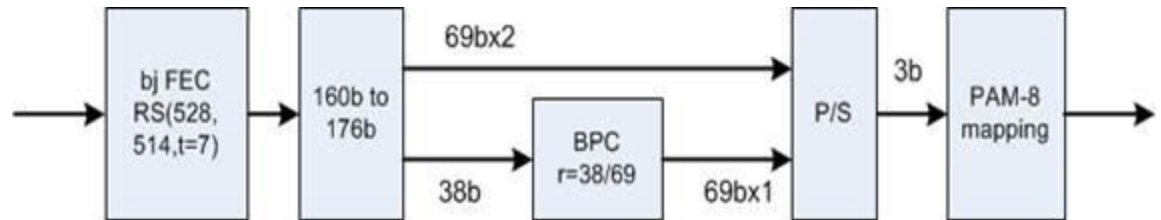
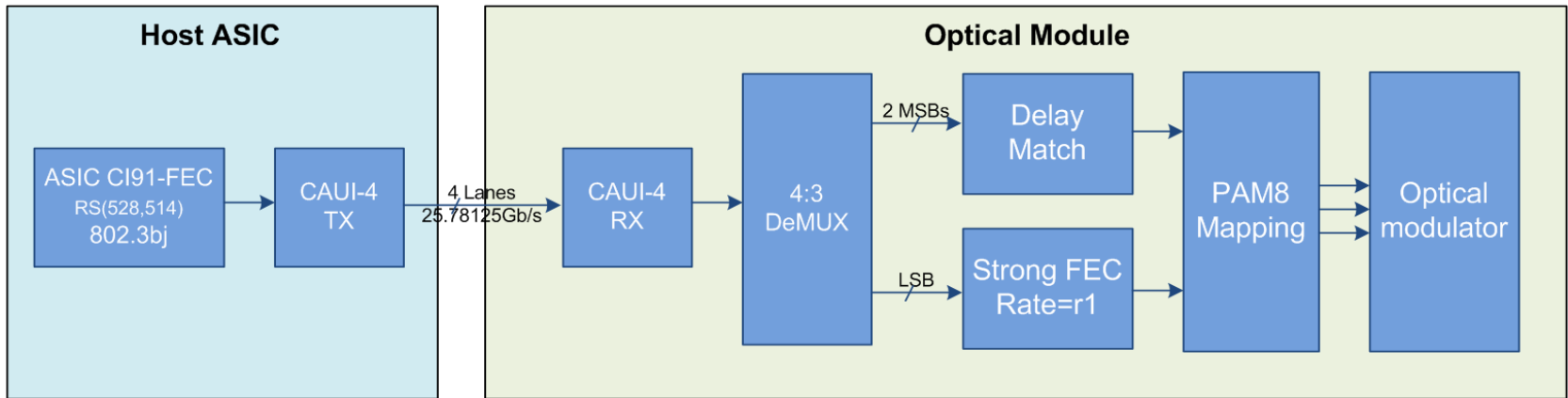
Channel Characteristics

Description	Value	Unit
Operating Distance (max)	500	m
Channel Insertion Loss (max)	4	dB
Positive Dispersion (max)	1.0	ps/nm
Negative Dispersion (max)	-2.0	ps/nm
Optical Return Loss (min)*	29	dB

* Based on 35 dB RL for connectors per ISO/IEC 11801, dual-trunk architecture model having up to 8 connectors with a mix of APC and non-APC types.

Multilevel Coding using bj FEC

Pushing the bj FEC into the host ASIC



Low-Latency PAM-8 Strong FEC Proposal

- Block size: 8280
- Code Rate: 119/207
- Number of Extra OH bits: 200
- Code rate including extra OH: 38/69 (Approximately 0.55)

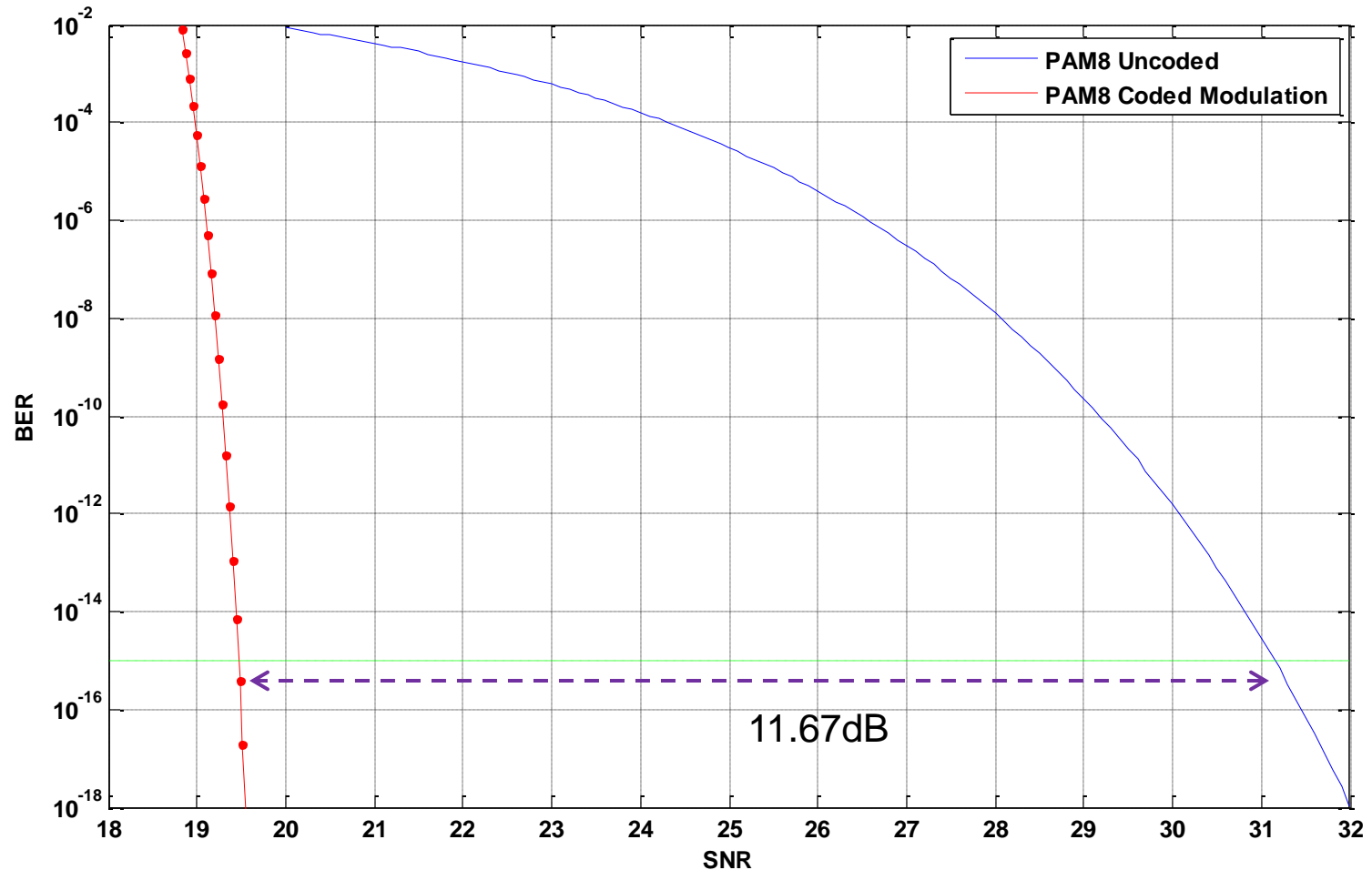
- Spectral Efficiency (Excluding bj FEC): $1+1+38/69=176/69$ (Approximately 2.55)
- Baud-Rate= $103.125*69/176=40.4296875$ Gs/s

- CAUI-4 clock to PAM-8 clock conversion ratio: **69/44**
 - This is a simple multiple of 156.25MHz. 100G Base KP4 is using a similar 2 digit ratio

- PAM-8 SNR for 1E-15 BER: **19.6dB**
 - The 6dB Set-Partition gain does not fully materialize because some of the optical noise sources are amplitude dependent (such as RIN).
 - If the noise was AWGN, then the PAM-8 SNR for 1E-15 BER should have been 19.3dB. So there is a loss of 0.3dB due to non-AWGN noise effect

- Strong FEC Encoder latency: 25ns – 50ns
- Strong FEC Decoder latency: 305ns
- RS bj FEC Decoder latency : 100ns
 - If the RS FEC is integrated with strong FEC, this additional latency can be reduced to 45 ns.

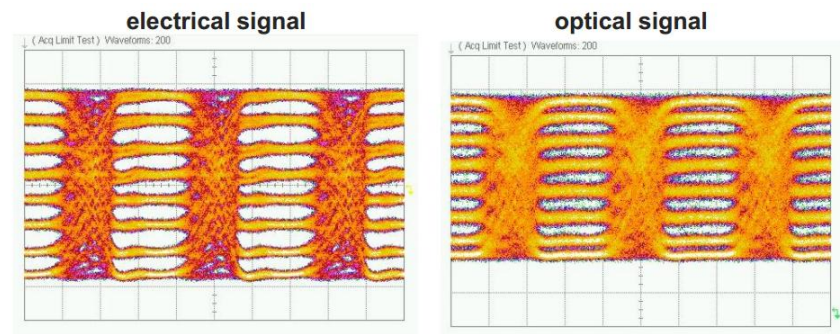
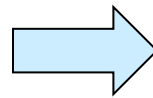
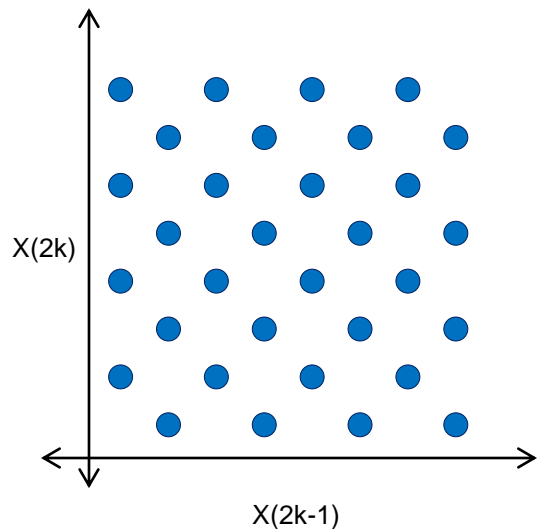
Example Coded Modulation Sim Results



- PAM8 coded modulation FEC delivers 11.67dB coding gain

FFS: Options to Reduce Latency

- DSQ32 is a 2-dimensional constellation mapping
- Constellation comprised of 32 PAM-8 points
- Data is encoded over 2 consecutive symbols
- Encoded signaling rate = 42.4GBd
- Latency < 150ns



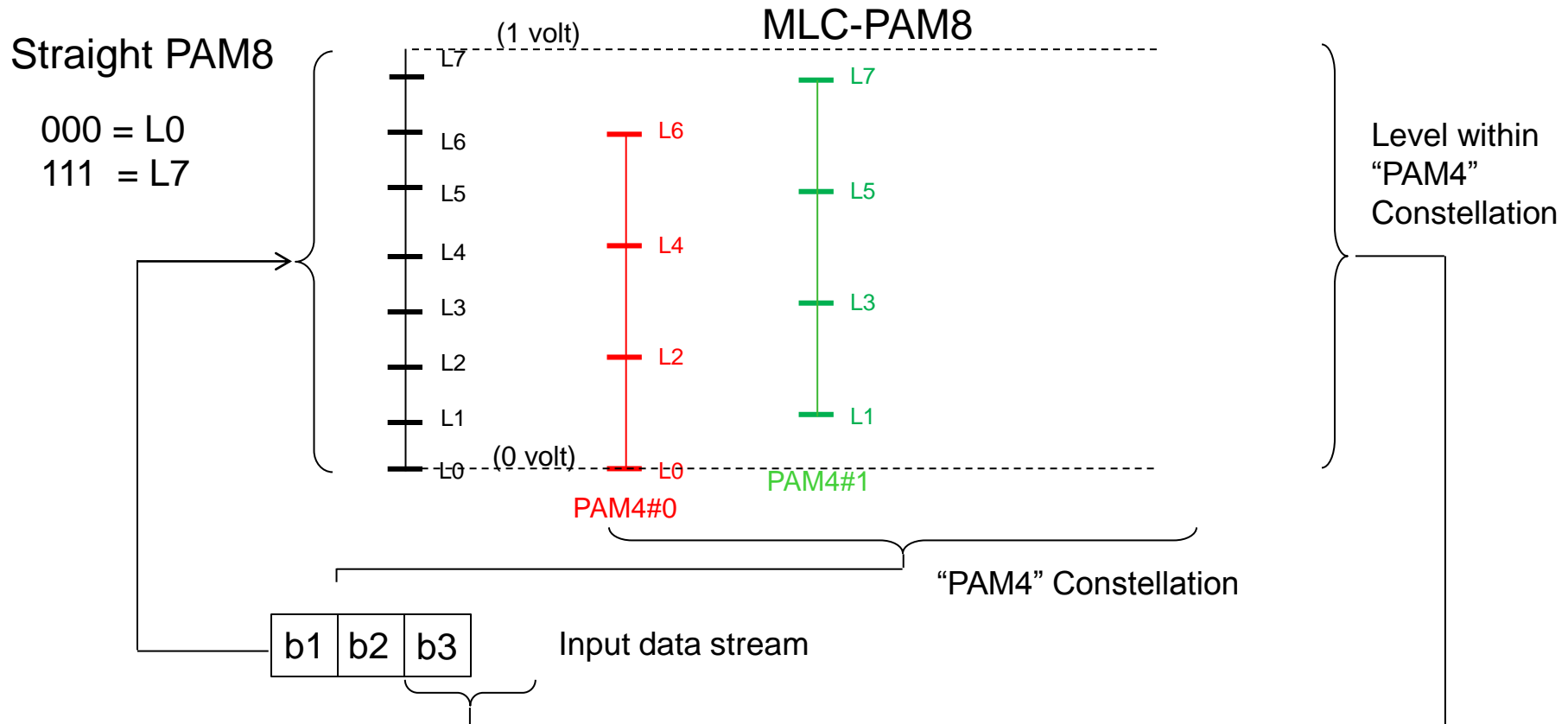
How constellation manifests as optical eye at TP2

Summary

- We have proposed a PAM8 solution to address 802.3bm 500 m SMF objective.
- Complexity transferred to digital CMOS.
- Simpler optics, single laser, low cost.

Backup

Multi Level Coding (MLC)



- MLC – Not all bits are equal. Focus FEC overhead/gain where it adds most value
- Treat one bit b1 as “PAM8”. Treat lower two bits (b2,b3) as “PAM4”
- Target all FEC overhead/gain to protecting the upper bit, and no FEC to lower two bits
- Enables higher FEC coding gain without bumping up the symbol (data) rate
- A 10% overhead FEC (on aggregate) results in 30% overhead FEC on upper bit