

# Feasibility of Unretimed 100Gbase-SR4

IEEE 802.3bm Task Force

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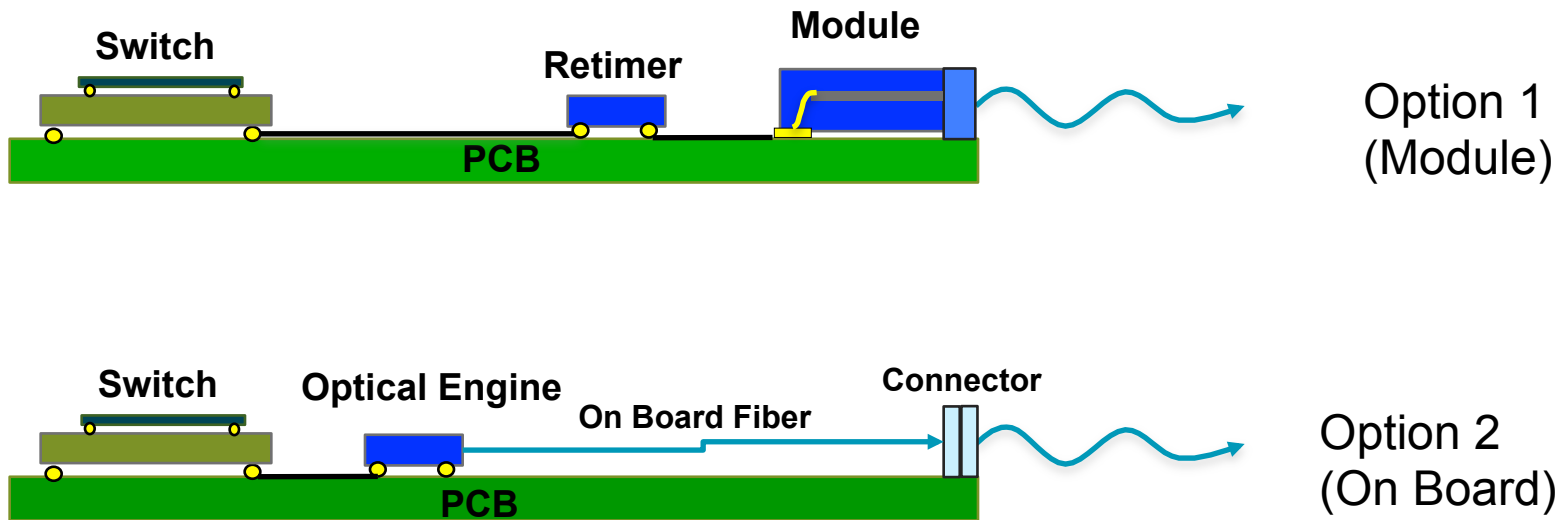
- Brad Booth – Dell
- Ahmet Balcioglu – Hittite
- Piers Dawe - IPtronics
- Oren Sleat – Mellanox

- Material presented here previously have been presented at one or more of the following venue
  - 100GNGOPTX task force
  - [http://www.ieee802.org/3/bm/public/nov12/ghiasi\\_02\\_1112\\_optx.pd](http://www.ieee802.org/3/bm/public/nov12/ghiasi_02_1112_optx.pd)
  - [‘Feasibility of Unretimed 100 GbE Based on 4x25. 78 GBd’](#), OWJ1.2, OFC 2012
  - IEEE Photonic Interconnect, ‘Enabling 850 nm VCSEL for 100 GbE Applications, Santa Fe, 2012
- There has been renewed interest in the low cost, low power, unretimed cPPI-4 interface for 20-30 m SR4 application and this presentation explores
  - Meeting transmitter TP1a jitter requirement
  - Example channels meeting cPPI-4
  - How to make limiting interface
- The key questions are
  - Does the 20 m SR4 PMD interoperate with 100 m SR4 PMD
  - Is FEC required
  - Is the interface limiting or linear

- 802.3bm objective defines PMD for operation up to 100 m which is retimed and uses FEC
- The 20 m objective was included to define lower power, cost, and size driven by data center applications
  - How do we address 20 m reach objective
- **Define re-timed 4-lane 100G PMA to PMA electrical interfaces for chip to chip and chip to module applications**
- **Define a 40 Gb/s PHY for operation over at least 40 km of SMF**
- **Define a 100 Gb/s PHY for operation up to at least 500 m of SMF**
- **Define a 100 Gb/s PHY for operation up to at least 100 m of MMF**
- **Define a 100 Gb/s PHY for operation up to at least 20 m of MMF**

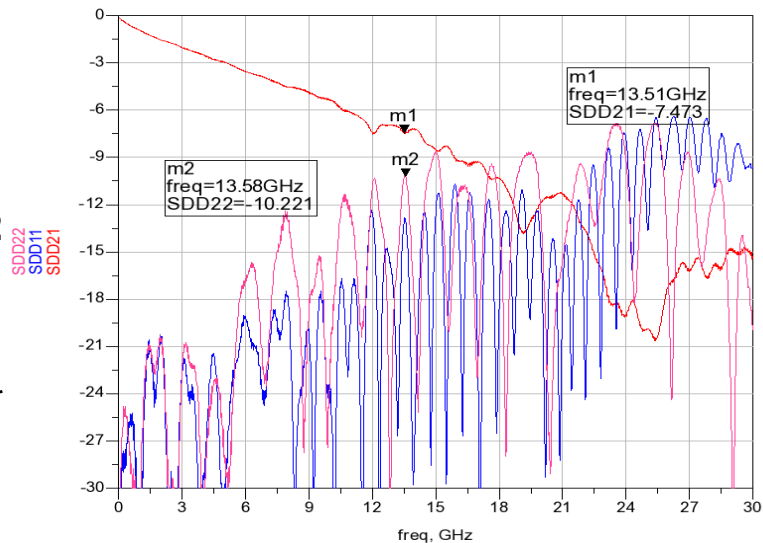
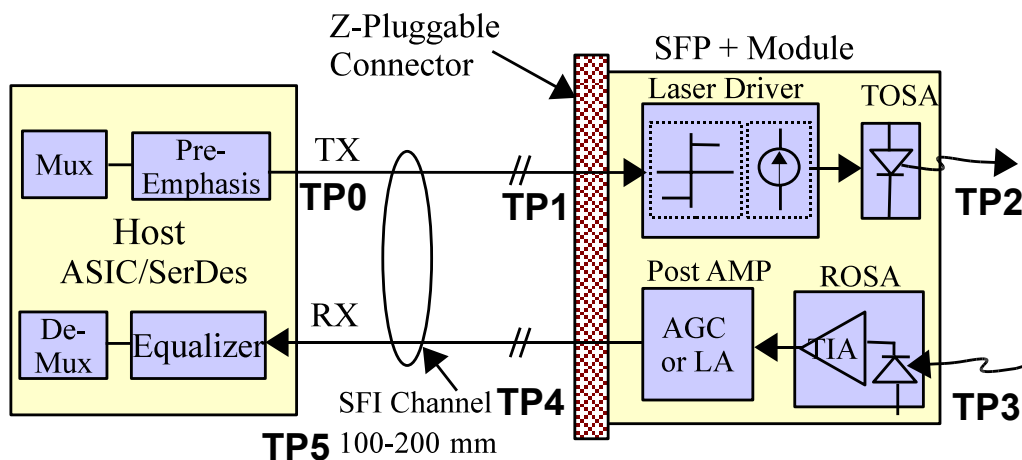
# Applications Reference Diagram

- Adding retimers increases the 100Gbase-SR4 power dissipation by  $\sim 2x$
- To support 100GBase-CR4 a retimer already exist in close proximity of the module

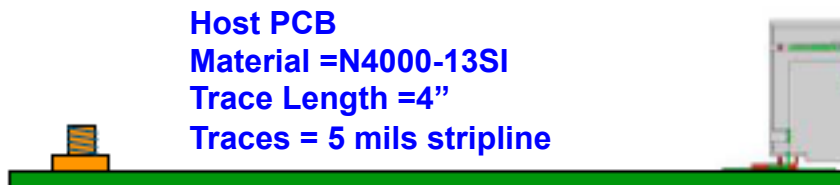


# Suitable Channel for Unretimed Application

- Channel has 7.4 dB loss at Nyquist



## Connector Quattro II



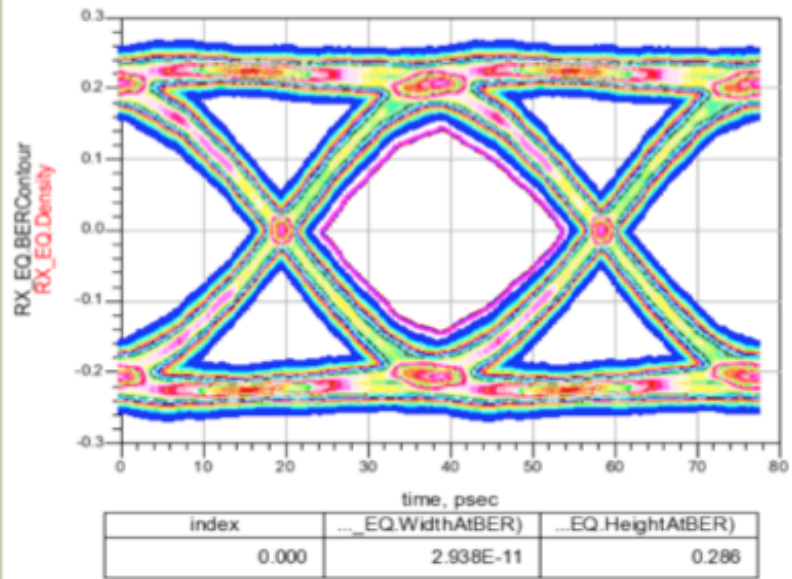
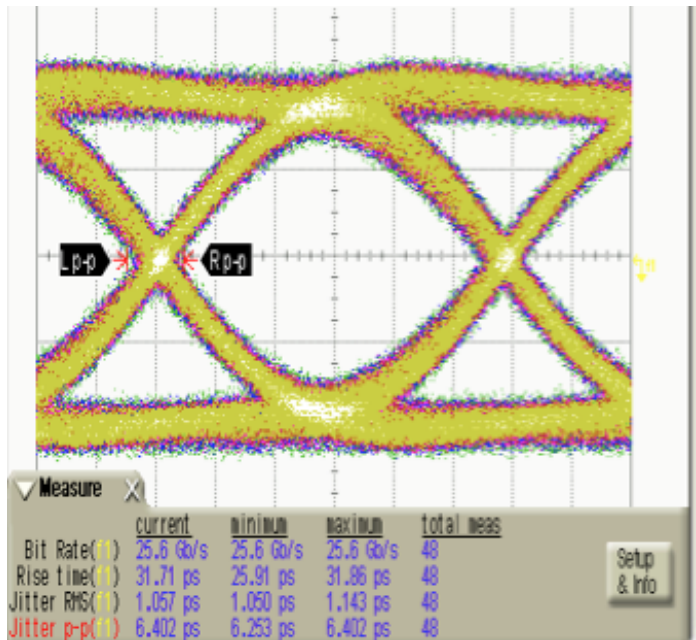
**Host PCB**  
**Material =N4000-13SI**  
**Trace Length =4"**  
**Traces = 5 mils stripline**



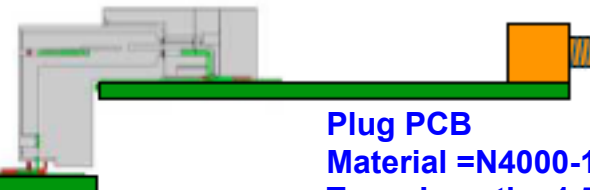
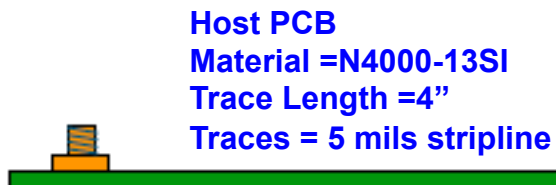
**Plug PCB**  
**Material =N4000-13SI**  
**Trace Length =1.5"**  
**Traces = 5 mils Microstrip**

# Far End Eye

- Measured and simulated eyes are good enough to drive the optics with  $<0.28$  UI of TJ at TP1a similar to SFP+!



## Connector Quattro II



- To make transmitter meeting DDPWS and J2 requirements the cPPI-4 channel would have to be  $\sim 7$  dB instead of 10.5 dB in case of CAUI-4
  - Still have 4 dB of host PCB allocation which equates to  $\sim 5''$  on Megtron-6
- In case of limiting interface an additional  $\sim 0.1$  UI of transmit and  $\sim 0.1$  UI of receive jitter must be found and the source of the improvement are
  - Reduction of fiber reach from 100 m to 20-30 m
  - Improvement of the SerDes
- To make linear module receiver work
  - Crosstalk does add some penalty but the fact one the host can now equalize for the fiber/Laser there is net gain
  - This interface DFE as result of MTTFPA the interface require at least FEC encoder and we might as well turn on
- With addition of FEC both limiting and linear interface become very feasible
- If we don't define unretimed interface in this group it will be defined by MSA's.



**Thank You**