100 GbE PAM Power Dissipation

IEEE 802.3bm Task Force

Ali Ghiasi, Zhongfeng Wang, and Vivek Telang - Broadcom

Jan 22-23, 2013

Phoenix, TX

List of supporters

- Vipul Bhatt – Cisco
- Gary Nicholl - Cisco
- Matt Traverso – Cisco
- Arash Farhood – Cortina
- Sudeep Bhoja – Inphi
- Andre Szczepanek – Inphi
- Beck Mason – JDS
- Brian Welch – Luxtera
- Chris Bergey – Luxtera

Overview

- Investigate unipolar PAM power dissipation
  - PAM-8 operating at 40.4 GBd
  - PAM-8 with DSQ-32 mapping operating at 42.4 GBd
- Key advantage of PAM are
  - Replaces high cost and power EO/OE components that do not evolve with more complex silicon which do evolve with Morse Law
  - Replaces WDM/CWDM components with single non-color laser
  - Follows the evolution of 10Gbase-LR
  - 1st generation implementation with segmented modulator will fit will fit QSFP28 class III (2.5 W) or CFP4 class II (3.0 W)
  - 1st generation implementation with standard MZM/EA still fits QSFP28 class IV (3.5 W) or CFP4 class II (3.0 W)
- PAM cost advantage analysis is given by http://www.ieee802.org/3/bm/public/jan13/welch_01_0113_optx.pdf

Do Nothing is not an Option

- Lack of unified 10G-SFP+ form is hammering 100 GbE
  - One of the key reason 100Gbase-bm project was started was defining a low power, cost, and size form factor based on SMF fibre with reach of 500 m
- 100 GbE has enormous problem addressing emerging high density line card applications
  - 100 GbE today can only support 4 CFP modules on a line card and even the next generation 100G module supports only 8 CFP2
  - The industry is waiting for cost and power optimized CFP4/QSFP28
- Factor limiting deployment of 100 GbE
  - Current 10x10G PMDs (100Gbase-SR4 will fill this void)
  - Lack of SMF datacenter optimized PMD with reach of 500 m
- With 100Gbase-SR4 having reach of <=100 m and 100Gbase-LR4 an overkill high cost PMD, these data centres will have to either stay with 40Gbase-xy lag or we will see proliferation of various PMD addressing the largest 100 GbE market!

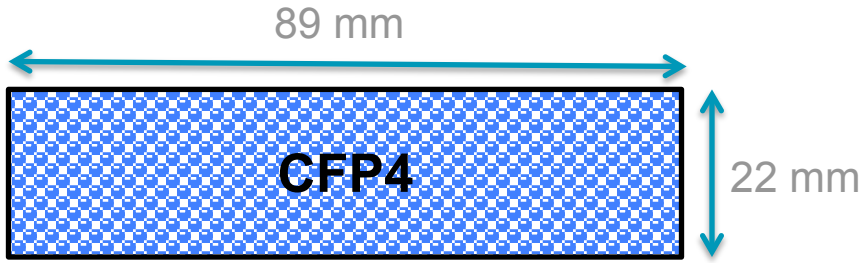
100Gbase-bm Objective

- Not defining a 500 m SMF PMD meeting the objective will be failure of the bm group!

- Define re-timed 4-lane 100G PMA to PMA electrical interfaces for chip to chip and chip to module applications
- Define a 40 Gb/s PHY for operation over at least 40 km of SMF
- Define a 100 Gb/s PHY for operation up to at least 500 m of SMF
- Define a 100 Gb/s PHY for operation up to at least 100 m of MMF
- Define a 100 Gb/s PHY for operation up to at least 20 m of MMF

Module Form Factors and Power Limit

- CFP4 size/pitch and PD
  - Class I – 1.5 W
  - Class II – 3.0 W
  - Class III – 4.5 W
  - Class IV – 6.0 W

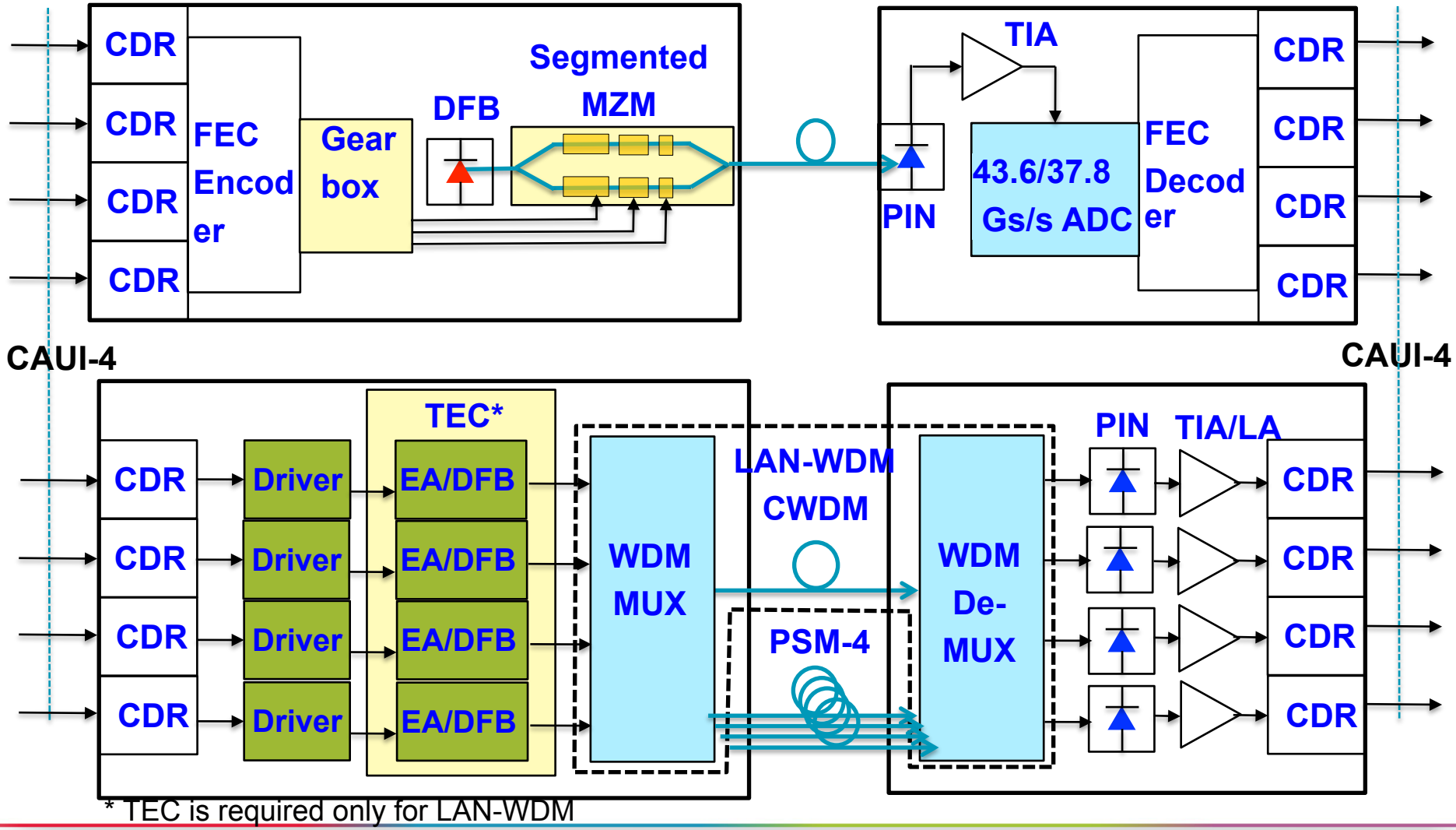


- QSFP28 size/pitch and PD
  - Class I – 1.5 W
  - Class II – 2.0 W
  - Class III – 2.5 W
  - Class IV – 3.5 W

- PAM PMD meeting QSFP28 Class III PD provides the most flexible implementation without the need for more complex cooling's

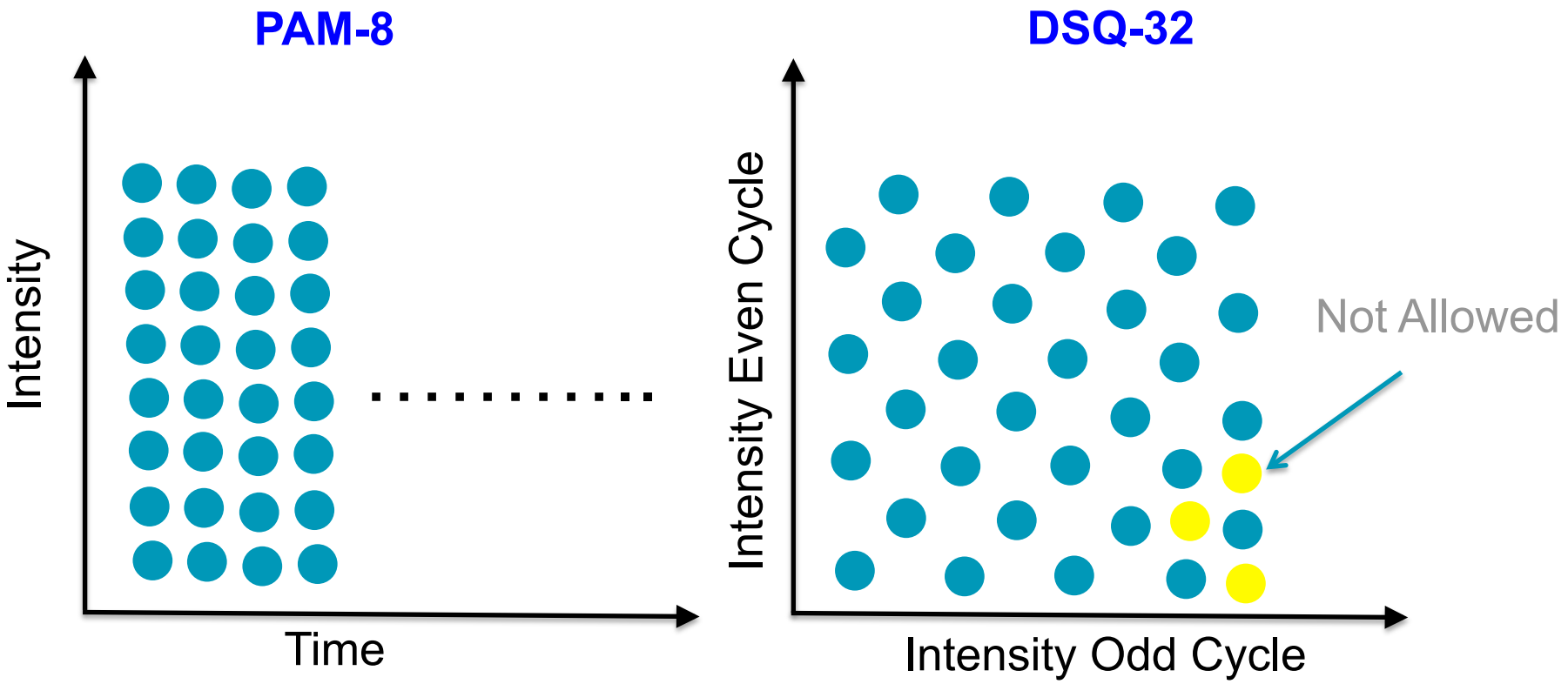
PAM Serial vs Parallel Implementation of 100 GbE

- LAN-WDM/CWDM and PSM4 have ~4x the components!



PAM-8 and DSQ-32 Mapping of PAM-8

- PAM-8 has 8 intensity levels
- DSQ-32 is a PAM-8 mapping with some constellation points restricted
  - For PAM-8 and DSQ-32 Baudrate and implementation see http://www.ieee802.org/3/bm/public/nov12/ghiasi_01a_1112_optx.pdf



PAM-8 and DSQ-32 Power Dissipation

- Both PAM-8 and DSQ-32 can fit with in the QSFP28 2.5 W class
- ADC and DAC power estimates based on http://www.slideshare.net/kennliu/fujitsu-iccad-presentationenable-100g?from=share_email and assuming 28 nm CMOS
  - Assuming PAM-8 DAC and ADC have ENOB of 6 bits
  - Assuming PAM-8 with DSQ-32 DAC and ADC have ENOB of 6 bits

Power Breakdown	PAM-8 @ 40.4 GBd		DSQ-32 @ 42.4 GBd	
	Std MZM	Seg MZM	Std MZM	Seg MZM
CAUI-4 System Interface (W)	0.80	0.80	0.80	0.80
Laser (W)	0.20	0.20	0.13	0.13
TEC (W)	0.00	0.00	0.00	0.00
Mod Driver or Segmented Driver (W)	0.80	0.25	0.80	0.25
DAC or Gearbox/Bitmux (W)	0.28	0.18	0.29	0.19
FEC (W)	0.35	0.35	0.25	0.25
TIA (W)	0.13	0.13	0.13	0.13
ADC (W)	0.59	0.59	0.54	0.54
Total PD (W)	3.1441	2.4968	2.9315	2.2806

Summary

- One of the key objective of the 802.3b was to define SMF PMD with reach of 500 m
  - Doing nothing will be a failure for this body
- PAM PMD can meet the more aggressive QSFP28 Class III (2.5W) PD in addition to CFP4
  - Will enable low cost stack line cards with 36 QSFP28 without any extra-ordinary cooling or the burden of going with belly-belly designs
- PAM PMD heavily leveraging CMOS technology node
  - With every node the PAM digital PD will be reduce by ~$\sqrt{2}$
  - PMD levering analog IC and/or multiple EO/OE PD is only reduced at much smaller increments
- Not defining SMF PMD addressing 500 m data center reach only will result in multiple MSA and market fragmentation!

Thank You