CAUI-4 chip to chip baseline discussion

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Ryan Latchman <ryan.latchman@mindspeed.com>
Ali Ghiasi aghiasi@broadcom.com
Mike Li <mpli@altera.com>

Supporters

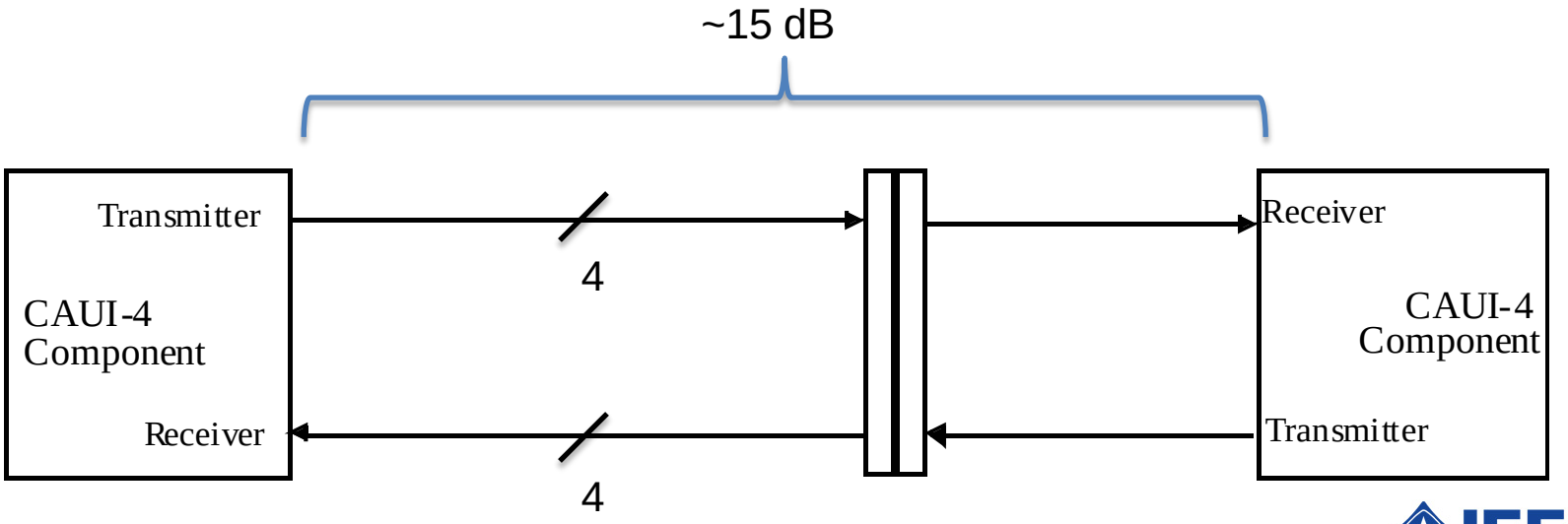
- Tom Palkert – Xilinx
- Mark Gustlin – Xilinx
- Rick Rabinovich – Alcatel Lucent
- Jonathan King - Finisar

Agenda

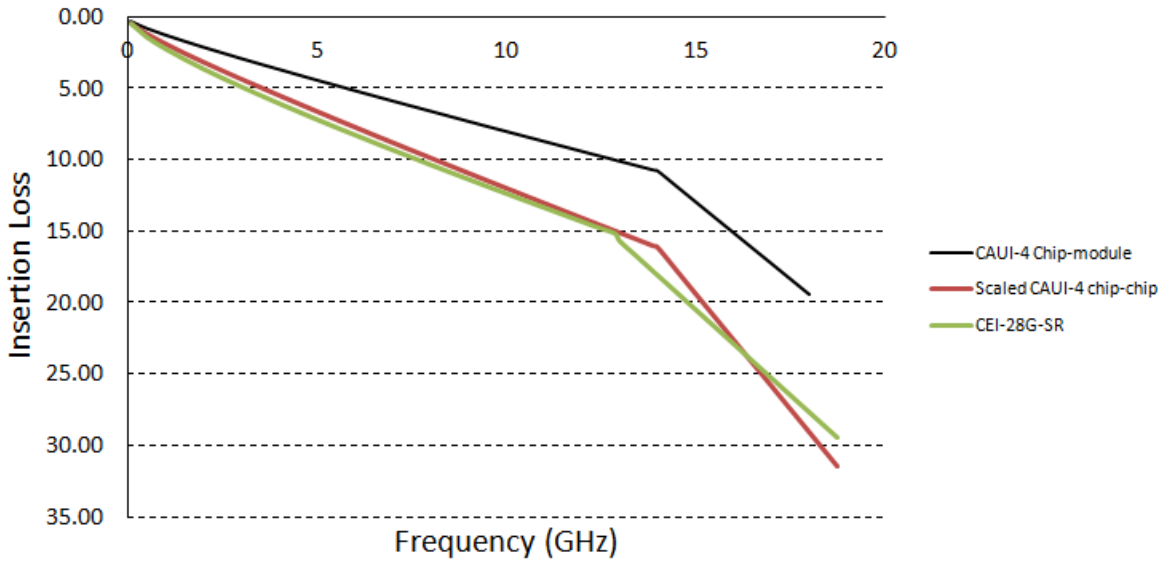
- Chip to chip spec discussion
  - Application space
  - Current Status with a view towards baseline
    - Channel
    - Transmitter
    - Receiver
  - Areas of focus

Application

- Chip to chip interface
  - Low power, low latency AC coupled interface between ICs running at 4 x 25.78Gb/s
    - No FEC, no transmitter training
  - ~15 dB loss target with 1 connector (connector is optional)
    - Consistent with 25cm reach target
    - See http://www.ieee802.org/3/bm/public/nov12/palkert_02_1112_optx.pdf, http://www.ieee802.org/3/bm/public/nov12/ghiasi_03_1112_optx.pdf
    - Higher loss channels also under analysis to enable longer links



Channel



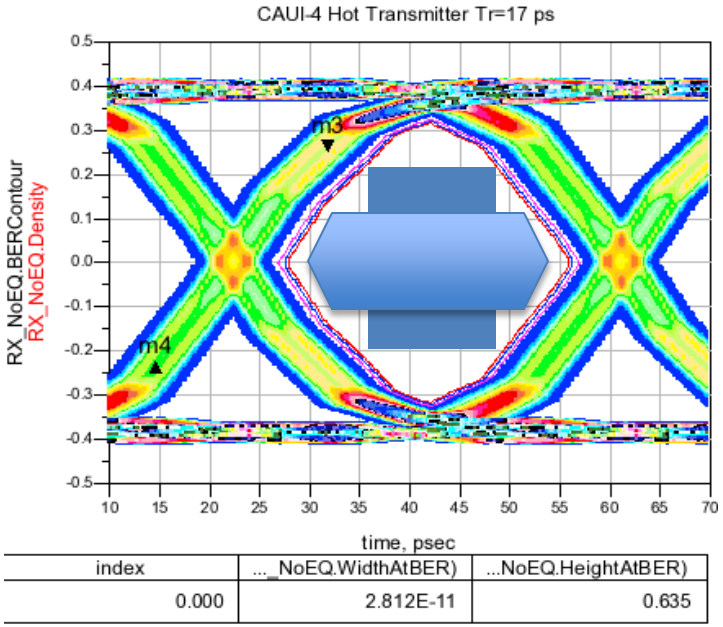
- Ensure robust MTTFPA
  - CTLE and/or restricted DFE limiting error propagation
  - No need for FEC for better latency and less power
  - 15dB+ channels under analysis
- Other channel parameters may include:
  - ILD, ICN, return-loss…
- Potential to leverage far end eye mask which will inherently limit channel parameters
- Potential to leverage COM similar to 802.3bj

CAUI-4 chip to chip transmitter considerations

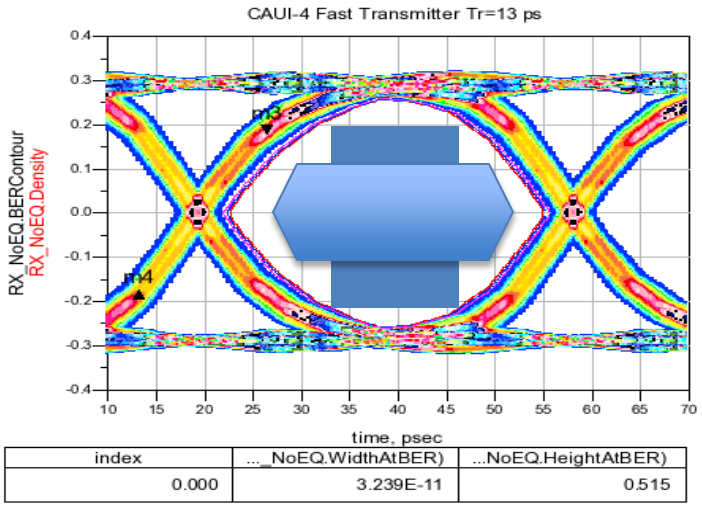
	KR4 (D1.3, TP0a)	MR	CAUI-4 chip to chip Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Differential peak-to-peak output voltage (max) with Tx disabled	30mV		30mVppd
Common Mode Voltage (max)	1.9V	1.7V	1.9V
Common Mode Voltage (min)	0V	-0.1V	0V
Differential output return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= 12-0.5*f for 0.01<=f<=8 GHz 5.65 - 9.71*log10(f/14) from 8<=f<=19 GHz
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=13GHz	-6dB , f<10GHz -4dB, 10G<f<25.78125GHz	RL(f) > 8-0.5*f for 0.01<=f<=8 GHz 1.65 - 9.71*log10(f/14) from 8<=f<=19 GHz
Common-mode AC output voltage (max,rms)	12mV	12mV	12mV
Amplitude peak-to-peak (max)	1200mV	1200mV	1200mV
Transition Time (20%-80%, min, no EQ)	8ps	8ps	8ps
Output eye mask			TBD
De-emphasis range			TBD

CAUI-4 chip to chip transmitter considerations

- Define near end eye mask at TP0a
  - Allow transmitters to trade-off amplitude, rise/fall time, and jitter (potentially using a square mask)
  - No (or default) de-emphasis
  - X1, X2, Y1, Y2 (TBD right now) with consideration given to both square and hexagonal masks



index	..._NoEQ.WidthAtBER)	...NoEQ.HeightAtBER)
0.000	2.812E-11	0.635



index	..._NoEQ.WidthAtBER)	...NoEQ.HeightAtBER)
0.000	3.239E-11	0.515

- Define de-emphasis range
  - Potential to make requirement dependent on rise/fall time similar to Annex 83A
- Define far end mask at ~TP5
  - Lumps transmitter and channel parameters into a far end mask with reference CTLE (similar to CAUI4 chip-module)

CAUI-4 chip to chip receiver considerations

	KR4 (D1.3, TP5a)	MR	CAUI-4 chip to chip Potential
Differential Input Return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= 12-0.5*f for 0.01<=f<=8 GHz 5.65 - 9.71*log10(f/14) from 8<=f<=19 GHz
Differential to common-mode return loss (min)	RL(f) >= 20-1.44*f for 0.01<=f<=6.95 15 from 6.95<=f<=13		TBD
Input Differential Voltage (max)		1200	1200mV
Differential Impedance		80ohms min, 100ohms typical, 120ohms max	TBD
Input Impedance Mismatch (max)		10%	TBD
Input common mode voltage		-200mV (min), 1800mV (max)	TBD

Receiver Interference Tolerance

Parameter	Test values
Maximum BER*	10^{-12}
Channel Insertion Loss at 12.89GHz	~15dB
Applied peak-to-peak sinusoidal jitter	TBD
Applied peak-to-peak random jitter	TBD
Applied even-odd jitter	TBD
Applied RMS broadband noise	TBD

* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Compliance points

- **See 93.8.2.1 Receiver test fixture from 802.3bj for TP5a**
- **See 93.8.1.1 Transmitter test fixture from 802.3bj for TP0a**
- **May need additional compliance point for far end eye mask if that is specified**
  - **Would require implementation specific break out board**