FEC Coding and Analysis for 100G PAM8 System

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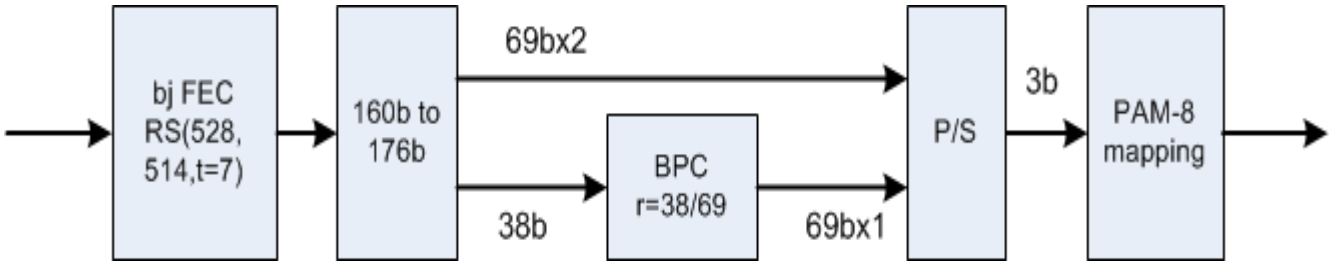
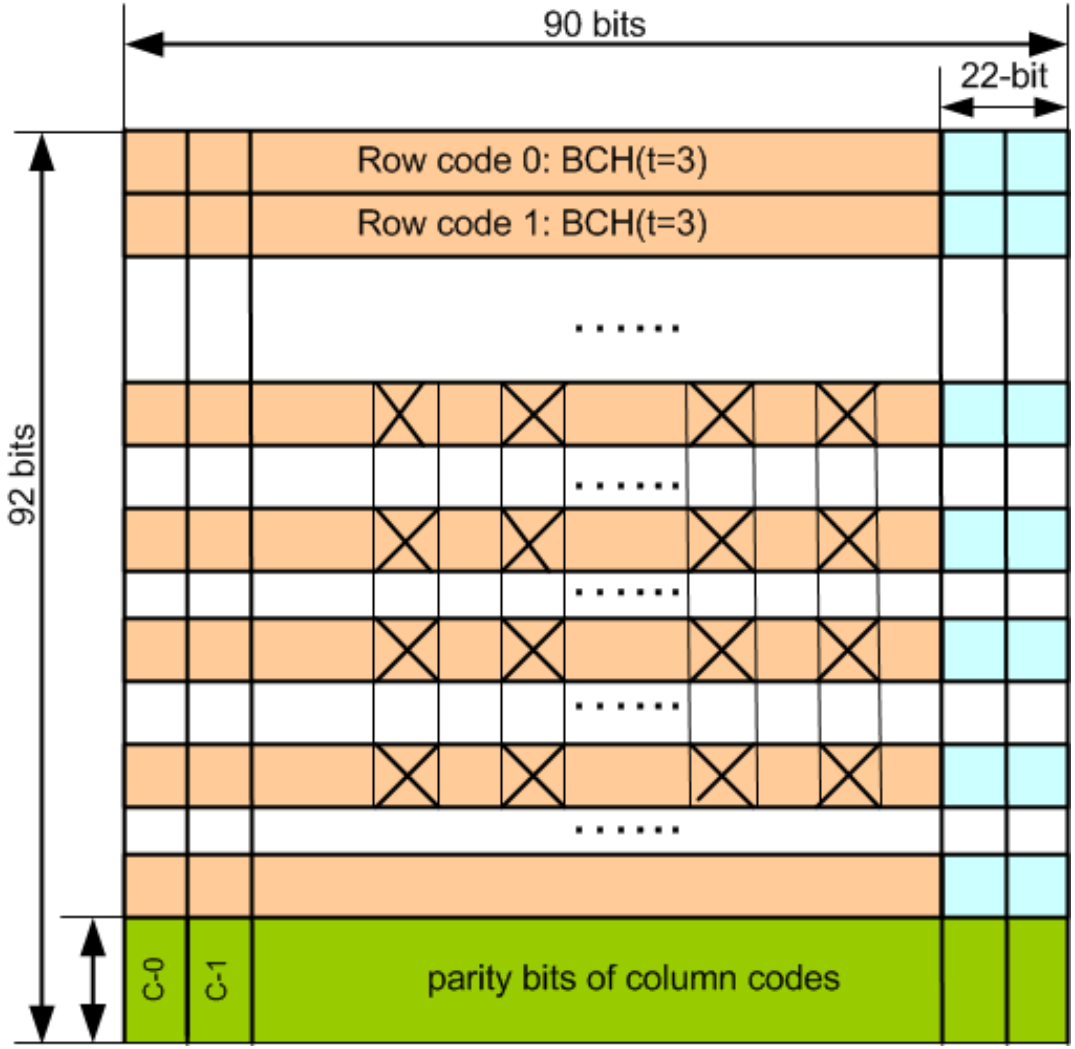
Strong FEC for PAM8 System



- In the PAM8 baseline proposal (802.3bm, Jan 2013), some parameters are specified for the strong FEC:
  - Block size: 8280 bits
  - Raw code rate: 119/207
  - Net code rate: 38/69 (200 dummy bits are included at input)

- Consider a true-product code (TrPC): BCH(92, 70, t=3) x BCH(90, 68, t=3) with 200 dummy bits. This code satisfied all the above specifications.
  - Block size: 92x90=8280
  - Raw code rate: 68x70/90/92= 119/207
  - Net code rate: (68x70-200)/92/90=38/69

Code Matrix for Product Codes



Strong FEC Analysis

- For a product code, using BCH(t=3) as component code is a common practice. It has been well studied before and is an optimal choice in general for true product codes.
- Adding one extra parity bit for each component code can reduce false decoding probability. Multiplying the regular BCH(t=3) code generate polynomial Go(x) by (x+1) can build the extended BCH code generate polynomial Ge(x).
- Any product code may have error flaring issue. But the error floor of a true product code can be generally made very low,
  e.g., BERo < 1e-20.
- The net coding gain for the candidate code is larger than 11 dB at target BER=1e-15. Detailed simulation will be provided later.

Alternate FEC Options

- There are other TrPC options:
  - Use TrPC: BCH(90, 66, t=3) x BCH(92, 70, t=3) with 60 dummy bits
  - Use TrPC: BCH(92, 68, t=3) x BCH(90, 68, t=3) with 64 dummy bits,
  - Use TrPC: BCH(90, 67, t=3) x BCH(92, 69, t=3) with 63 dummy bits
  - Adding more extra parity bits to component codes can reduce false decoding probability even further and thus improve the decoding performance slightly.

- Pseudo-product codes (PsPCs) are also interesting
  - Use PsPC: BCH(180, 132, t=6) x BCH(92, 70, t=3) with 63 dummy bits, where each row code covers 2 rows in the code matrix
  - Use PsPC, BCH(368, 269, t=11) x BCH(90, 68, t=3) with 13 dummy bits, where each row code covers 4 rows in the code matrix
    - ✓ Achieve about 8.5dB coding gain in low-latency mode or about 12 dB in high-latency mode.

- Non-orthogonally intersected product codes
  - For this kind of product codes, two dimensional component codes intercross each other in a non-orthogonal way from code matrix perspective.
  - Error flaring in this case may be an issue.

Decoding of Product Codes

- Product codes are iteratively decoded.
- In general, column decoding is performed first in order to minimize false decoding caused by burst errors.
- With more extra parity bits are added to row codes, row decoding can be undertaken first, which will save half iteration of time, which is significant if maximum number of iterations is limited to a few due to very high-throughput requirement.

Summary

- We have shown some promising candidate FEC codes that satisfied the current specifications for the strong FEC in the PAM8 baseline proposal.
- We will continue study to obtain more accurate estimation for the coding gain and error floor for each candidate code.
- We will explore other candidate FEC codes as well.