

CAUI-4 Chip-Chip Baseline

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Agenda

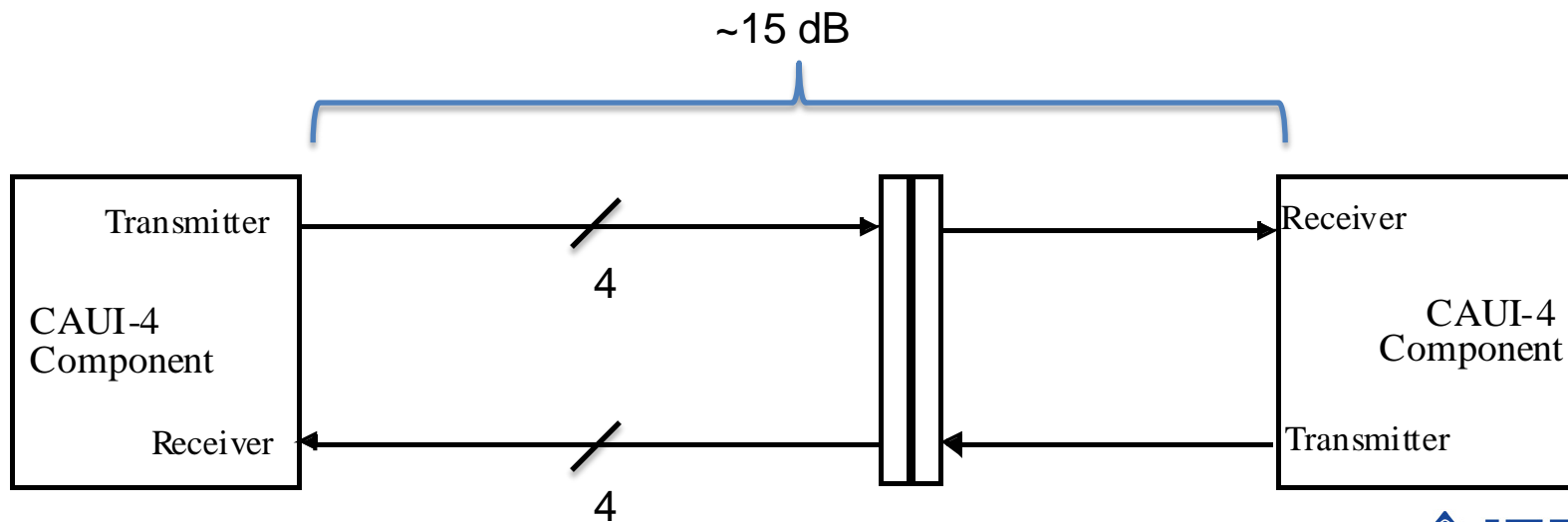
- Supporters / Contributors
- Chip to chip draft baseline
 - Application
 - Transmitter
 - Channel
 - Receiver
 - Interference tolerance
 - Compliance points

Supporters / Contributors

- Mike Li, Altera
- Ali Ghiasi, Broadcom
- Andre Szczepanek, Inphi
- Charles Moore, Avago
- Rick Rabinovich, Alcatel Lucent
- Brian Misek, Avago
- David Warren, HP

Application

- Chip to chip interface
 - Low power, low latency, AC coupled interface between ICs running at 4 x 25.78Gb/s
 - No FEC, No-DFE/or limited DFE (e.g., 1-tap or analog), no transmitter training
 - ~15 dB loss target with 1 connector (connector is optional)
 - Consistent with 25cm reach target
 - See http://www.ieee802.org/3/bm/public/nov12/palkert_02_1112_optx.pdf, http://www.ieee802.org/3/bm/public/nov12/ghiasi_03_1112_optx.pdf
 - Higher loss channels also under analysis to enable longer links



CAUI-4 chip to chip transmitter baseline

	KR4 (D1.4, TP0a)	CAUI-4 chip to chip Potential								
Signaling rate, per lane	25.78125+/-100ppm	25.78125+/-100ppm								
Differential peak-to-peak output voltage (max) with Tx disabled	30mV	30mVppd								
Common Mode Voltage (max)	1.9V	1.9V								
Common Mode Voltage (min)	0V	0V								
Differential output return loss (min)	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz	RL(f) >= 12.05-f for 0.05<=f<=6 GHz 6.45 – 0.075f from 6<f<=19 GHz								
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=19GHz	RL(f)>= 6dB, 0.05<=f<=19GHz								
Common-mode AC output voltage (max,rms)	12mV	12mV								
Amplitude peak-to-peak (max)	1200mV	1200mV								
Transition Time (20%-80%, min, no EQ)	8ps	8ps								
Output Jitter (max)										
DJ	0.15 (excluding DDJ)	0.15 (with reference CTLE)								
RJ	0.15	0.15								
TJ	0.28 (excluding DDJ)	0.28 (BER TBD, with reference CTLE)								
Output waveform	<table border="1"> <tbody> <tr> <td>steady state voltage vf (max)</td> <td>0.6</td> </tr> <tr> <td>steady state voltage vf (min)</td> <td>0.4</td> </tr> <tr> <td>linear fit pulse peak (min)</td> <td>0.8xvf</td> </tr> <tr> <td>normalized RMS linear fit error (max)</td> <td>0.037</td> </tr> </tbody> </table>	steady state voltage vf (max)	0.6	steady state voltage vf (min)	0.4	linear fit pulse peak (min)	0.8xvf	normalized RMS linear fit error (max)	0.037	TBD (eye mask or other)
steady state voltage vf (max)	0.6									
steady state voltage vf (min)	0.4									
linear fit pulse peak (min)	0.8xvf									
normalized RMS linear fit error (max)	0.037									
De-emphasis range	<table border="1"> <tbody> <tr> <td>normalized coefficient step size (min)</td> <td>0.0083</td> </tr> <tr> <td>normalized coefficient step size (max)</td> <td>0.05</td> </tr> <tr> <td>precursor full scale range (min)</td> <td>1.54</td> </tr> <tr> <td>post cursor full scale range (min)</td> <td>4</td> </tr> </tbody> </table>	normalized coefficient step size (min)	0.0083	normalized coefficient step size (max)	0.05	precursor full scale range (min)	1.54	post cursor full scale range (min)	4	TBD (no Tx training or back channel)
normalized coefficient step size (min)	0.0083									
normalized coefficient step size (max)	0.05									
precursor full scale range (min)	1.54									
post cursor full scale range (min)	4									

CAUI-4 chip to chip channel baseline

Table 93-9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance	C_d z_p C_p	TBD	nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	A_v A_f A_n	TBD — —	V V V
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient	$c(-1)$	TBD	— — —
Transmitter equalizer, post-cursor coefficient	$c(1)$	TBD	— — —
Continuous time filter, DC gain Minimum value Maximum value Step size	ϵ_{DC}	TBD	dB dB dB
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	0	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.07	UI
Receiver additive Gaussian noise, RMS	σ_r	1	mV
Target detector error ratio	DER_0	TBD	—

93.9.1 Channel operating margin

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 93-9 shall be greater than or equal to TBD. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

TBD

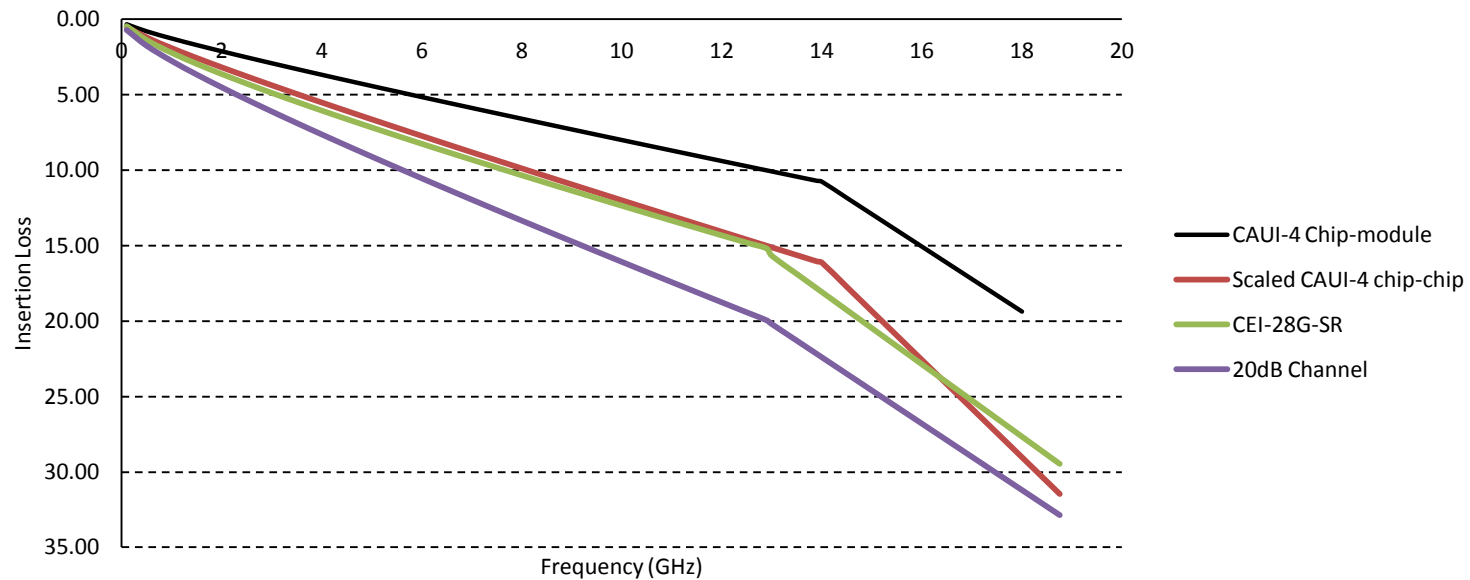
Modify to fixed setting or remove requirement

Modify to fixed setting

Increase the AC gain of CTLE?

1e-12 (or 1e-15) - TBD

CAUI-4 chip to chip informative channel characteristics



- $$\text{Insertion Loss} = 1.614 (0.075 + .537f^{(0.5)} + 0.566f) \quad 0.01 \leq f < 14$$

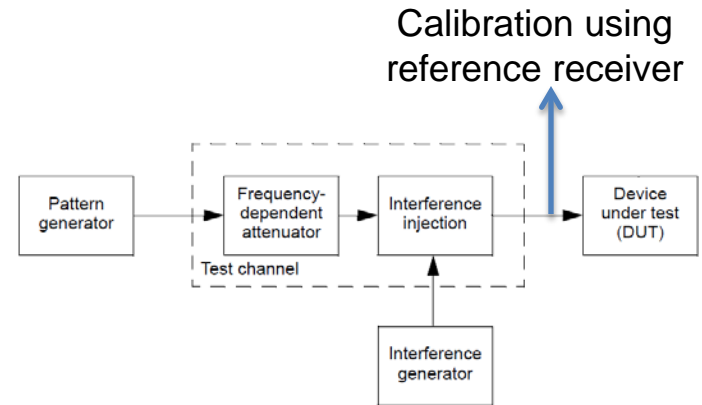
$$1.614 (-18 + 2f) \quad 14 \leq f < 18.75$$
- Or insertion loss increase depending on simulation results with Ali's & Mike's channel (http://www.ieee802.org/3/bm/public/jan13/li_01_0113_optx.pdf)
- Return loss = TBD

CAUI-4 chip to chip receiver baseline

	KR4 (D1.4, TP5a)	MR	CAUI-4 chip to chip Potential
Differential Input Return loss (min)	$RL(f) \geq$ $12.05-f$ for $0.05 \leq f \leq 6$ GHz $6.45 - 0.075f$ from $6 < f \leq 19$ GHz	$A_0 = -12$ $f_0 = 50$ MHz $f_1 = 4.4189$ $f_2 = 25.78125$ Slope = 12dB/dec	$RL(f) \geq$ $12.05-f$ for $0.05 \leq f \leq 6$ GHz $6.45 - 0.075f$ from $6 < f \leq 19$ GHz
Differential to common mode input returnloss	$RL(f) = 25 - 1.44f$ $0.05 \leq f \leq 6.95$ 15 $6/95 < f \leq 19$		$RL(f) = 25 - 1.44f$ $0.05 \leq f \leq 6.95$ 15 $6.95 < f \leq 19$
Interference Tolerance	Table 93-7	Tx Jitter + SJ + channel (Table 11-13)	See table on next slide
Input amplitude (max)		1200	TBD

Receiver Interference Tolerance baseline

Parameter	Test values
Maximum BER*	TBD
Applied peak-to-peak sinusoidal jitter	$5 \times 10^5/f$ ($100\text{kHz} < f \leq 10\text{MHz}$) $0.05UI$ ($10\text{MHz} < f < 10\text{LB}$)
Applied broad band noise	TBD
Applied peak-to-peak random jitter	TBD
Minimum eye height after reference CTLE	TBD
Minimum eye opening after reference CTLE	TBD
Channel Insertion Loss at 12.89GHz	TBD
COM of ISI channel	TBD



* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Compliance points

- See 93.8.2.1 Receiver test fixture from 802.3bj for TP5a
- See 93.8.1.1 Transmitter test fixture from 802.3bj for TP0a