Changes to Clause 45 and Annex 83D to implement proposal in comment #41 against P802.3bm D2.1 and discussed in ran_01_0314_optx.

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the identified reserved row in Table 45-3 (as modified by IEEE Std 802.3bj-201x) and insert ~~a~~ four new ~~row for register 1.169~~ rows immediately below the changed row as follows:

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.167 through 1.~~169~~168	Reserved	
1.169	CAUI-4 chip-to-module recommended CTLE	45.2.1.92a

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.176 through 1.~~199~~178	Reserved	
1.179	CAUI-4 chip-to-module recommended CTLE	45.2.1.92a
1.180 through 1.183	CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 through lane 3	45.2.1.92b 45.2.1.92c
1.184 through 1.187	CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 3	45.2.1.92d 45.2.1.92e
1.188 through 1.199	Reserved	

Change the text of 45.2.1.3 to add a note as follows:

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number.

A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier to indicate that a unique identifier as described above is not provided.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

Table 45–15—40G/100G PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.13.12	100GBASE-KP4 ability	1 = PMA/PMD is able to perform 100GBASE-KP4 0 = PMA/PMD is not able to perform 100GBASE-KP4	RO
1.13.11	100GBASE-ER4 ability	1 = PMA/PMD is able to perform 100GBASE-ER4 0 = PMA/PMD is not able to perform 100GBASE-ER4	RO
1.13.10	100GBASE-LR4 ability	1 = PMA/PMD is able to perform 100GBASE-LR4 0 = PMA/PMD is not able to perform 100GBASE-LR4	RO
1.13.9	100GBASE-SR10 ability	1 = PMA/PMD is able to perform 100GBASE-SR10 0 = PMA/PMD is not able to perform 100GBASE-SR10	RO
1.13.8	100GBASE-CR10 ability	1 = PMA/PMD is able to perform 100GBASE-CR10 0 = PMA/PMD is not able to perform 100GBASE-CR10	RO
1.13.7	100GBASE-SR4 ability	1 = PMA/PMD is able to perform 100GBASE-SR4 0 = PMA/PMD is not able to perform 100GBASE-SR4	RO
1.13.6~~7.5~~	Reserved	Ignore on read	RO
1.13.5	40GBASE-ER4 ability	1 = PMA/PMD is able to perform 40GBASE-ER4 0 = PMA/PMD is not able to perform 40GBASE-ER4	RO
1.13.4	40GBASE-FR ability	1 = PMA/PMD is able to perform 40GBASE-FR 0 = PMA/PMD is not able to perform 40GBASE-FR	RO
1.13.3	40GBASE-LR4 ability	1 = PMA/PMD is able to perform 40GBASE-LR4 0 = PMA/PMD is not able to perform 40GBASE-LR4	RO
1.13.2	40GBASE-SR4 ability	1 = PMA/PMD is able to perform 40GBASE-SR4 0 = PMA/PMD is not able to perform 40GBASE-SR4	RO
1.13.1	40GBASE-CR4 ability	1 = PMA/PMD is able to perform 40GBASE-CR4 0 = PMA/PMD is not able to perform 40GBASE-CR4	RO
1.13.0	40GBASE-KR4 ability	1 = PMA/PMD is able to perform 40GBASE-KR4 0 = PMA/PMD is not able to perform 40GBASE-KR4	RO

[a]RO = Read only

Insert 45.2.1.12.5a and 45.2.1.12.5b after 45.2.1.12.5 as follows:

45.2.1.12.5a 100GBASE-SR4 ability (1.13.7)

When read as a one, bit 1.13.7 indicates that the PMA/PMD is able to operate as a 100GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.13.7 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR4 PMA/PMD type.

45.2.1.12.5b 40GBASE-ER4 ability (1.13.5)

When read as a one, bit 1.13.5 indicates that the PMA/PMD is able to operate as a 40GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.13.5 indicates that the PMA/PMD is not able to operate as a 40GBASE-ER4 PMA/PMD type.

Insert 45.2.1.~~88c~~ 92a through 45.2.1.92e after 45.2.1.92~~88b (as inserted by IEEE Std 802.3bj-201x)~~ as follows:

45.2.1.92a CAUI-4 chip-to-module recommended CTLE register (Register 1.~~169~~179)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–71a~~. The value stored in this register corresponds to the CTLE peaking value (see 83E.3.1.6.1) recommended by the host (and used in the evaluation of host output compliance). The module may optionally use this information to adjust its CTLE setting~~.

Table 45–71a—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.~~169~~179.15:~~6~~5	Reserved	Value always 0, writes ignored	RO
1.~~169~~179.~~5~~4:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	~~RO~~ R/W
1.~~169~~179.0	Reserved	Value always 0, writes ignored	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.92a.1 Recommended CTLE peaking (1.179.4:1)

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 chip-to-module interface defined in Annex 83E (see 83E.3.1.6). The module may optionally use this information to adjust its CTLE setting.

45.2.1.92b CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.180)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–71b.

45.2.1.92b.1 Post-cursor setting (1.180.4:2)

The value of these bits sets the post-cursor coefficient c(1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1).

45.2.1.92b.2 Pre-cursor setting (1.180.1:0)

The value of these bits sets the pre-cursor coefficient c(–1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1).

Table 45–71b—CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.180.15:5	Reserved	Value always 0, writes ignored	RO
1.180.4:2	Post-cursor setting	4 3 2 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = –0.25 1 0 0 = –0.2 0 1 1 = –0.15 0 1 0 = –0.1 0 0 1 = –0.05 0 0 0 = 0	R/W
1.180.1:0	Pre-cursor setting	1 0 1 1 = –0.15 1 0 = –0.1 0 1 = –0.05 0 0 = 0	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.92c CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers (Registers 1.181, 1.182, 1.183)

The CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers are defined similarly to register 1.180 (which is used for lane 0, see 45.2.1.92b) but for lanes 1 through 3 respectively.

45.2.1.92d CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.184)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–71c.

45.2.1.92d.1 Post-cursor setting (1.184.4:2)

The value of these bits sets the post-cursor coefficient c(1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1).

45.2.1.92d.2 Pre-cursor setting (1.184.1:0)

The value of these bits sets the pre-cursor coefficient c(–1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1).

45.2.1.92e CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers (Registers 1.185, 1.186, 1.187)

The CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers are defined similarly to register 1.184 (which is used for lane 0, see 45.2.1.92d) but for lanes 1 through 3 respectively.

Table 45–71c—CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.184.15:5	Reserved	Value always 0, writes ignored	RO
1.184.4:2	Post-cursor setting	4 3 2 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = –0.25 1 0 0 = –0.2 0 1 1 = –0.15 0 1 0 = –0.1 0 0 1 = –0.05 0 0 0 = 0	R/W
1.184.1:0	Pre-cursor setting	1 0 1 1 = –0.15 1 0 = –0.1 0 1 = –0.05 0 0 = 0	R/W

[a]R/W = Read/Write, RO = Read only

Changes to 83D.3.1.1

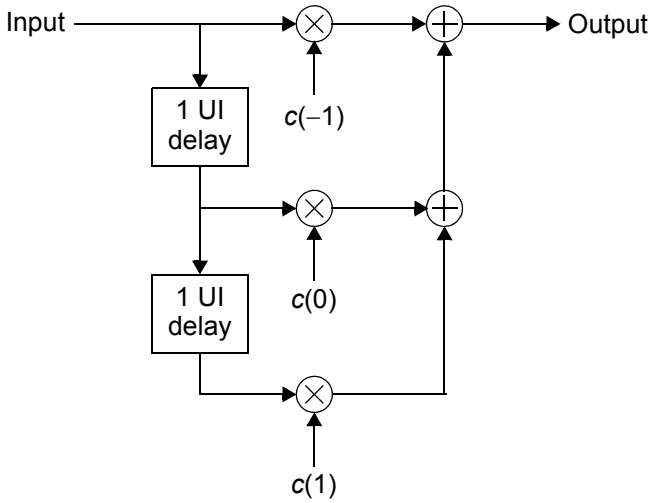

Figure 83D–4—Transmit equalizer functional model

If a Clause 45 MDIO is implemented, the c(–1) and c(1) coefficients are accessible through registers 1.180 through 1.187 (see 45.2.1.92b through 45.2.1.92e).

Table 83D–2—Pre-cursor equalization

Pre-cursor equalization setting	Value
R_{pre} at tap setting 0	1 ±12.5%
R_{pre} at tap setting 1	1.11 ±12.5%
R_{pre} at tap setting 2	1.25 ±12.5%
R_{pre} at tap setting 3	1.43 ±12.5%

Table 83D–3—Post-cursor equalization

Post-cursor equalization setting	Value
R_{pst} at tap setting 0	1 ±12.5%
R_{pst} at tap setting 1	1.11 ±12.5%
R_{pst} at tap setting 2	1.25 ±12.5%
R_{pst} at tap setting 3	1.43 ±12.5%
R_{pst} at tap setting 4	1.67 ±12.5%
R_{pst} at tap setting 5	2 ±12.5%