Complementary Transmitter and Receiver Jitter Test Methodology

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Overview

- Overview of FC-MJS jitter methodology
- Allocating jitter burden from the transmitter to the receiver through Golden PLL jitter tracking
- Decoupling of receiver stress sensitivity and receiver jitter tolerance

Fundamental Issue

802.3aq (LRM) receiver jitter tolerance introduced an inconsistent set of specifications by separating stress receiver testing and transmitter jitter tracking

- Transmitter jitter relief through MJS Golden PLL was maintained
  - Compliant transmitters may have low frequency jitter present, but not observed due to by the Golden PLL tracking effect
- Receivers currently tested at two spot frequencies without additional stress
- Full stress with the addition of SJ can result in broken links that is not observed with stress and SJ imposed in independent tests
- Testing the receiver at only two discrete frequencies may not guarantee the receiver can actually tolerate transmitters with jitter tracked out by the Golden PLL
- A retimed 100Gbase-SR4 link with a source CMU and 3 cascaded CDRs may result in significant interoperability risk using the existing two point specification

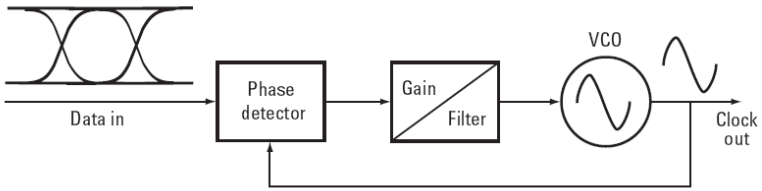
Receiver test should complement transmitter test

Reliable link operation requires that the receiver test complements transmitter test. The receiver test should be extended to include SJ as allowed in the current transmitter spec. Alternatively, the transmitter test could be more stringent, but it is not practical to force the transmitter to produce low or no jitter over regions where the receiver is not tested

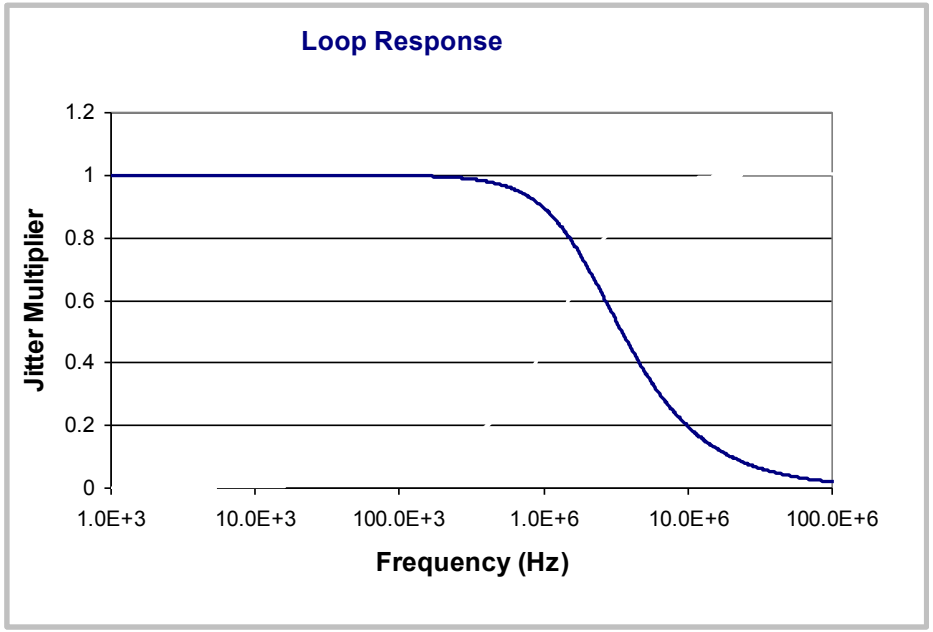
PLL concepts: PLL jitter transfer indicates how *recovered clock* (jitter out) tracks the data (jitter in)

The response of the PLL is generally a low-pass function, sometimes referred to as the jitter transfer response or JTF

$$\text{Closed loop gain} = \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1 + A(s)} = G(s) = |G(s)|e^{j\phi(s)}$$

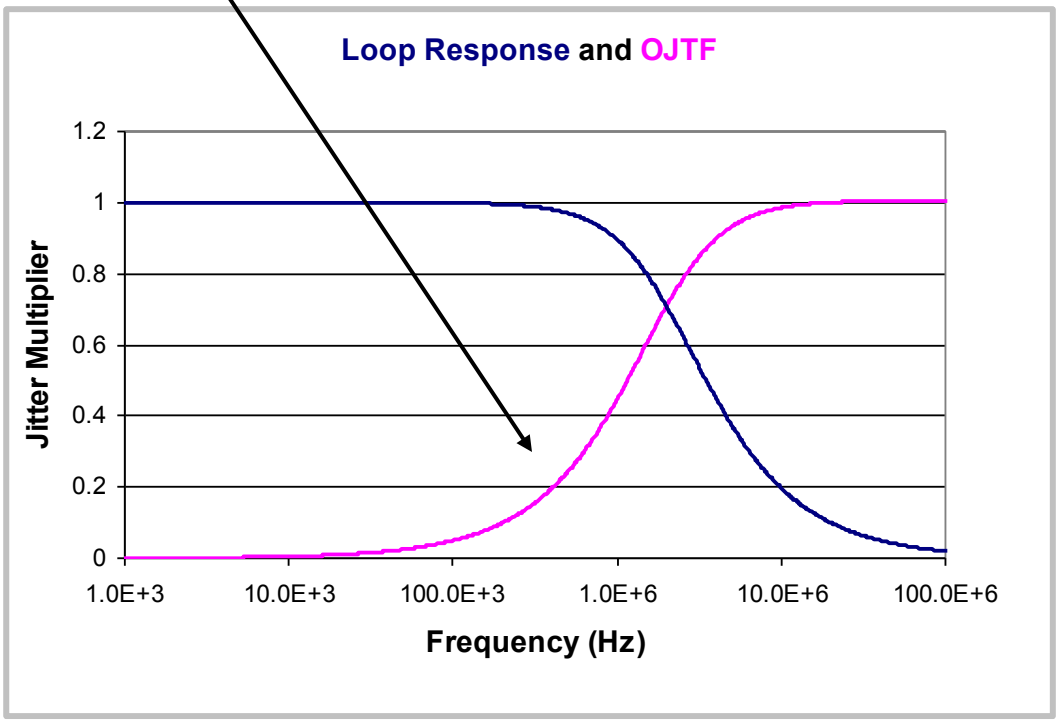


Low frequency jitter is transferred to the clock, high frequency jitter is not



The observed jitter transfer function (OJTF, the jitter that is observed by a receiver, or on the instrument clocked/ triggered by the recovered clock)

$$\mathrm{OJTF} = 1 - G(s) = 1 - \left|G(s)\right| e^{j\phi(s)}$$



The observed jitter is a complement to the PLL jitter transfer response

OJTF=1-JTF (Phase matters!)

As the jitter on the recovered clock trigger rolls off, common mode effect is reduced

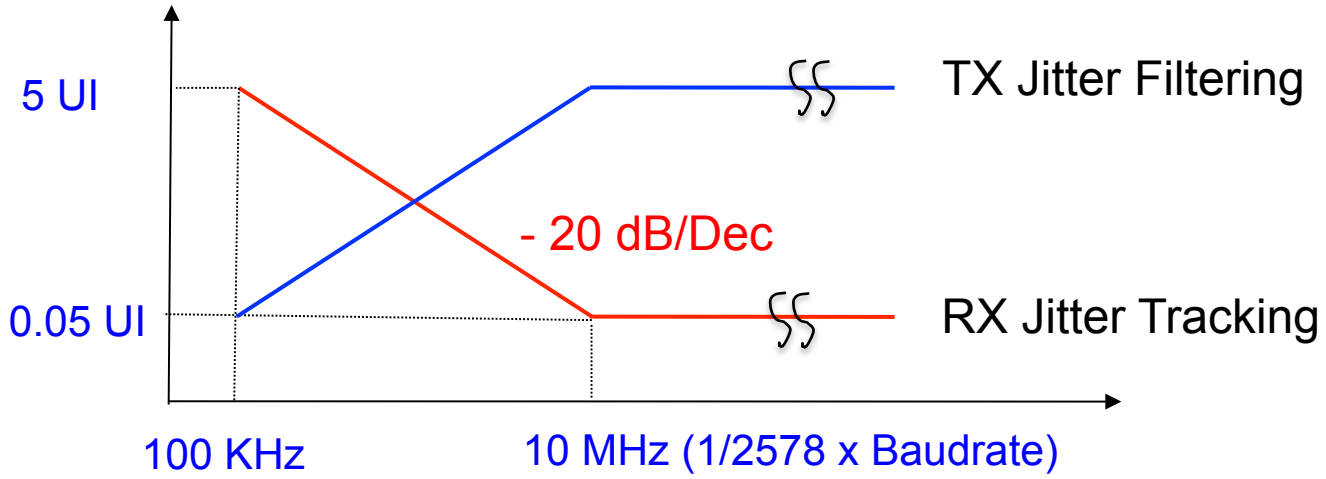
As jitter frequency gets large, eventually there is no jitter on the recovered clock and all the higher frequency jitter on the data stream is observed

Comprehensive Jitter Methodology

A comprehensive methodology to test transmitters and receivers for jitter was developed during 1 GFC standardization in the FC-MJS project and has become the basis for data communications system specification

This methodology was based on systems using low cost oscillators and a reduction in power supply filtering to enable low-cost high-volume applications

- Transmitter test assumes low frequency jitter should be tracked by a receiver, thus transmitter specs are relaxed by observing the transmitter using a reference PLL with OJTF defined as a high pass single pole filter with -20 dB/dec rolloff and -3dB corner frequency at 1/1667 Baudrate (changed to 1/2578*baudrate since 10 GbE)
- Receiver test should complement transmitter test by verifying low frequency jitter is tolerated.

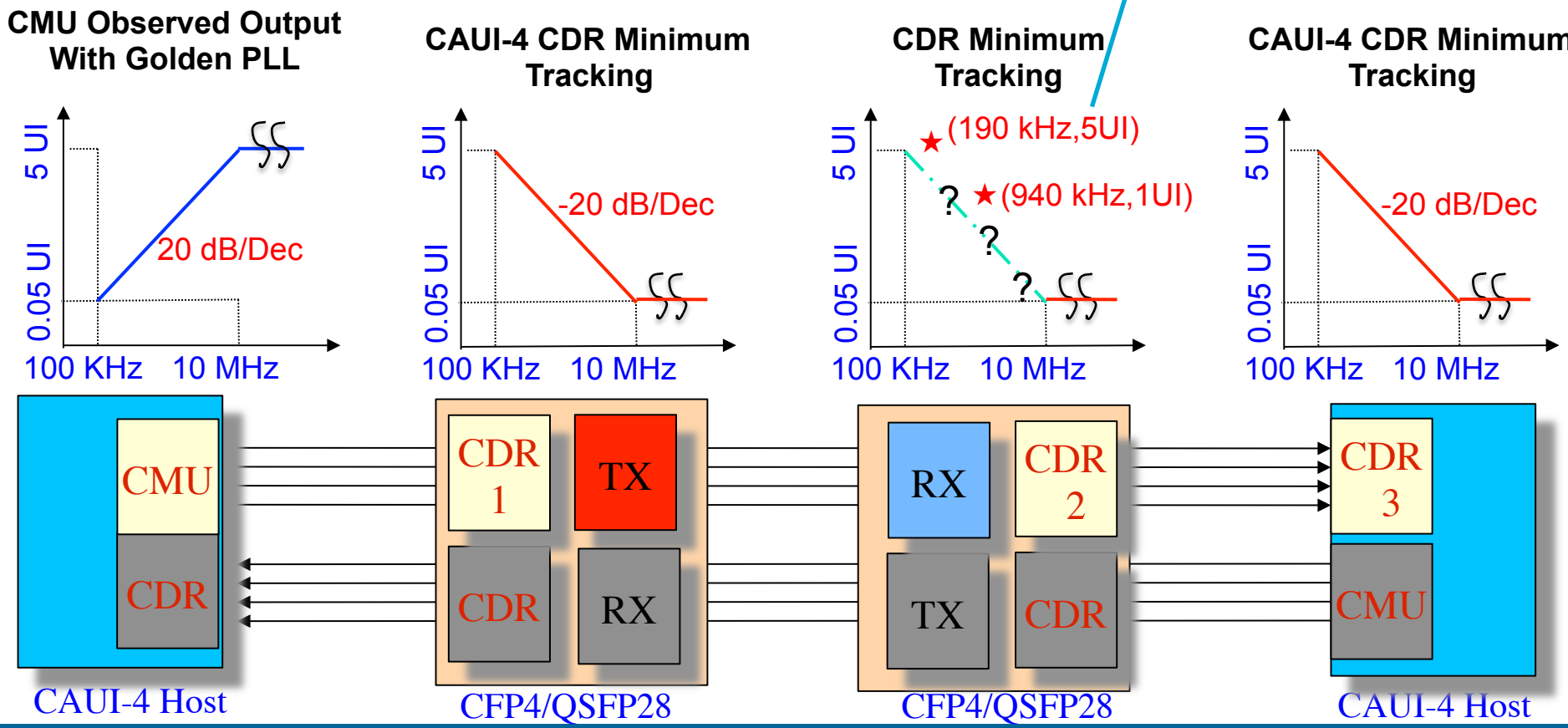


Current 100GBase-SR4 Application Model

Clause 95 introduces an inconsistency between transmitter jitter tracking and receiver jitter tolerance

- CDR2 may break due to spurious SJ coming from upstream CMU/CDR
- CDR3 may break as result of over stress from module during jitter tolerance test

Not Consistent with CDR 1 output or CDR3 input



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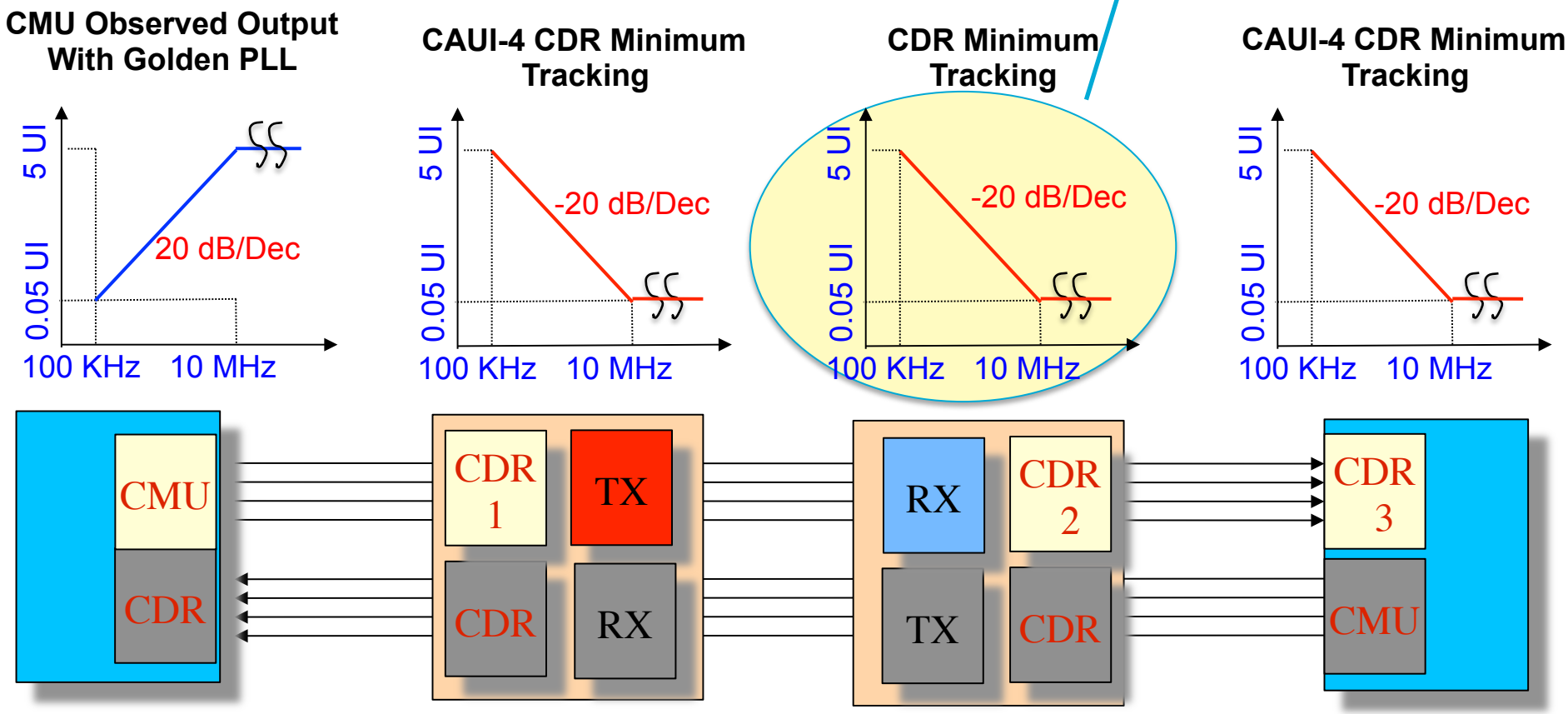
For 100Gbase-SR4 Link to be Self Consistent

- CDR2 as defined in 95.7.2 must track the full range of upstream SJ
- CDR2 can't be tested at two overstress points since it may break CDR3

Make CDR3 Self Consistent with CDR1 and CDR3



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Clause 95 Transmitter and Receiver Jitter Definition

Clause 95.8.5 Transmitter and dispersion penalty (TDP) defines test methodology including relaxed jitter performance of the transmitter through Golden PLL timing

- "The clock recovery unit (CRU) used in the TDP measurement has a high-pass OJTF with corner frequency of 10 MHz and a slope of 20 dB/decade"

Clause 95.8.9 defines stress receiver sensitivity at max VECP, J2, J4, and MAX OMA

- SJ defined to be in range of 0-0.05 UI, which can be 0 UI but real link may have 0.05 UI!

Clause 95.8.9 defines jitter tolerance at max OMA

- Jitter tolerance test is not defined at max VECP, J2, and J4
- Defining only SJ at only two points (190,5)/(940,1) kHz/UI does not guarantee the CDR can operate over the range transmitter jitter tracked by the Golden PLL

Jitter tolerance test needs to be added to stress receiver sensitivity test in table 95-7 over the full range of Golden PLL band 100 kHz-10x PLL corner frequency (100 MHz) instead of creating two separate tests to avoid potential interoperability issue!

Clause 87/88 Stress Receiver Sensitivity Test Clause 87.8.11.1

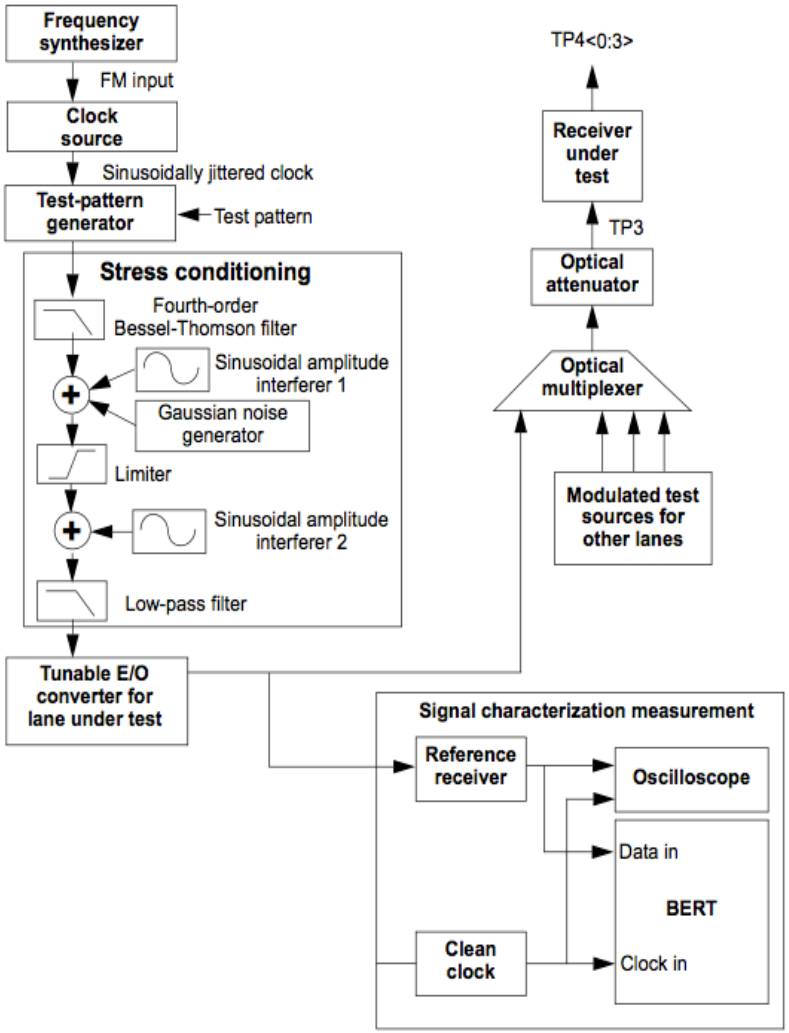

Figure 87–3—Stressed receiver conformance test block diagram

Follow the Test Method of 100GBase-LR4

Table 95-7 need to reference Stress Receiver Sensitivity CL 88.8.10 or pull the text into CL 95

CL 95.8.8 Stress receiver sensitivity should reference 87.8.11.1 test method with exception in CL 88.8.10

88.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 88–8 if measured using the method defined in 87.8.11 with the following exceptions:

a) Added sinusoidal jitter is as specified in Table 88–13.
b) The stressed eye J2 Jitter, stressed eye J9 Jitter, and vertical eye closure penalty are as given in Table 88–8.
c) The test pattern is as given in Table 88–11.
d) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 88.8.8.

Table 88–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	$5 \times 10^5 / f$
10 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

Update Table 95-7 as Shown

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–11	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.6	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty (VECP),[d] each lane	3.6	dB
Stressed eye J2 jitter,[d] each lane	0.41	UI
Stressed eye J4 jitter,[d] each lane	0.55	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	
Receiver jitter tolerance in OMA, each lane (max)[e]	–5.6	dBm
Conditions of receiver jitter tolerance test:		
Jitter frequency and peak-to-peak amplitude	(190, 5)	kHz, UI
Jitter frequency and peak-to-peak amplitude	(940, 1)	kHz, UI
OMA of each aggressor lane	3	dBm

and jitter tolerance *

* With applied Sinusoidal jitter (SJ) as given in 88.8.10.