Feasibility of Unretime cPPI-4 and How to Proceed

IEEE 802.3bm Task Force

Ali Ghiasi

Broadcom Corporation

May 14, 2013

Victoria

Overview

- Material presented here previously have been presented at one or more of the following venue
  - 100GNGOPTX task force
  - http://www.ieee802.org/3/bm/public/nov12/ghiasi_02_1112_optx.pd
  - 'Feasibility of Unretimed 100 GbE Based on 4x25. 78 GBd',OWJ1.2, OFC 2012
  - IEEE Photonic Interconnect, 'Enabling 850 nm VCSEL for 100 GbE Applications, Santa Fe, 2012
- There has been renewed interest in the low cost, low power, unretime cPPI-4 interface for 20-30 m SR4
- The key questions are
  - Does the 20 m unretime PMD has broad market potential as it will fragment the market
  - Alternatively within 12-18 months with process and device improvement if there is market need for unretime then the PMD electrical interface for 100GBase-SR4 can be defined in an MSA or OIF.

802.3bm Objective

- 802.3bm objective defines PMD for operation up to 100 m which is retimed and uses FEC
- The 20 m objective was to included to define lower power, cost, and size driven by data center applications
  - How do we address 20 m reach objective

- Define re-timed 4-lane 100G PMA to PMA electrical interfaces for chip to chip and chip to module applications
- Define a 40 Gb/s PHY for operation over at least 40 km of SMF
- Define a 100 Gb/s PHY for operation up to at least 500 m of SMF
- Define a 100 Gb/s PHY for operation up to at least 100 m of MMF
- Define a 100 Gb/s PHY for operation up to at least 20 m of MMF

Risk of Sprinkling One Two Many CDR

- During MMF ad-hoc meeting 55 mW for 25.78 GBd CDR was reported, not sure what functionality is include and if the report power is the worst case
  http://www.ieee802.org/3/bm/public/mmfadhoc/meetings/apr11_13/king_01a_0413_mmf.pdf
  - At 25.78 GBd testability features are essential due to lack of option to probe
  - Eye scan typically require another slicer and may add ~30% to the power
  - Loopback adds more power
  - Pattern generation and checking adds more power
- During development of XFP MSA carful analysis and attention was given to cascading CDRs
  - We started trivializing and ignoring jitter peaking as result of cascaded CDRs with 802.3ba project
  - The reference-less CDR which is the only option for QSFP28 does carry the risk of false lock
- Next lets compare the above reported 25.78 GBd CDR PD of 55 mW with latest 25G VCSEL link PD.

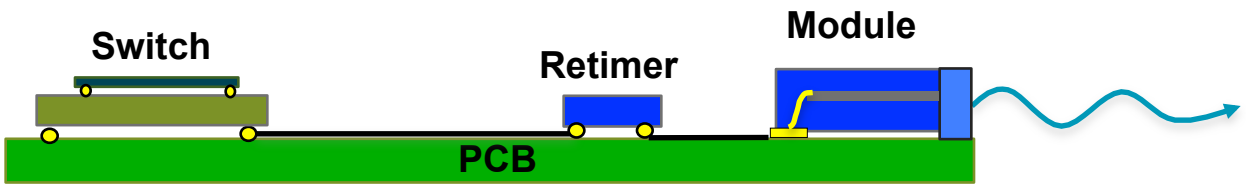
Is the CDR Power Negligible in Comparison to the 850 nm VCSEL Link

- Even at 55 mW/CDR a retime interface adds 4.2 pj/bit to the 1.4 pj/bit for the optics (300% Increase!)
  - Jonathan E. Proesel, et al. “Ultra Low Power 10- to 25-Gb/s CMOS-Driven VCSEL Links”, OFC 2012 OW4I.3, reports 1.37 pj/bit@15 GBd and 3.6 pj/bit@25 GBd
  - Jonathan E. Proesel, et al. “35-Gb/s VCSEL-Based Optical Link using 32-nm SOI CMOS Circuits”, OFC 2013 OM2H.2, reports 1.0 pj/bit@25 GBd and 2.7 pj/bit@35 GBd
    - Paper reports 1 pj/bit for 25 GBd link with 0 dB excess loss, instead used 35 GBd results with 3 dB excess passive loss but scaled for operation at 25.78 GBd

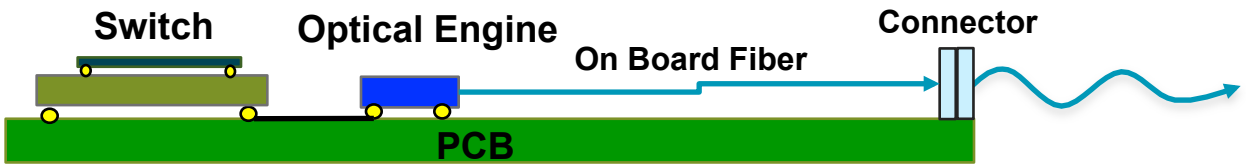
		Worst Corner @ 35 GBd	Worst Corner Scaled @ 25.78 GBd
TX	Post AMP	11 mW	4.2 mW
	LDD	7.7 mW	2.9 mW
	VCSEL	28 mW	10.7 mW
RX	TIA	13 mW	5.0 mW
	LA & LPF	29 mW	11.1 mW
	Out Driver	6 mW	2.3 mW
Total Power		95 mW (2.7 pj/bit)	36.2 mW (1.4 pj/bit)

Applications Reference Diagram

- Adding retimers increases the 100Gbase-SR4 power dissipation by ~3x
- To support 100GBase-CR4 a retimer already exist in close proximity of the module and it could drive unretime link



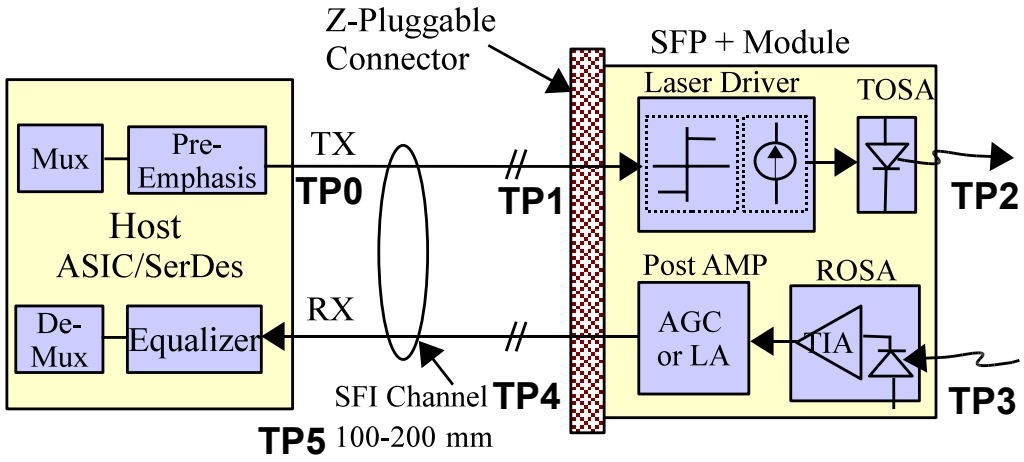
Option 1
(Module)

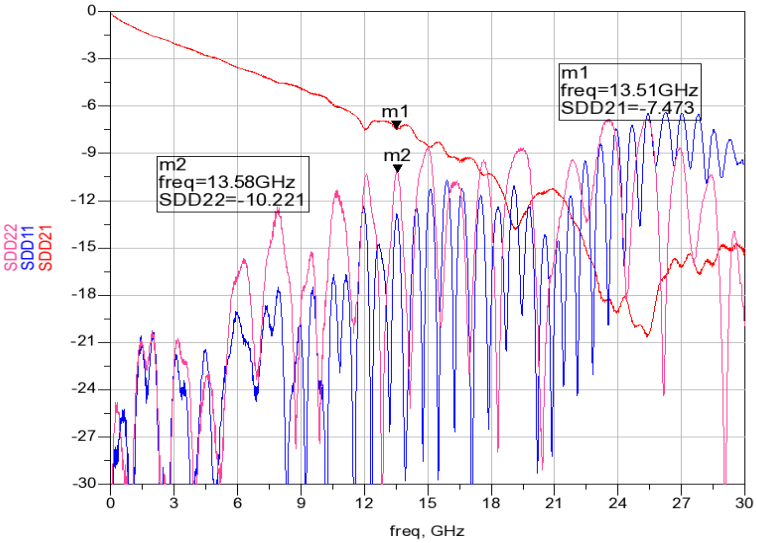


Option 2
(On Board)

Suitable Channel for Unretime Application

- Channel has 7.4 dB loss at Nyquist





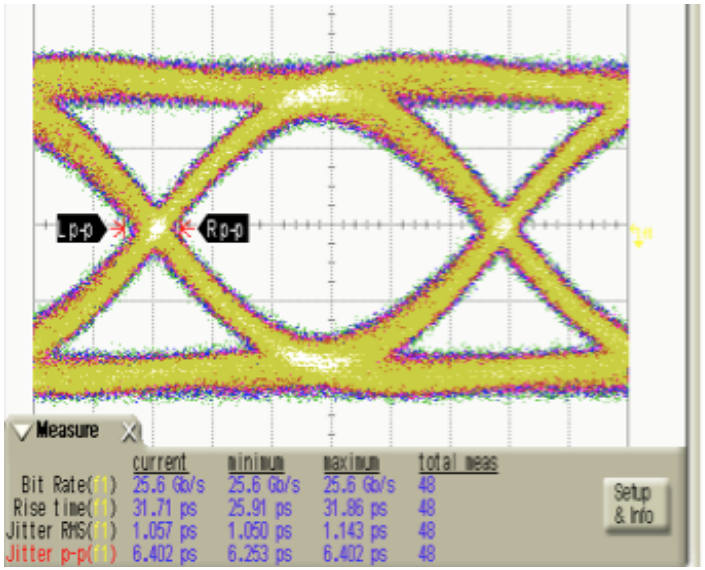
Host PCB
Material =N4000-13SI
Trace Length =4”
Traces = 5 mils stripline

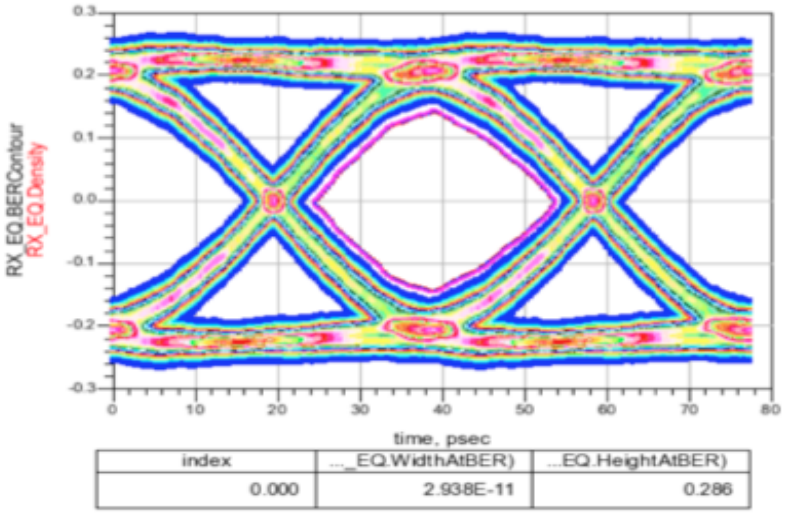
Connector Quattro II

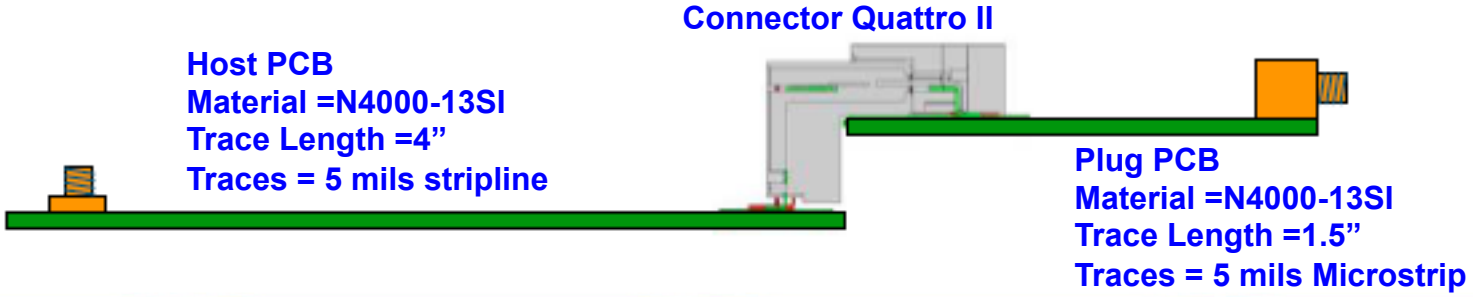
Plug PCB
Material =N4000-13SI
Trace Length =1.5”
Traces = 5 mils Microstrip

Far End Eye

- Measured and simulated eyes are good enough to drive the optics with <0.28 UI of TJ at TP1a similar to SFP+!
  - The optics need to improve to work with 0.28 UI TJ from current 0.22 UI TJ at LD driver input







Summary

- As long as the adding CDR does not add more than 10% to the module cost or power then one could argue why take the extra step and go unretime
  - King_01a_0413.mmf.pdf states CDR cost is negligible and the latest generation of the 25.78G CDR has PD of 55 mW or 4.2 pj/bit, adding total of 440 mW to the module
  - In comparisons reported 35 GBd VCSEL link TX+RX scaled for operation to 25.78GBd has PD of only 36.2 mW or 1.4 pj/bit
  - Adding two CDR to the VCSEL link increases the link power dissipation by 300%
- I have shown feasibility of unretime 100 m SR4 link
  - Natural progression of 100 m SR4 link next will be unretime
  - Process and device improvement will make unretime link even more feasible in 12-18 month
  - PMD electrical interface can be defined in an MSA or in OIF
  - At the time when we defiend 10Gbase-SR it would have been impossible to define the PMD electrical interface which is now called SFP+
- Defining a 20 m unretime SR4 link is too small a step and will likely fragment the market with time we can get to 100 m unretime.

Thank You