A CAUI-4 Chip-to-Chip Link Study: Presentation 3

Mike Peng Li
Altera Corporation

For IEEE 802.3bm
Rev 1.1

May 13-17, 2013

Supporters

Elizabeth Kochuparambil, Cisco

Jeremy Buan, Hirose

Rick Rabinovich, ALU

Ryan Latchman, Mindspeed

Scott Kipp, Brocade

Shashi Patel, Brocade

Purposes

- Explore the solution space and technical feasibility for the CAUI-4 chip-to-chip link under the assumptions of
  - Tx FIR+Rx CTLE equalizations
  - No FEC
  - Measured channels with IL, ILD, and xtalk

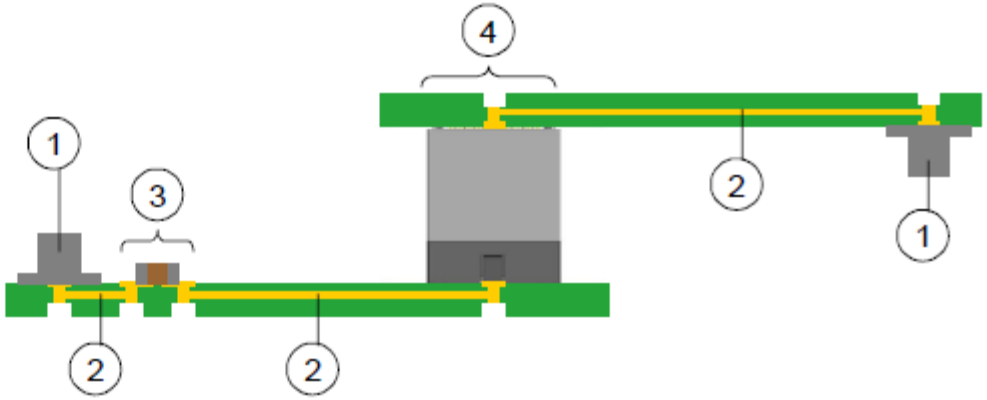
Background and Motivation

- Study 1 based on a 20 dB ([1]) synthesized channel with IL and xtalk was presented in Jan meeting.
- Study 2 based on a 13 dB and a 15 dB ([2]) measured channels with IL, ILD, and xtalk were presented in March meeting.
- Excessive margin have been found in both studies 1 and 2, suggesting the feasibility of a 20 dB IL channel for CAUI-4 c2c
- This study (study 3) focuses on a 20 dB measured channel, with ILD, and xtalk.

I. Channel Consideration

Channel Topology

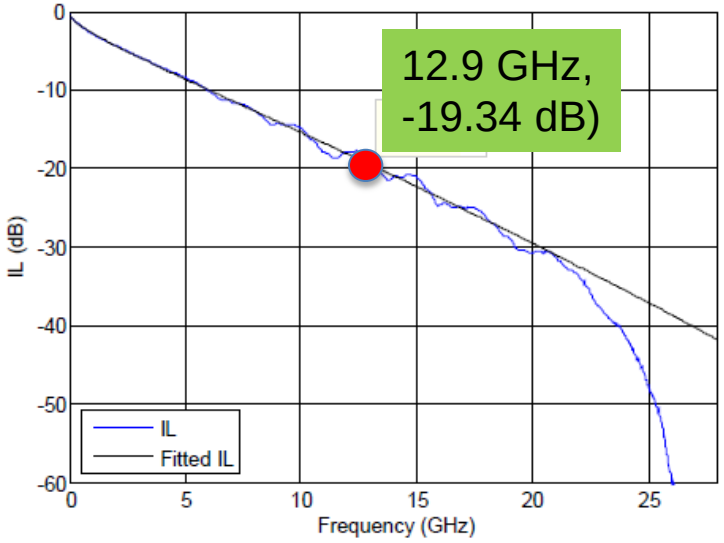
1. SMA connector
2. Stripline trace
3. DC blocking capacitor
4. IT5 connector

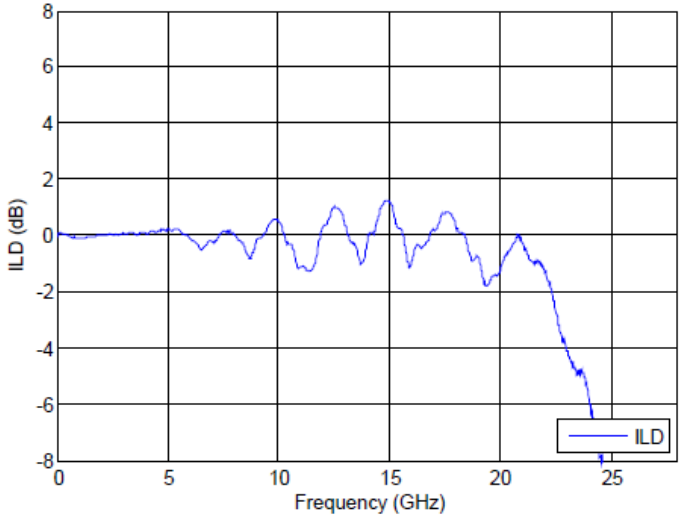


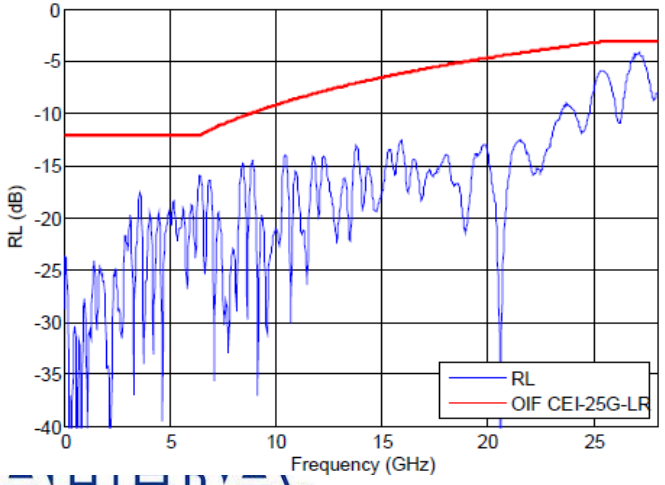
- provided by Hirose

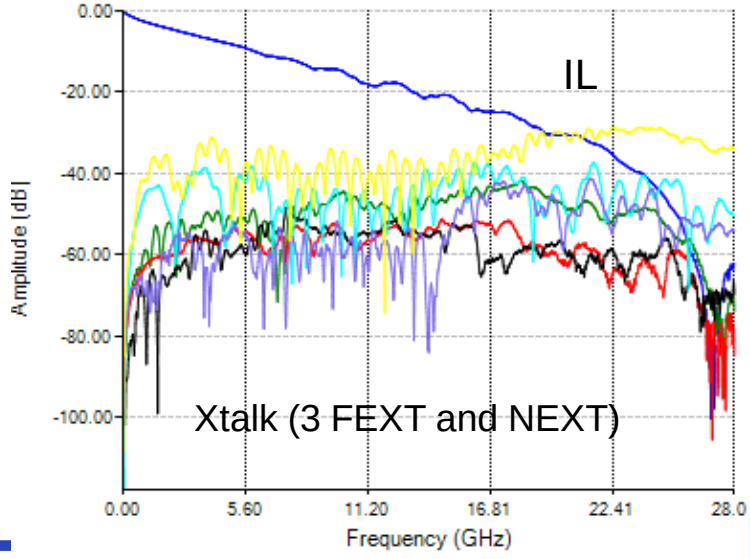
Channel Characteristics

- IL, ILD, RL, xtalk (provided by Hirose)







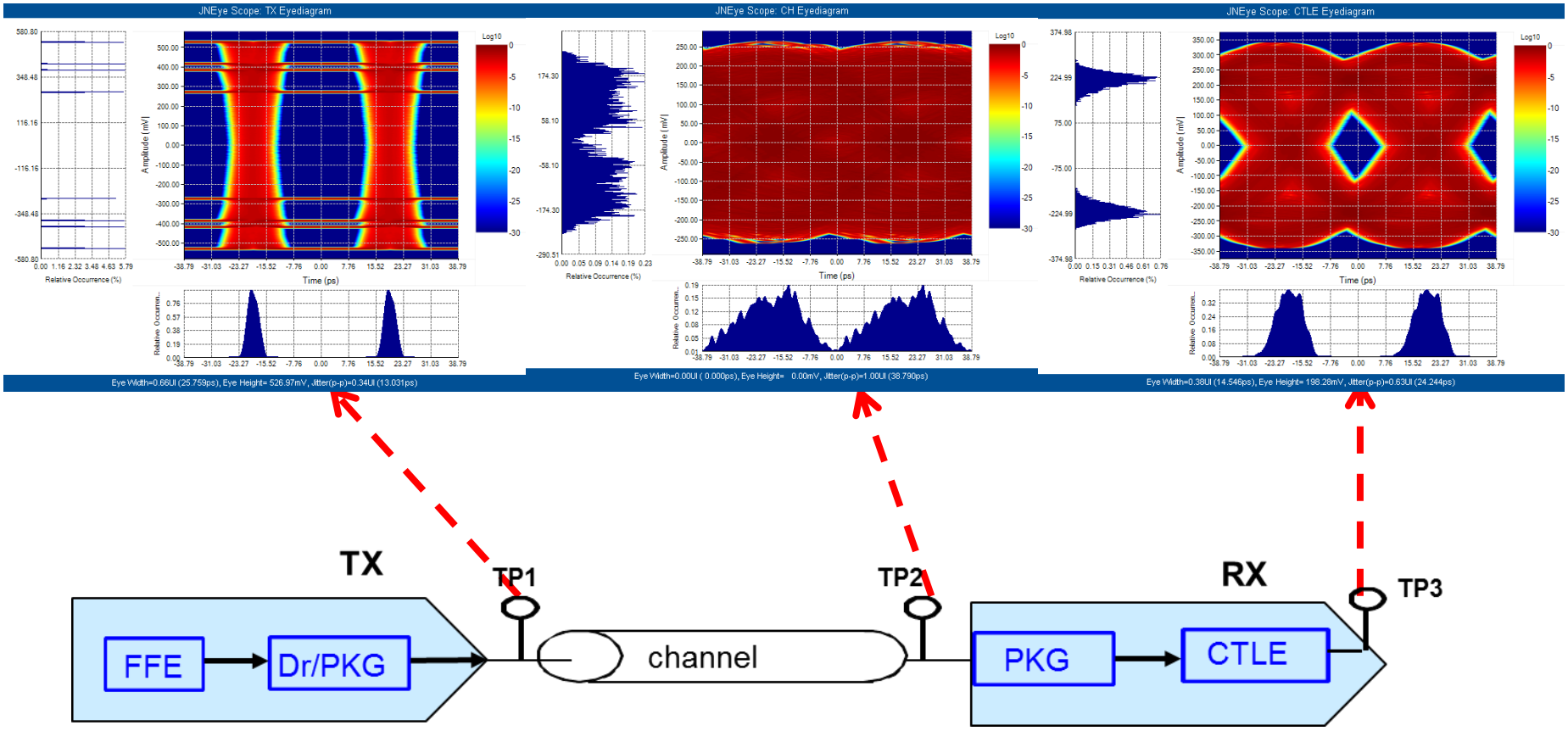


II. Simulation, Solution Space, and Feasibility

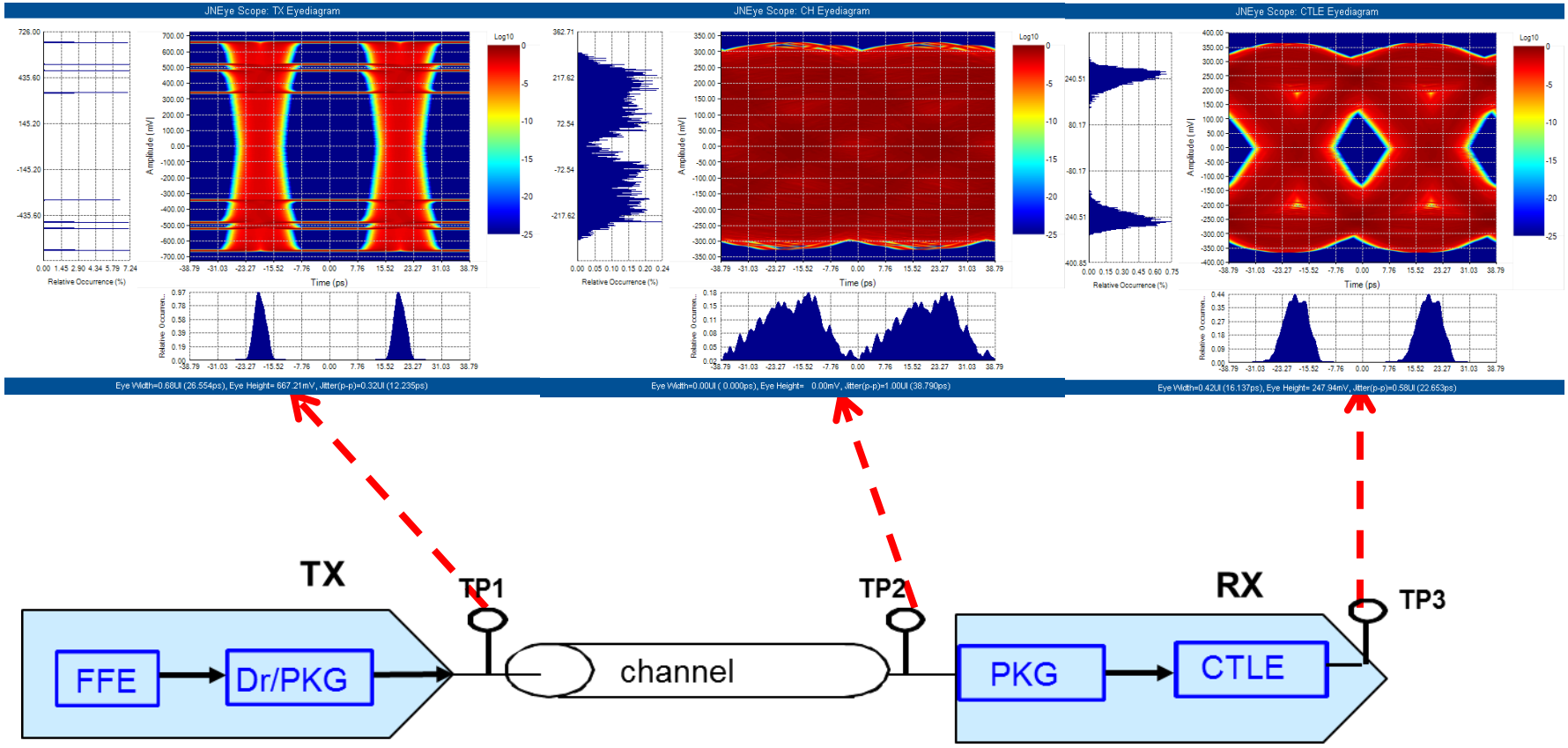
Simulation Setup

- Data rate
  - 25.78 Gbps
- Data Pattern
  - PRBS2^15-1
- Tx
  - A 3-tap FIR (c-1, c0, c+1)
  - Vod = 800 mV, 1000 mV
  - Jitter
    - BUJ: 0.15 UI, DCD: 0.035 UI, RJ: 0.15 UI
  - Noise
    - RN: 1 mv rms
- Rx
  - CTLE
    - Active, 15 dB AC gain at Nyquist
- Both Tx and Rx models have been correlated with actual device measurements
- Channel
  - S-parameters provided by Hirose

Simulation Results (I): Vod = 800 mV



Simulation Results (II): Vod = 1000 mV



Simulation Results at CTLE Output

Vod (mV)	CH IL (dB)	BER	EW (UI)	EH (mv)
800	-19.3	1e-12	0.40	206
800	-19.3	1e-15	0.38	198
1000	-19.3	1e-12	0.42	248
1000	-19.3	1e-15	0.39	237

25-32 G Serdes Power (I)

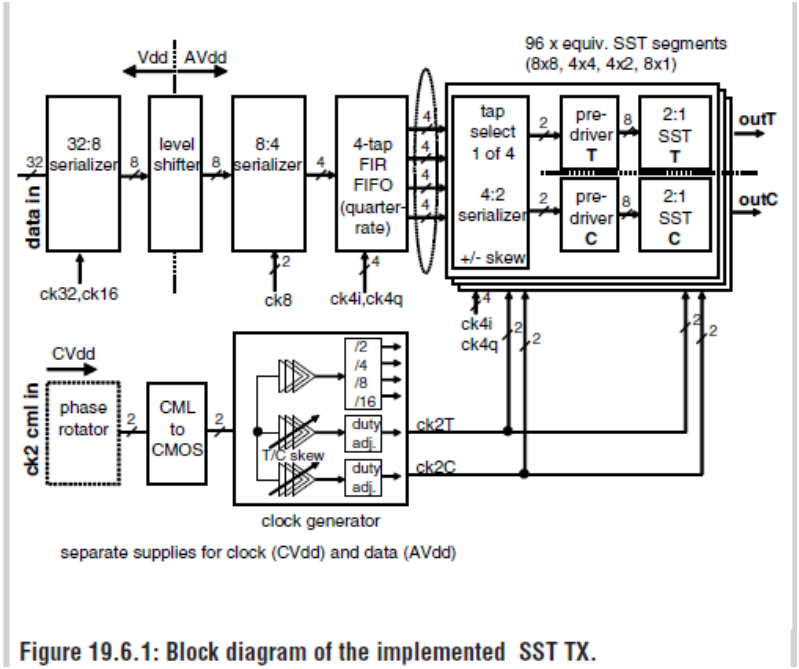
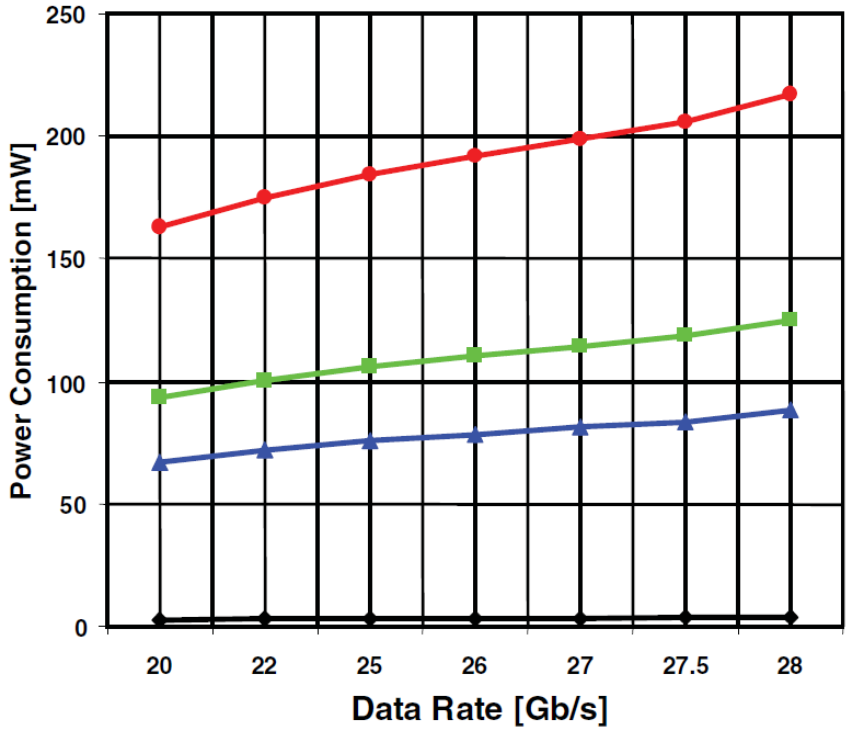


Figure 19.6.1: Block diagram of the implemented SST TX.



- Total TX power ~180 mW at 25 Gbps
- TX includes SER, 4-tap FIR, driver, CG
- From C. Menolfi et al., "A 28Gb/s Source-Series Terminated TX in 32nm CMOS SOI," ISSCC Dig. Tech. Papers, pp. 334-335, Feb. 2012.

25-32 G Serdes Power (II)

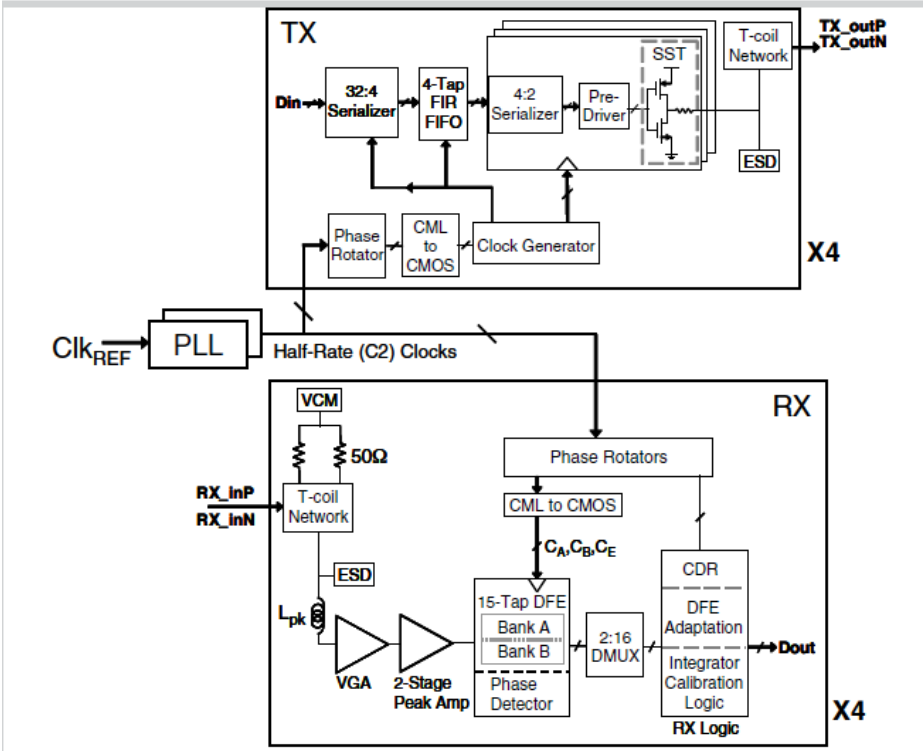


Figure 19.1.1: Top-level transceiver architecture.

- Serdes is designed for 28 Gbps BP
- TX has 4-tap FIR, driver, CG, RX has VGA, CTLE/peaking amp, 15 tap DFE
- Total power reported is 693 mW at 28 Gbps (inferred RX power would be ~513 mW)
- From J. Bulzacchelli et al., "A 28Gb/s 4-Tap FFE/15-Tap DFE Serial Link Transceiver in 32nm SOI CMOS Technology", ISSCC Dig. Tech. Papers, pp. 324-326, Feb. 2012.

III. Summary and Closing Remarks

Summary

- A link solution space and feasibility study is carried out for CAUI-4 chip-to-chip at 25.78 Gbps, and for a measured channel with the following characteristics
  - IL is 19.34 at Nyquist (12.9 GHz)
  - ILD is <= (+-) 1.3 dB for frequency < Nyquist
  - Overall xtalk (power sum, 3 FEXT and 3 NEXT) is ~ - 33 dB
- We have found that Tx FIR + Rx CTLE is sufficient to compensate this channel, and to achieve the link BER objective of 1e-12 and 1e-15, with margins (see table below)

Vod (mV)	CH IL (dB)	BER	EW (UI)	EH (mv)
800	-19.3	1e-12	0.40	206
800	-19.3	1e-15	0.38	198
1000	-19.3	1e-12	0.42	248
1000	-19.3	1e-15	0.39	237

- In view of the three studies conducted ([1], [2], and this study), we conclude that 20 dB channel objective for CAUI-4 chip-to-chip is achievable with confidence/margin, and the following benefits
  - Meet the CAUI-4 end customer requirements (see [3])
  - Enable more applications (e.g., Interlaken MR)
  - Aligned with CEI -28G MR chip-to-chip
  - Enable wide acceptance

References

[1]:http://www.ieee802.org/3/bm/public/jan13/li_01_0113_optx.pdf

[2]:http://www.ieee802.org/3/bm/public/mar13/li_01_0313_optx.pdf

[3]:http://www.ieee802.org/3/bm/public/may13/rabinovich_01_0513_optx.pdf

Acknowledgements

- The author would like to thank Jeremy Buan of Hirose for providing the measured channel S-parameters that are used in this presentation.