Working document: SRS test draft – rev 1

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(post meeting)

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Potential approach for this draft for SRS test

- Follow a similar format to clause 86
  - Reference clause 52 for basic SRS test with exceptions appropriate for 100GBASE-SR4
  - *Petrilla_04_0513_optx* and associated reference spreadsheet suggested:
    - SRS max spec value of -5.1dBm (TBC)
    - SRS test source VECP value of 4.8 dB (TBC)
    - The values in magenta are placeholders, and are expected to be updated. New text or changes to the text in Draft 1p0 are also in magenta.

Reminder of SRS test definition in clause 86

Separate jitter tolerance test needed ?

J9 relevance?
J4

Not relevant

86.8.4.7 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 86–8 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) The reference test procedure for a single lane is defined in 52.9.9. See 86.8.2.1 and below for multi-lane considerations.
b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator.
c) The fourth-order Bessel-Thomson filter is replaced by a low-pass filter followed by a limiter and a fourth-order Bessel-Thomson filter.
d) The sinusoidal jitter is at a fixed 80 MHz frequency and between 0 and 0.05 UI peak-to-peak amplitude.
e) The Gaussian noise generator, the amplitude of the sinusoidal jitter, and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J9 Jitter specifications given in Table 86–8 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).
f) The pattern for the received compliance signal is specified in Table 86–12.
g) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.
h) Where nPPI or XLAUI/CAUI is exposed, a PMD receiver is considered compliant if it meets the module electrical output specifications at TP4 given in Table 86A–3 for nPPI, or the requirements in Table 83B–3 for XLAUI/CAUI.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 86–8. Pattern 3 or Pattern 5, or a valid 40GBASE–R4 or 100GBASE–R10 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 40GBASE-SR4 and 100GBASE-SR10, the relevant BER is the interface BER. The interface BER is the average of the four or ten BERs of the receive lanes when stressed: see 86.8.2.1.

Clause 86 Receiver jitter tolerance section

86.8.4.8 Receiver jitter tolerance

Receiver jitter tolerance shall be as defined as in 68.6.11, with the following differences:

a) The reference test procedure for a single lane is defined in 68.6.11. See 86.8.2.1 for multi-lane considerations.
b) The pattern to be received is specified in Table 86–12.
c) The parameters of the signal are specified in Table 86–8 and the power in OMA at the receiver is set to the maximum for receiver jitter tolerance in OMA given in Table 86–8.
d) Each receive lane is tested in turn while all are operated. All aggressor lanes are operated as specified in Table 86–8.
e) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 40GBASE-R4 or 100GBASE-R10 signal.
f) The transmitter is transmitting one of these signals using all lanes.
g) The transmitter and the receiver are not synchronous.
h) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed.
i) The mode-conditioning patch cord suitable for 62.5/125 µm fiber is not used.

- Need to add similar section to clause 95 (or include it in the SRS test section).

Current text in clause 95

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined in TBD with the following exceptions:

a) Added sinusoidal jitter is as specified in Table 95–11.
b) The stressed eye jitter and vertical eye closure penalty are as given in Table 95–7.
c) The test pattern is as given in Table 95–10.
d) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 95.8.7.

- Clearly incomplete – e.g. needs to reference correct BER for 100GBASE-SR4
- Combines Sinusoidal jitter tolerance and SRS test
- In clause 86, the SRS test method references clause 52 and a list of appropriate exceptions, and has a separate additional section describing jitter tolerance testing, which references clause 68.
  a) We could do the same in clause 95, or
  b) Reference clause 52 for both (with the more usual jitter tolerance mask, and greater commonality with ITU specs for example) rather than the two frequency points in 86, or
  c) Consolidate the SRS and jitter tolerance tests within clause 95 (which would mean a lot of duplication of test diagrams and methodology)

  ……opinions?

Option (a): Proposed text for SRS for clause 95

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) The reference test procedure for a single lane is defined in 52.9.9. See 95.8.1.1 ~~and below~~ for multilane considerations.

b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator.

c) The fourth-order Bessel-Thomson filter is replaced by a low-pass filter followed by a limiter and a fourth-order Bessel-Thomson filter.

d) The sinusoidal jitter is at a fixed 80 MHz frequency and between 0 and 0.05 UI peak-to-peak amplitude.

e) The Gaussian noise generator, the amplitude of the sinusoidal jitter, and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J4 Jitter specifications given in Table 95–7 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).

f) The pattern for the received compliance signal is specified in Table 95–10.

g) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 95–7. Pattern 3 or Pattern 5, or a valid 100GBASE–R4 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 100GBASE-SR4 the relevant BER is the interface BER. The interface BER is the average of the four BERs of the receive lanes when stressed: see 95.8.1.1.

Option (a):Proposed text for Receiver jitter tolerance for clause 95

95.8.9 Receiver jitter tolerance

Receiver jitter tolerance shall be as defined as in 68.6.11, with the following differences:

a) The reference test procedure for a single lane is defined in 68.6.11. See 95.8.1.1 for multi-lane considerations.

b) The pattern to be received is specified in Table 95–10.

c) The parameters of the signal are specified in Table 95–7 and the power in OMA at the receiver is set to the maximum for receiver jitter tolerance in OMA given in Table 95–7.

d) Each receive lane is tested in turn while all are operated. All aggressor lanes are operated as specified in Table 95–7.

e) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 100GBASE-R4 signal.

f) The transmitter is transmitting one of these signals using all lanes.

g) The transmitter and the receiver are not synchronous.

h) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed.

i) The mode-conditioning patch cord suitable for 62.5/125 mm fiber is not used.

Ed Note to be removed: Table 95–7 needs changes and added lines (if following format of Table 86-8) to show aggressor channel power and jitter points for SRS and jitter tolerance tests.

Option (a): Changes and additions to Table 95-7

Table 95–7—100GBASE-SR4 receive characteristics *(continued)*

Description	Value	Unit
Stressed receiver sensitivity (OMA), each lane[c] (max)	TBD	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty (VECP),[d] each lane	TBD	dB
Stressed eye J2 jitter,[d] each lane	TBD	UI
Stressed eye J4 jitter,[d] each lane	TBD	UI
OMA of each aggressor lane	TBD	dBm
Receiver jitter tolerance in OMA, each lane (max)[e]	TBD	dBm
Conditions of receiver jitter tolerance test:		
Jitter frequency and peak-to-peak amplitude	(190, 5)	kHz, UI
Jitter frequency and peak-to-peak amplitude	(940, 1)	kHz, UI
OMA of each aggressor lane	TBD	dBm

[c] Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.

[d] Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

[e] This is a test of the optical receiver's ability to track low frequency jitter, and is inappropriate for any subsystem that does not include a CRU

Further work

- For the SRS test, we need proposed text for an exception which describes the SRS test source eye-mask.
- Values to replace TBDs in Table 95-7.

Back-up

Snapshot of ‘ExampleMMF_LinkModel_130503.xls’ from John Petrilla – to be updated

Spreadsheet by Del Hanson, David Cunningham, Piers Dawe, David Dolfi Agilent Technologies

Rev. 3.2/3 This file 10GEPBud3_1_16a.xls of 17-Oct-01

Model/format rev 3.1.16a of 31-Oct-01

Basics	Input=	Bold		Ts(20-80)	21.0	ps	Case: 850nm serial	newMMF	Attenuation=	3.5	dB/km	NomSens OMA	-11.20	dBm	Margin	0.00	dB at
	Q=	3.8905		Ts(10-90)	31.9	ps	*Target* Target reach	0.100	km	*Fiber* at	850	nm	*Receive* Refl Rx	-12	dB	*Answer!*	0.1	km
	Base Rate=	25781.3	MBd	RIN(OMA)	-128.0	dB/Hz	*and* L_start=	0.05	km	C_att=	1.00		Rec_BW=	18,047	MHz	est Rx BW	19,336	MHz
Transmitter				RIN at MinER	-135.3	dB/Hz	*graph* L_inc=	0.005	km	Attenuation=	3.62	dB/km	c_rx	329	ns.MHz			
Wavelength Uc		840	nm	RIN_Coef=	0.70		Power Budget P=	8.20	dB	at	840	nm						
RMS Width, Uw		0.60	nm	DJ+ & TP4eye	21.4	ps	inc. DCD Connections etc	1.50	dB	Disp. min. Uo=	1316	nm	T_rx(10-90)	18.2	ps	Test Source ER=		
Tx pwr OMA=		-3.00	dBm	DCD_DJ=	1.94	ps	TP3 Pwr.Bud.-Conn.Loss	6.7	dB	Disp. So=	0.1028	ps/nm^2*km	TP4 Eye	8	ps	*Test Tx*	6.5	dB
Min. Ext Ratio=		4.00	dB	Effect. DJ=	0.53	(UI)	ex DCD C1=	480	ns.MHz	Disp. D1=	-108.41	ps/(nm.km)	Opening		(=Tx ey	TestERper	1.98	dBo
Worst"ave.TxPwr		-2.35	dBm	MPN k(OMA)	0.3		Reflection Noise factor	0	no units				RMS Baseline wander SD	0.025	fraction of 1/2 eye			
Ext. ratio penalty		3.66	dBo	Tx eye height	10.4%		Effective Rate	27138	MBd	(not in use)	10					V.E.C.P.	4.81	dBo
Tx mask	X1=	0.3	UI	Refl Tx	-12	dB	Tb_eff=	37	ps	BWm=	4400	MHz*km	P_BLW(no ISI)	0.02	dB			Stressed
	X2=	0.4	UI	ModalNoisePen	0.129	dB	Effective Rec Eye	0.21	UI	Eff. BWm=	4.4E+03	MHz*km	P_BLW	0.02	dB			Rx sens
	Y1=	0.25		Tx mask top	0.2	UI												

L	Patt	Ch IL	D1.L	D2.L	BWcd	effBWm	Te	Tc	Pisi central	P Eye corners	P_DJ central	P_DJ corners	Preflection central	Beta	SDmpn	Pmpn	Prin	Pcross central	Ptotal central	<Ptotal corners	LP Pen central	Margin	OMA central
(km)	(dB)	(dB)	ps/nm	ps/nm	(MHz)	(MHz)	(ps)	(ps)	J=0, dB	(dB)	(dB)	(dB)	(dB)			(dB)	(dB)	(dB)	(dB)	(dB)	(dB)	(dB)	(dBm)
0.002	0.01	1.51	-0.22	0.00	1E+06	#######	32	37	2.20	0.24	1.71	3.80		-1E-02	0.00	0.00		0.40	4.45	6.78	4.4	2.2	-4.8
0.05	**0.18**	**1.68**	**-5.4**	**0.00**	**57,497**	**88,000**	**33**	**38**	**2.44**	0.24	**1.72**	3.84	**0**	**-0.28**	**0.02**	**0.01**	**0.66**	**0.25**	**5.4**	7.7	**5.2**	**1.3**	**-5.6**
0.055	0.20	1.70	-6.0	0.00	52,270	80,000	34	38	2.49	0.24	1.73	3.84	0	-0.30	0.02	0.01	0.66	0.25	5.5	7.8	5.3	1.2	-5.6
0.06	0.22	1.72	-6.5	0.00	47,914	73,333	34	39	2.54	0.24	1.73	3.85	0	-0.33	0.02	0.02	0.66	0.26	5.6	7.9	5.3	1.1	-5.7
0.065	0.24	1.74	-7.0	0.00	44,228	67,692	34	39	2.60	0.24	1.73	3.86	0	-0.36	0.03	0.02	0.66	0.27	5.7	8.0	5.4	1.0	-5.7
0.07	0.25	1.75	-7.6	0.00	41,069	62,857	35	39	2.67	0.24	1.74	3.87	0	-0.39	0.03	0.03	0.67	0.29	5.8	8.2	5.5	0.9	-5.7
0.075	**0.27**	**1.77**	**-8.1**	**0.00**	**38,331**	**58,667**	**35**	**40**	**2.74**	0.24	**1.74**	3.89	**0**	**-0.42**	**0.03**	**0.04**	**0.67**	**0.30**	**5.9**	8.3	**5.6**	**0.8**	**-5.8**
0.08	0.29	1.79	-8.7	0.00	35,936	55,000	36	40	2.81	0.24	1.74	3.90	0	-0.44	0.04	0.05	0.68	0.32	6.0	8.4	5.7	0.7	-5.8
0.085	0.31	1.81	-9.2	0.00	33,822	51,765	36	40	2.89	0.25	1.75	3.92	0	-0.47	0.04	0.06	0.69	0.35	6.2	8.6	5.9	0.5	-5.9
0.09	0.33	1.83	-9.8	0.00	31,943	48,889	37	41	2.98	0.25	1.75	3.93	0	-0.50	0.05	0.07	0.70	0.37	6.3	8.8	6.0	0.4	-5.9
0.095	0.34	1.84	-10.3	0.00	30,261	46,316	37	41	3.07	0.25	1.76	3.95	0	-0.53	0.05	0.09	0.72	0.41	6.5	9.0	6.2	0.2	-6.0
0.10	**0.36**	**1.86**	**-10.8**	**0.00**	**28,748**	**44,000**	**38**	**42**	**3.16**	0.25	**1.76**	3.98	**0**	**-0.55**	**0.06**	**0.11**	**0.74**	**0.44**	**6.7**	9.2	**6.34**	**0.00**	**-6.1**

- SRS = -5.1 dBm for 100 m OM4
- VECP = 4.8 dB

SRS and receiver jitter tolerance test conditions in Table 86-8

Conditions of stressed receiver sensitivity test:				
	Vertical eye closure penalty (VECP)[c], each lane	—	1.9	dB
	Stressed eye J2 Jitter[c], each lane	—	0.3	UI
	Stressed eye J9 Jitter[c], each lane	—	0.47	UI
	OMA of each aggressor lane	—	–0.4	dBm
Receiver jitter tolerance in OMA, each lane[d]		Max	–5.4	dBm
Conditions of receiver jitter tolerance test:				
	Jitter frequency and peak-to-peak amplitude	—	(75, 5)	(kHz, UI)
	Jitter frequency and peak-to-peak amplitude	—	(375, 1)	(kHz, UI)
	OMA of each aggressor lane	—	–0.4	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Measured with conformance test signal at TP3 (see 86.8.4.7).
[c]Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant.
[d]This is a test of the optical receiver's ability to track low-frequency jitter and is inappropriate for any subsystem that does not include a CRU.

Table 95-7 in Draft 1p0

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Lane wavelengths (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–11 TBC	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	TBD	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty,[d] each lane	TBD	dB
Stressed eye jitter,[d] each lane	TBD	UI

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with TBD test signal at TP3 for the BER specified in 95.1.1.