Proposed text for P802.3bm D1p0: SRS and receiver jitter tolerance

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Proposed text for SRS for clause 95

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) The reference test procedure for a single lane is defined in 52.9.9. See 95.8.1.1 ~~and below~~ for multilane considerations.

b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator.

c) The fourth-order Bessel-Thomson filter is replaced by a low-pass filter followed by a limiter and a fourth-order Bessel-Thomson filter.

d) The sinusoidal jitter is at a fixed 80 MHz frequency and between 0 and 0.05 UI peak-to-peak amplitude.

e) The Gaussian noise generator, the amplitude of the sinusoidal jitter, and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J4 Jitter specifications given in Table 95–7 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).

f) The pattern for the received compliance signal is specified in Table 95–10.

g) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 95–7. Pattern 3 or Pattern 5, or a valid 100GBASE–R4 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 100GBASE-SR4 the relevant BER is the interface BER. The interface BER is the average of the four BERs of the receive lanes when stressed: see 95.8.1.1.

Proposed text for Receiver jitter tolerance for clause 95

95.8.9 Receiver jitter tolerance

Receiver jitter tolerance shall be as defined as in 68.6.11, with the following differences:

a) The reference test procedure for a single lane is defined in 68.6.11. See 95.8.1.1 for multi-lane considerations.

b) The pattern to be received is specified in Table 95–10.

c) The parameters of the signal are specified in Table 95–7 and the power in OMA at the receiver is set to the maximum for receiver jitter tolerance in OMA given in Table 95–7.

d) Each receive lane is tested in turn while all are operated. All aggressor lanes are operated as specified in Table 95–7.

e) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 100GBASE-R4 signal.

f) The transmitter is transmitting one of these signals using all lanes.

g) The transmitter and the receiver are not synchronous.

h) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed.

i) The mode-conditioning patch cord suitable for 62.5/125 mm fiber is not used.

Ed Note to be removed: Table 95–7 needs changes and added lines (if following format of Table 86-8) to show aggressor channel power and jitter points for SRS and jitter tolerance tests.

Proposed changes and additions to Table 95-7

Table 95–7—100GBASE-SR4 receive characteristics *(continued)*

Description	Value	Unit
Stressed receiver sensitivity (OMA), each lane[c] (max)	TBD	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty (VECP),[d] each lane	TBD	dB
Stressed eye J2 jitter,[d] each lane	TBD	UI
Stressed eye J4 jitter,[d] each lane	TBD	UI
OMA of each aggressor lane	TBD	dBm
Receiver jitter tolerance in OMA, each lane (max)[e]	TBD	dBm
Conditions of receiver jitter tolerance test:		
Jitter frequency and peak-to-peak amplitude	(190, 5)	kHz, UI
Jitter frequency and peak-to-peak amplitude	(940, 1)	kHz, UI
OMA of each aggressor lane	TBD	dBm

[c] Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.

[d] Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

[e] This is a test of the optical receiver's ability to track low frequency jitter, and is inappropriate for any subsystem that does not include a CRU

Notes

- For the SRS test, we need proposed text for an exception which describes the SRS test source eye-mask.
- Values are needed to replace TBDs in Table 95-7.
- The values in magenta are placeholders, and are expected to be updated. New text or changes to the text in Draft 1p0 are also in magenta.