

FEC Latency Considerations

Andre Szczepanek

Supporters

- Vipul Bhatt (Cisco)
- Arash Farhood (Cortina)
- Sudeep Bhoja (Inphi)
- xxxx

Overview

- Evaluate the additional latency introduced if FEC is implemented outside of the MAC ASIC.
 - As required by :
 - SR4, CR4, PAM-N Multilevel coding schemes,
 - Existing legacy hosts that don't support 802.3bj NRZ FEC

- I have heard concerns raised that implementing FEC outside the MAC may be impractical due to added latency
 - So let's quantify what is possible in a vanilla 40nm TSMC CMOS process

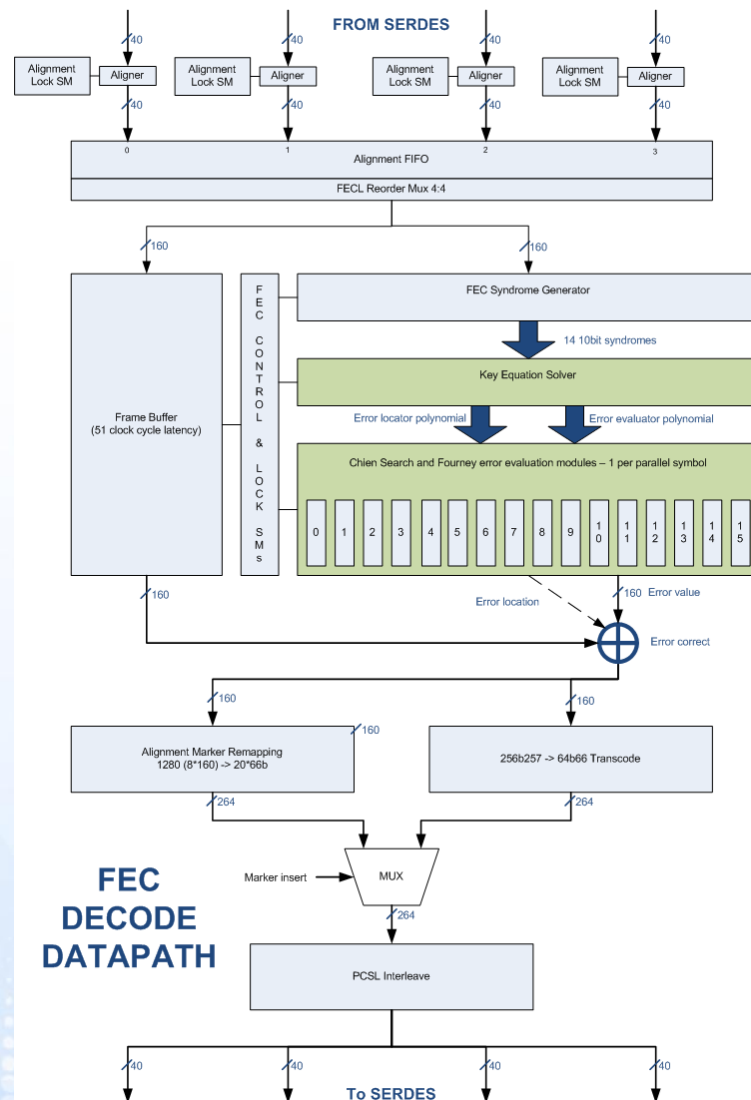
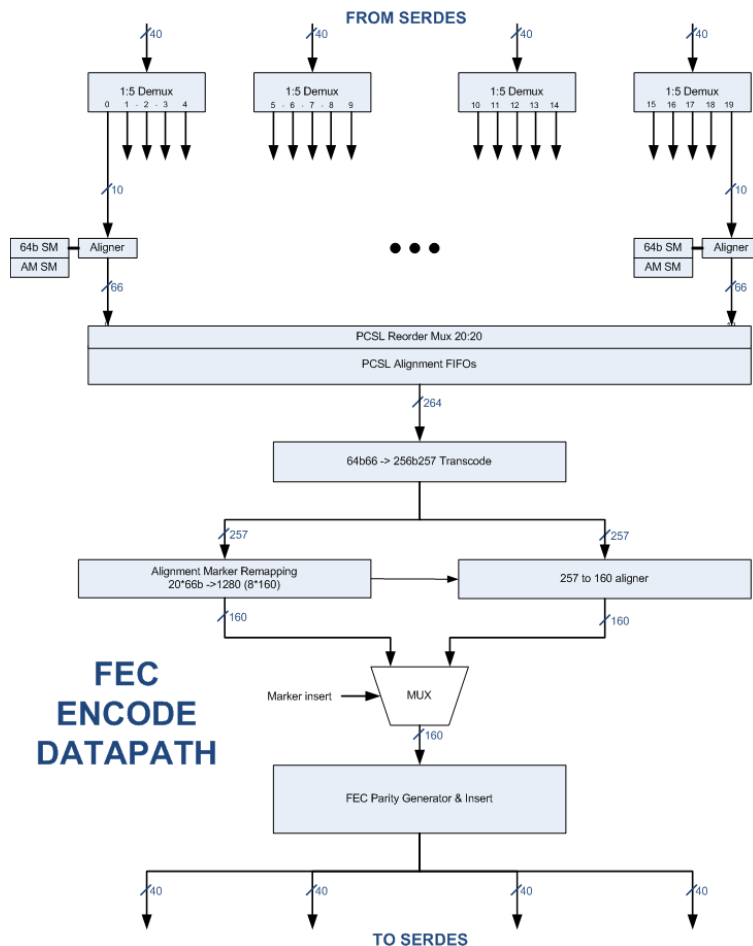
Assumptions

- Static skew due to optics in a 802.ba/bm link only needs to be removed once
 - If it is removed by a FEC PCS in a module it won't be removed again by the PCS in the MAC ASIC
 - No double-counting !
- So latency due to Static skew removal in a FEC PCS should not be counted as part of the latency “cost” of implementing a FEC PCS
- 802.3bj KR4 FEC

An implementation

- Prototype FEC datapath RTL, synthesized to a 40nm TSMC CMOS library
- 644Mhz datapaths (160bit @ 100Ge)
 - 1.5515ns clock cycle

Block Diagrams



FEC encoder Latency

■ Latency breakdown

- 64b66b Alignment, FIFOS, and PCSL ordering
 - 6 clock cycles (excluding static latency provision)
 - 9.3ns
- Transcoding & mapping
 - 2 clock cycles
 - 3.1ns
- Parity generation
 - 2 clock cycles
 - 3.1ns

■ Total encode latency = 15.5ns

■ Latency Delta vs FEC on MAC = 12.4ns

FEC decoder Latency

■ Latency breakdown

- FEC Alignment, FIFOS, and FEC ordering
 - 9 clock cycles
 - excluding static latency provision, but including dynamic skew
 - 14ns
- FEC error correction datapath
 - Syndrome generator, Key Equation Solver, Chien/Fourney
 - 51 clock cycles
 - 79.1ns
- Transcoding & mapping
 - 2 clock cycles
 - 3.1ns

■ Total decode latency = 96.2ns

■ Latency Delta vs FEC on MAC = 17.3ns

Conclusions

- The additional Latency introduced by implementing the 802.3bj FEC outside of the MAC can be less than 30ns
 - Encoder delta plus Decoder delta = $12.4 + 17.3 = 29.7\text{ns}$
- The additional latency caused by implementing FEC on a module is not a show-stopper.
 - It is practical to implement FEC outside the MAC
 - PCS latency concerns should not preclude the use of different FEC coding for optical links