## Investigation of 100 GbE Based on PAM-4 and PAM-8 <br> IEEE 802.3bm Task Force

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## Agenda

- System Overview
- Electronics Front End
- Retimer and FEC
- Electro-Optical Subsystems
- PAM-N Transmitter/DAC
- PAM-N Receiver
- Optical Link Budgets Implications
- PAM-4 operate with more relax link parameters (lower RIN and less power) but require faster electronics but less ENOB, and BJ FEC likely sufficient
- PAM-8 link must operate with very strengthen link parameters (higher RIN and and more power) but require more moderate speed electronics but with higher ENOB, and would require stronger FEC than BJ FEC
- Electronics Back End
- ADC/Decoder


## PAM-4 vs PAM-8 Implementation

- PAM-4

- PAM-8


CAUI-4

* BJ FEC maybe sufficient for PAM-4


## PAM-8 vs PAM-4 Link Budget


-12.0 dBm 51G NRZ Optical Rx for 1E-5 BER (Assumes $15 \mathrm{~A} / \mathrm{sqrt}(\mathrm{Hz})$, see back

-16.05 dBm 34G NRZ Optical Rx for 1E-5 BER (Assumes $15 \mathrm{~A} /$ sqrt(Hz), see backup)

Simply a reference sensitivity of an NRZ signal at 34G

## PAM-N Electro-Optical Subsystems

## Transmitters

- PAM8 and PAM4 transmitters @ 34.375G and 51.5625G
- Three and Two segment electrooptical DACs
- Segmented Mach Zender Interferometer type
- CMOS Inverter diode drive Mild inductive pre-emphasis
- High Bandwidth MZI
- PN BW > 100 GHz
- 40 nm CMOS


## Receivers

- PAM8 and PAM4 receivers @ 34.375G and 51.5625G
- Linear front end to drive electrical ADC
- Mild linear equalization
- Integrated Photodetector
- Germanium on waveguide
- 3dB BW ~ 50 GHz
- Receiver BW (TIA+PD)
- PAM8 ~ 22 GHz
- PAM4 ~ 26 GHz
- 40 nm CMOS


## PAM-N Electro-Optical Subsystems

## Conditions

- Electro-Optical Link Deterministic Simulations
- Captures deterministic performance only, not Gaussian noise effects
- Excludes source jitter
- Assumes ideal input NRZ streams
- Excludes laser RIN


## Results

1. Transmitter Performance
2. Receiver Performance I

- Driven by optical transmitter
- Noiseless

3. Receiver Performance II

- Driven by optical transmitter
- PD and TIA noise
- No laser RIN


## Actual Circuit Simulation of the Transmitter



## Actual Receiver Circuit Performance I Noise Free



PAM8 @ 34.37G


PAM4 @ 51.5625G

## Actual Receiver Receiver Performance II With Noise



PAM8 ~ 8.5k UI

## PAM-N Link Penalties

## PAM 8

- Vertical Eye Closure ~ 8.8 dB
- PAM8 Loss $=8.4 \mathrm{~dB}$
- Linearity Penalty ~ 0.4 dB
- Horizontal Eye Closure
- Noise Less ~ 0.47 UI
- With Noise $\sim 0.56$ UI


## PAM 4

- Vertical Eye Closure ~ 4.87 dB
- PAM8 Loss $=4.77 \mathrm{~dB}$
- Linearity Penalty ~ 0.1 dB
- Horizontal Eye Closure
- Noise Less ~ 0.36 UI
- With Noise ~ 0.46 UI


## Jitter Budget

## PAM8

| Module CDR | Optical TX | Optical RX | ADC Input |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { DJ }=2 \mathrm{ps} \\ \text { RJ (RMS) }=0.1 \mathrm{ps} \end{gathered}$ | $\begin{gathered} \text { DJ }=8.5 \mathrm{ps} \\ \text { RJ (RMS) }=0.1 \mathrm{ps} \end{gathered}$ | DJ $=5.17 \mathrm{ps}$ RJ (RMS) $=0.31 \mathrm{ps}$ | $\begin{gathered} \text { DJ-Out }=15.67 \mathrm{ps} \\ \text { RJ (RMS) }=0.34 \mathrm{ps} \\ \text { TJ (BER5) }=18.58 \mathrm{ps} \end{gathered}$ |

## PAM4

Module CDR

DJ = 1.5 ps
RJ (RMS) = 0.1 ps

| Optical TX | Optical RX | ADC Input |
| :---: | :---: | :---: |
| $\begin{aligned} \text { DJ } & =5.0 \mathrm{ps} \\ \text { RJ (RMS) } & =0.03 \mathrm{ps} \end{aligned}$ | $\begin{gathered} \mathrm{DJ}=1.98 \mathrm{ps} \\ \text { RJ (RMS) }=0.21 \mathrm{ps} \end{gathered}$ | $\begin{gathered} \text { DJ-Out }=8.48 \mathrm{ps} \\ \text { RJ (RMS) }=0.26 \mathrm{ps} \\ \text { TJ (BERS) }=10.48 \mathrm{ps} \end{gathered}$ |

## Basic Simulation Assumptions

- Modulator is MZ type
- In case of PAM-8, 3 input signals with amplitude $1 / 7,2 / 7$, and $4 / 7$ are linearly summed into MZ modulator
- In case of PAM-4, 2 input signals with amplitude 1/3, $2 / 3$ are linearly summed into MZ modulator
- Modulator Type MZ RC BW of 34 GHz zero chirp for both PAM-4 and PAM-8
- Input electrical signal $\mathrm{V} \pi / 2$ to limit the compression
- $\mathrm{RIN}=-149 \mathrm{dBm} / \mathrm{Hz}$ for PAM-8 and -145 for PAM-4
- TX Wavelength=1280 nm and linewidth 100 MHz
- TX DJ $=2$ ps for PAM-8 and 1.5 ps for PAM-4
- TX Output Power = - 2 dBm OMA for PAM-8 and -4 dBm for PAM-4
- Optical transmitter 20-80\% rise/fall 12 ps for PAM-8 and 8 ps for PAM-4
- Data pattern=PN12
- Extinction Ratio= 6.5 dB
- Receiver BW=28 for PAM-8 and 34 GHz for PAM-4
- Receiver sensitivity PAM-8-16 dBm OMA at 1e-5 and PAM-4 -12 dBm OMA at 1e-5


## Block Diagram of PAM-4 and PAM-8

- Rsoft Schematic



## PAM-4 Optical Receiver Response

- Response of a realistic PD+TZ AMP with 34 GHz BW and sensitivity of $1 \mathrm{e}-5$ at -13 dBm AOP or -12 dBm OMA at ER=6.5 dB PAM-4 Receiver



## PAM-8 Optical Receiver Response

- Response of a realistic PD+TZ AMP with 28GHz BW and sensitivity of $1 \mathrm{e}-5$ at -17 dBm AOP or -16 dBm OMA at ER=6.5 dB PAM-8 Receiver


$\mathrm{f}(\mathrm{Hz})$


## Optical Transmitter PAM-2 Response

## - At 34.37 GBd and 51.5625 GBd

- The components are limiting the 51.56 GBd operation but still PAM-4 link perform better than PAM-8


PAM-4 Link Operating at 53.1 Gbd with $O \mathrm{MA}=-4.8$


## PAM-4 and PAM-8 Transmit Optical Eye

- PAM-4 Tr=8 ps, $\sigma=0.14 \mathrm{ps}, \mathrm{PJ}=1.5 \mathrm{ps}$
- PAM-8 Tr=12 ps, $\sigma=0.1 \mathrm{ps}, \mathrm{PJ}=2 \mathrm{ps}$
- Segmented balance modulator will improve both eyes



## PAM-4 Receiver

- PAM-4 eye Diagram at OMA=-4.7 dBm and link sensitivity for PAM-2
- PAM-8 sensitivity subtract 0.8 dB for MPI and $\sim 0.4 \mathrm{~dB}$ for other penalty sensitivity at $\mathrm{AOP}=-11.8 \mathrm{dBm}$ (at $\mathrm{ER}=6.5 \mathrm{OMA}=\mathrm{AOP}-1$ )
- Estimated BER is 8e-6 but actual BER may be worse due to non-linear distortion and jitter interaction
- The link does have some modest amount of ISI that can be equalized


PAM-4 Receiver Sensitivity


## PAM-8 Receiver

- PAM-8 eye Diagram at OMA=-4.7 dBm and link sensitivity for PAM-2
- PAM-8 sensitivity subtract 1.8 dB for MPI and $\sim 0.4 \mathrm{~dB}$ for other penalty from AOP of -17 dBm (at $\mathrm{ER}=6.5 \mathrm{OMA}=\mathrm{AOP}-1$ )
- Estimated BER is 2e-5 but actual BER may be worse due to non-linear distortion and jitter interaction
- Due to high BW component link has very little ISI and is noise limited



## Noise Free PAM-4/PAM-8 Eyes - without and with PJ

- BER estimate may be to optimistic due to non-linear distortions and jitter
- Equalization may help open the eye when link is not noise limited and distortion is linear



## Multiple Patch Cords Reference Model

- Multipath Penalty with up to 3 patch cords are analyzed in http://www.ieee802.org/3/100GNGOPTX/public/mar12/plenary/ghiasi 03 0312_NG100GOPTX.pdf
- It is reasonable to assume that all mid-span connectors have RL of -35 dB a modest improvement from 1 GbE RL of 26 dB
- Assume both TOSA/ROSA will have RL of -21 dB or better - 100Gbase-LR4/ER4 have RL of -12 dB for the TOSA and -26 dB for the ROSA
- Next gen SMF PMD key advantage as stated is low cost and requiring high RL will drive the cost up http://www.ieee802.org/3/100GNGOPTX/public/jan12/nicholl_01_0112_NG100GOPTX.pdf



## Multipath Interference Penalty

- Assuming TOSA/ROSA dominates MPI at -21 dB
- MPI penalty for PAM-4=0.8 dBo
- MPI penalty for PAM-8=1.7 dBo



## FEC Requirements

- Raw BER will be 1E-5 (Q=4.27) and minimum BER with FEC 1E-17 (Q=8.49) or better
- Require min FEC gain of 6 dB , for actual FEC option see http://www.ieee802.org/3/bm/public/sep12/wang 010912 optx.pdf



## Feasibility of CMOS Operating at 34.37 GBd and 51.56 GBd

- Jun Cao, et al, "A 500 mW ADC-Based CMOS AFE with Digital Calibration for $10 \mathrm{~Gb} / \mathrm{s}$ Serial Link, ISSCC 2010",65 nm CMOS 4 way interleaved with with T-spaced FFE with power efficiency of 1.4 pj per conversion step
- Fujitsu announces on Sept 13201065 Gs/s ADC in 65 nm CMOS
- OIF starts OIF-56G-VSR project April 2012
- Broadcom announces on March $5^{\text {th }} 2012$ OTU-3 Mux/Demux capable of operation at 44 GBd in 40 nm CMOS
- Altera announces 40 GBd transceivers in 20 nm CMOS date Sept 52012


## PAM-4 vs PAM-8 PD

- FEC and DAC/ADC will determine the PAM-4 vs PAM-8 PD
- DAC/ADC PD estimated from http://www.slideshare.net/kennliu/fujitsu-iccad-presentationenable-100g? from=share email and assuming 28 nm CMOS
- Assuming PAM-4 DAC and ADC have ENOB of 5 bits
- Assuming PAM-8 DAC and ADC have ENOB of 6.4 bits

| PAM-4 vs PAM-8 | PAM-4 |  | PAM-8 |  |
| :--- | :---: | :---: | :---: | :---: |
| Loss at 14 GHz lin | Std MZM | Seg MZM | Std MZM | Seg MZM |
| CAUI-4 System Interface (W) | 0.80 | 0.80 | 0.80 | 0.80 |
| Laser (W) | 0.13 | 0.13 | 0.20 | 0.20 |
| TEC (W) | 0.00 | 0.00 | 0.00 | 0.00 |
| Mod Driver or Segmented Driver (W) | 1.00 | 0.30 | 0.60 | 0.20 |
| DAC or Gearbox/Bitmux (W) | 0.21 | 0.20 | 0.24 | 0.13 |
| FEC (W) | NA | NA | 0.35 | 0.35 |
| TIA (W) | 0.15 | 0.15 | 0.10 | 0.10 |
| ADC (W) | 0.32 | 0.43 | 0.57 | 0.57 |
| Total PD (W) | 2.6157 | 2.0050 | 2.8525 | 2.3467 |

## PAM-4 vs CAP/QAM-16

- PAM-4

- CAP/QAM-16


CAUI-4
CAP/QAM-16 due excess BW needed similar front end as PAM-4

## Summary

- Next generation SMF PMD targeted for cost sensitive data center application with reach of 500 m
- These application are latency sensitive and if we require a FEC with double the BJ latency would be non starter!
- A non BJ FEC would also require the PCS adding ~250 ns of latency
- As we search for lowest cost and power PMD we need to keep an eye on the key cost driver in these serial optical links
- RIN, TOSA/ROSA RL, connector RL, total link budget/power, and the baudrate
- Actual device implementation show feasibility of PAM-4/PAM-8
- For nearly identical transmitters and receivers, PAM-4 has greater margin and with more relax link budget
- Link budget simulation indicate BJ FEC is likely sufficient for PAM-4 but even with a hot transmitter BJ FEC is not sufficient to close the PAM-8 link budget
- Development in the 100G coherent and 56G VSR are/will make higher speed components more available.

Thank You

