Options and Simulation of CAUI-4

IEEE 802.3bm Task Force

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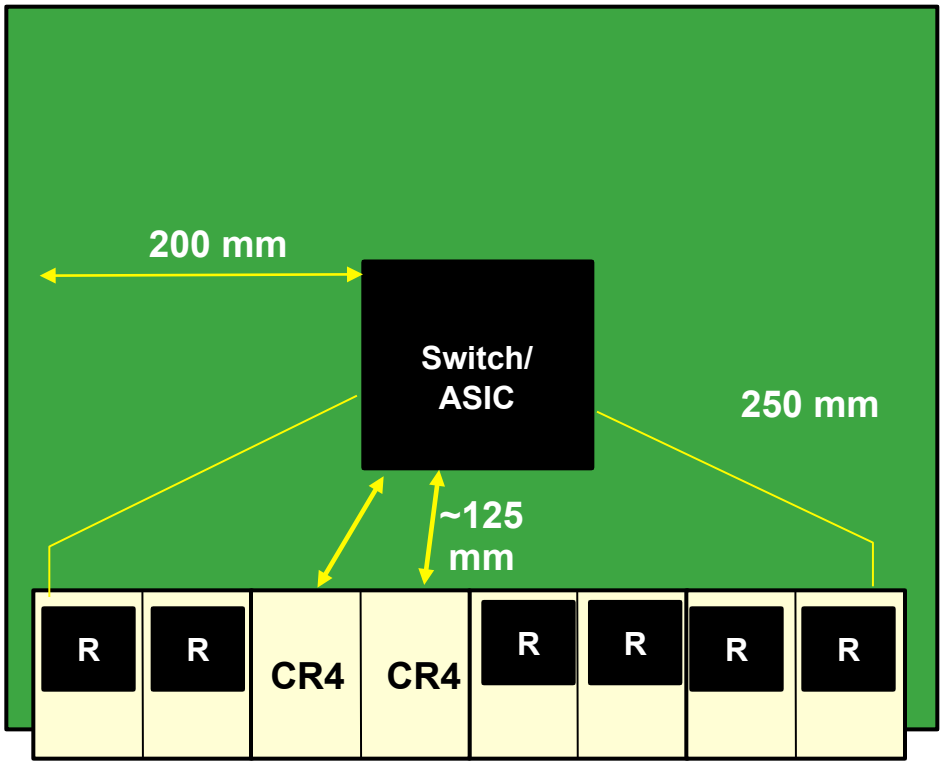
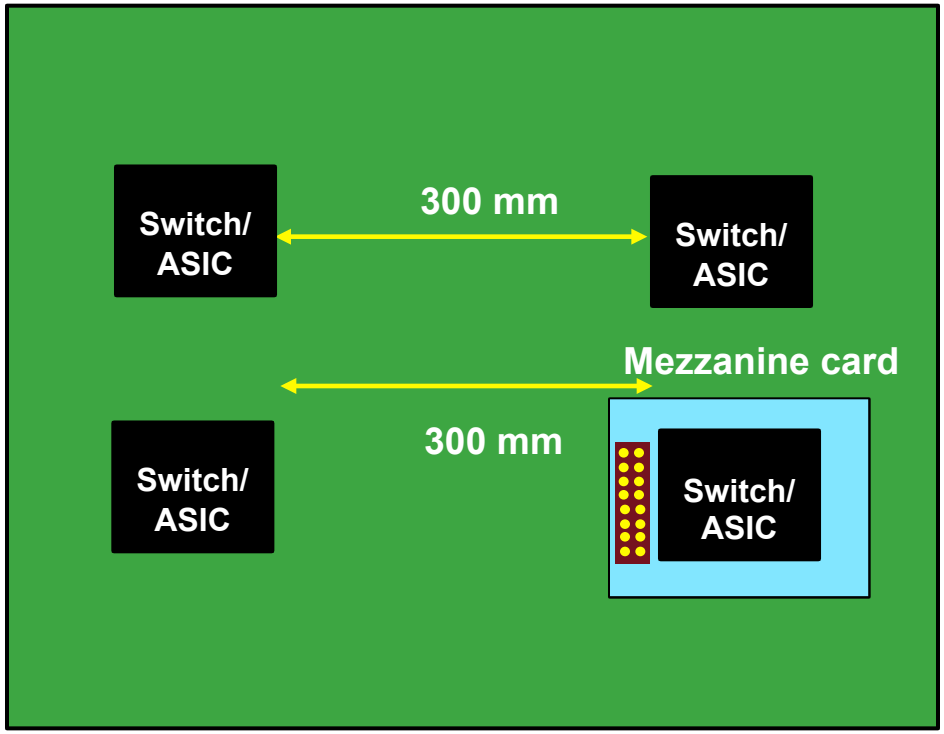
Overview

- CAUI-4 applications
- CAUI-4 channels
- CTLE
- CAUI-4 simulations
- Implication and feasibility of higher loss budget CAUI-4

CAUI-4 Applications and Background

- http://www.ieee802.org/3/bj/public/jul12/ghiasi_02a_0712.pdf identified CAUI-4 applications as well as limitations
  - A receiver with CTLE+1-2 tap DFE can support 18-20 dB loss budget and with a common interface for chip to module and chip to chip
  - A key constrain identified was commonality with CR4 and power penalty in the module which further constrain the above assumption



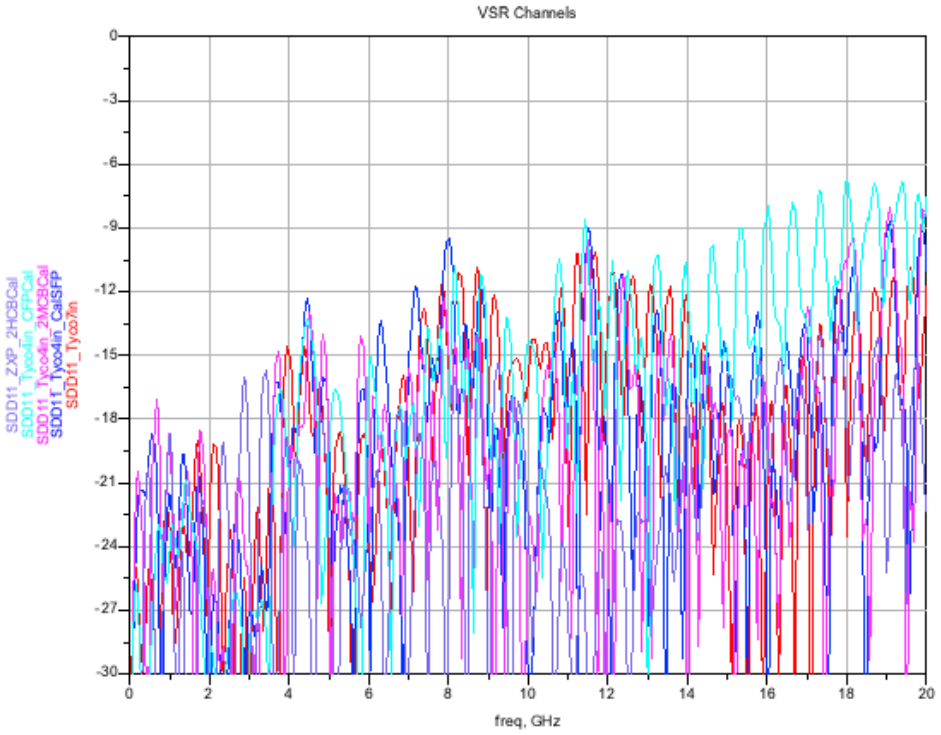


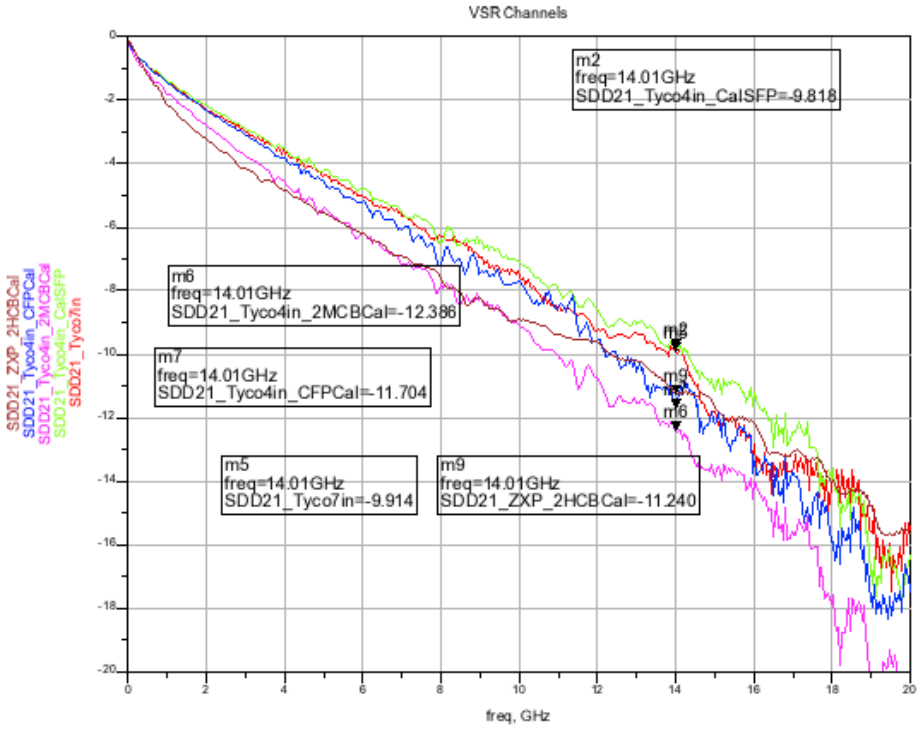
Reality Check 2 Month Later

- Mr. Latchman hosted several conference calls to study CAUI-4 solution for chip to module and chip to chip plus the commonality with CR4
  - Port commonality with CR4 is strongly desired with maximum mated channel loss of 10 dB
  - One may push the CAUI-4 loss budget by 2-3 dB assuming CTLE in the module but does not solve large ASIC driving 12-15” of PCB
  - There is also a need for chip to chip interface with loss budget of 18-20 dB, the question is do we define it in IEEE or just use the OIF-28G-MR
  - ICN and return loss for some of the next generation connectors are not as good as early VSR connectors, the extra margin may quickly evaporate
  - There was also interest to define informative annex how to engineer the CAUI-4 chip to module for greater than 10 dB at expense of CR4 compatibility
- Additional factor constraining solution space is that fact market wants the same interface on CFP2/CFP4, where generational improvement in CDR PD having DFE not possible
- Considering all the constrain keeping chip to module interface at 10 dB is the best option as other option is likely too little to be gained.

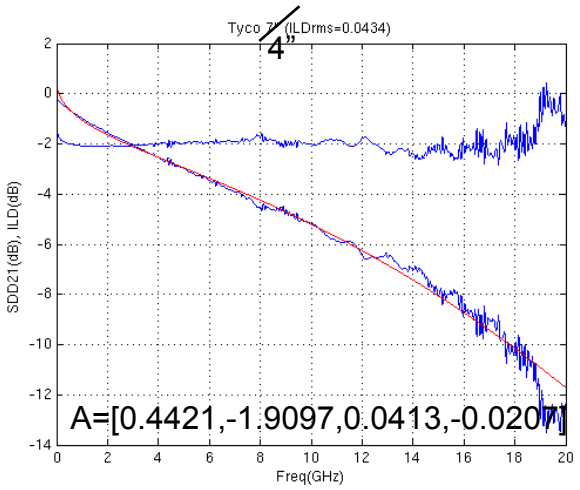
CAUI-4 Chanel RL and IL

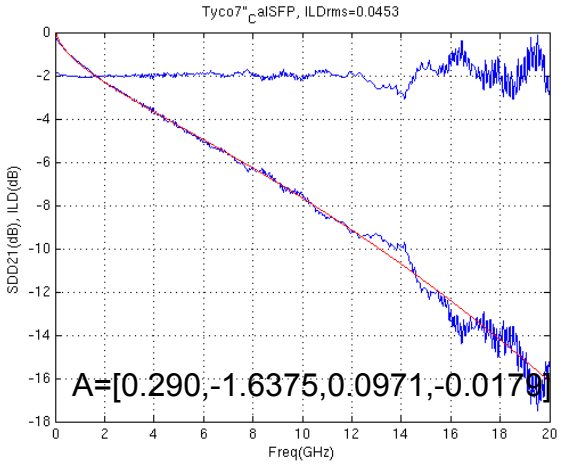
- Channel ILD, return loss, crosstalk, and sqrt(f) drives the far end eye
  - 5 channels are shown here but result for 3 channels are compared

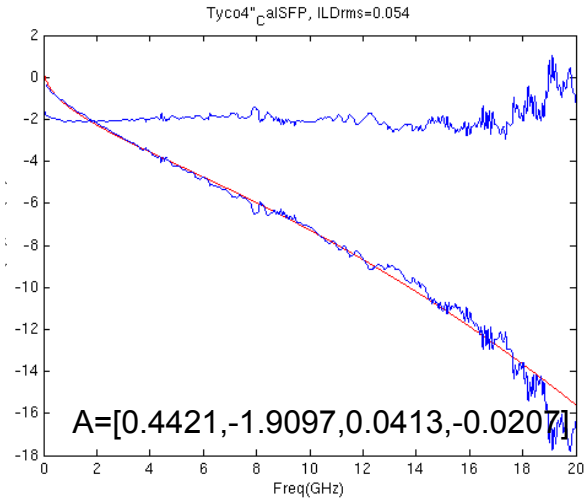


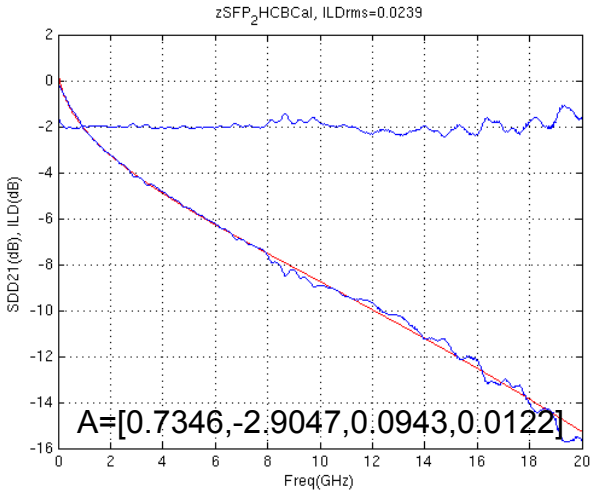


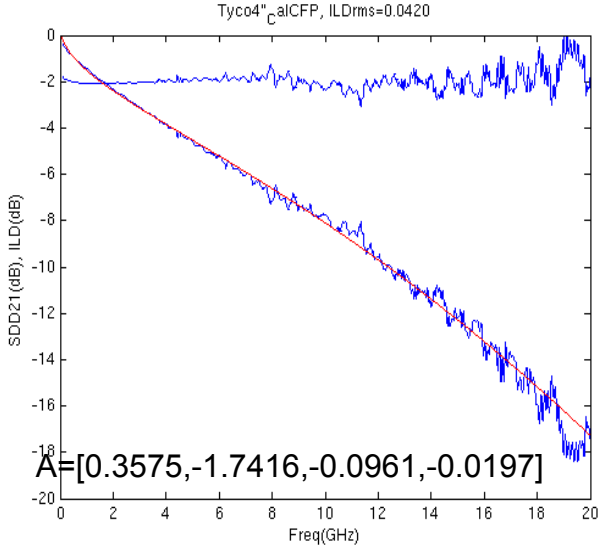
Channel ILD and Fit

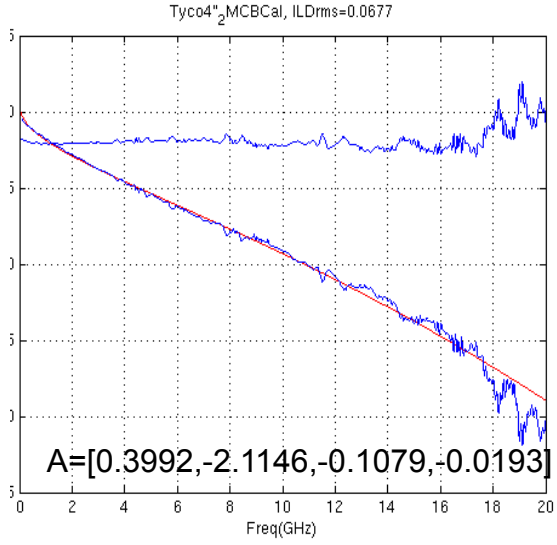








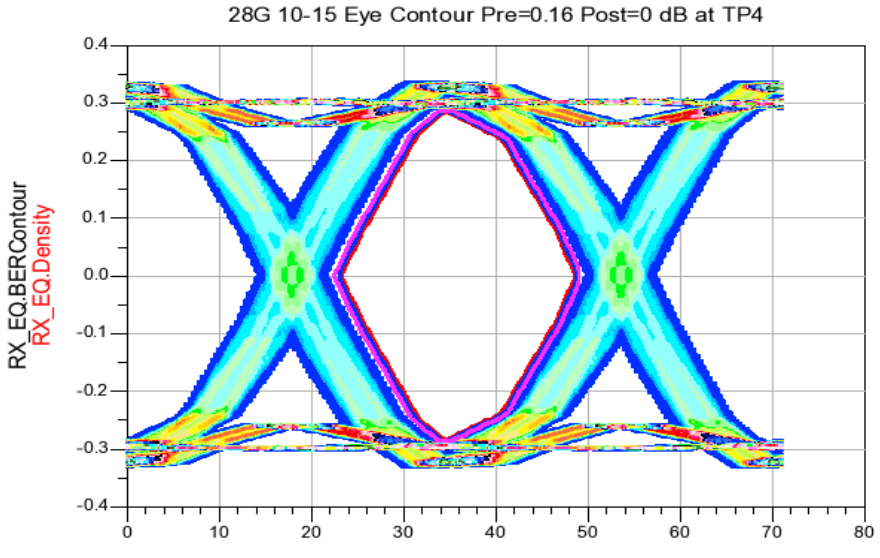




Transmitter and Link Setup

- Baudrate 28 GBd
- Tr/Tf 20-80 16 ps at package output
- Launch scaled for 600 mV
- channel parameters, near end eye at 1E-15 shown below
- Near end TJ 0.285 UI at 1E-15

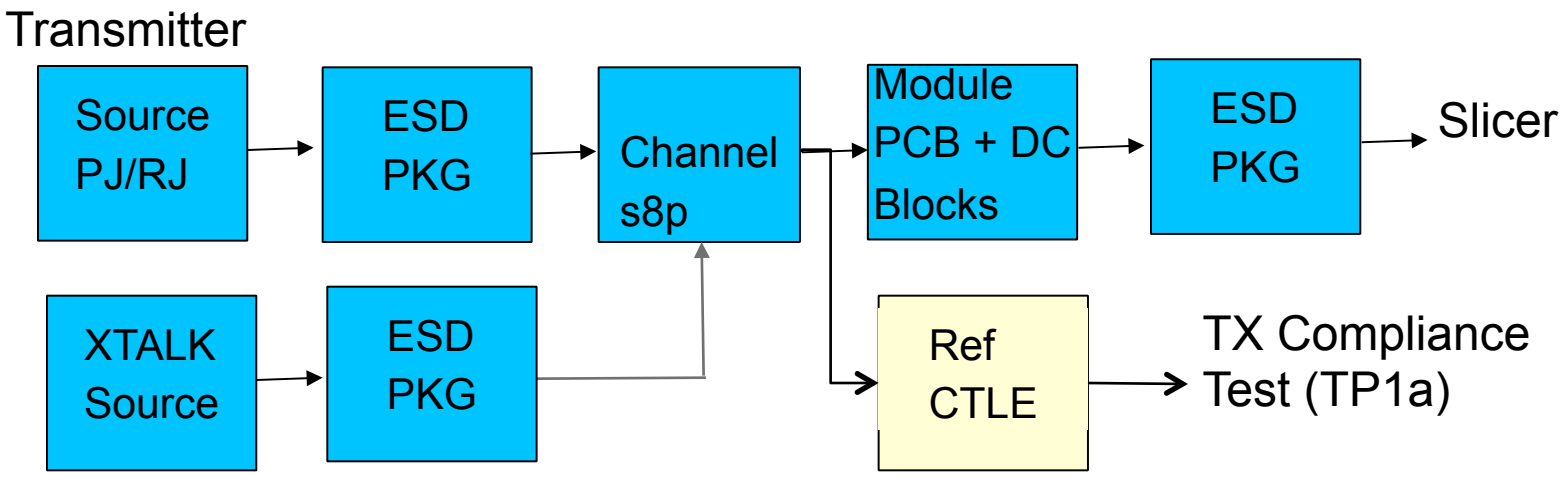
TJ 1E-15=0.285 UI



index	..._EQ.WidthAtBER)	...EQ.HeightAtBER)
0.000	2.554E-11	0.569

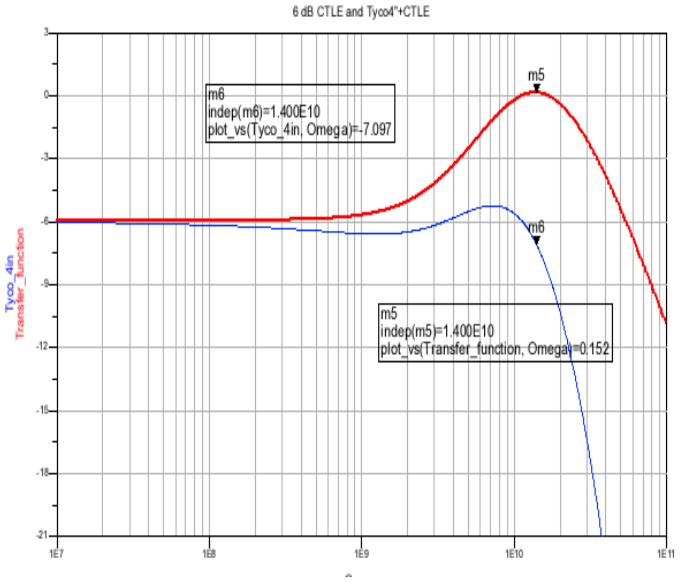
Channels and Simulation Block Diagram

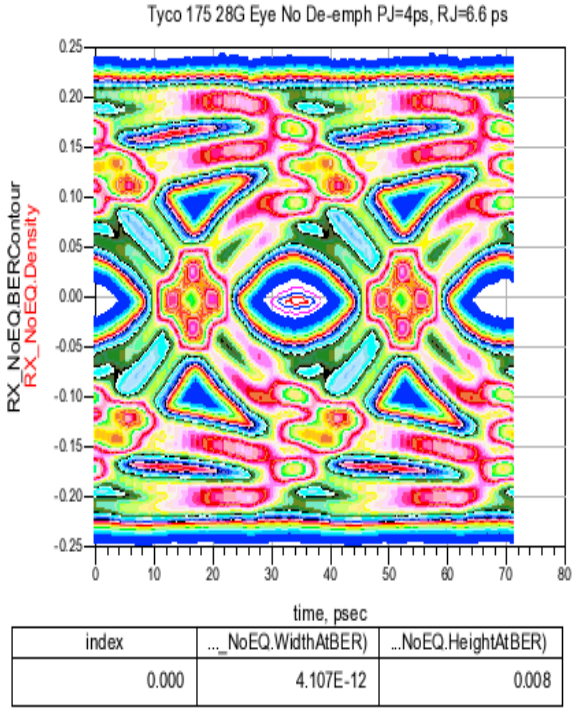
- TX compliance test is performed by inserting an HCB into the host and there is no RX ESD/PKG otherwise the receiver will be penalized



CTLE Equalizing 7 dB Channel

- Applying 6 dB CTLE to the channel
  - Showing frequency response of the channel with and without equalization
  - Showing unequalized and equalized eye





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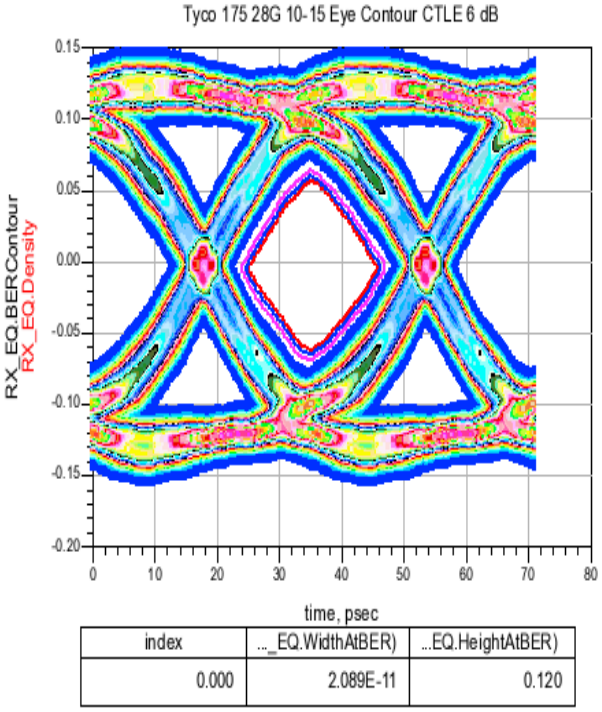
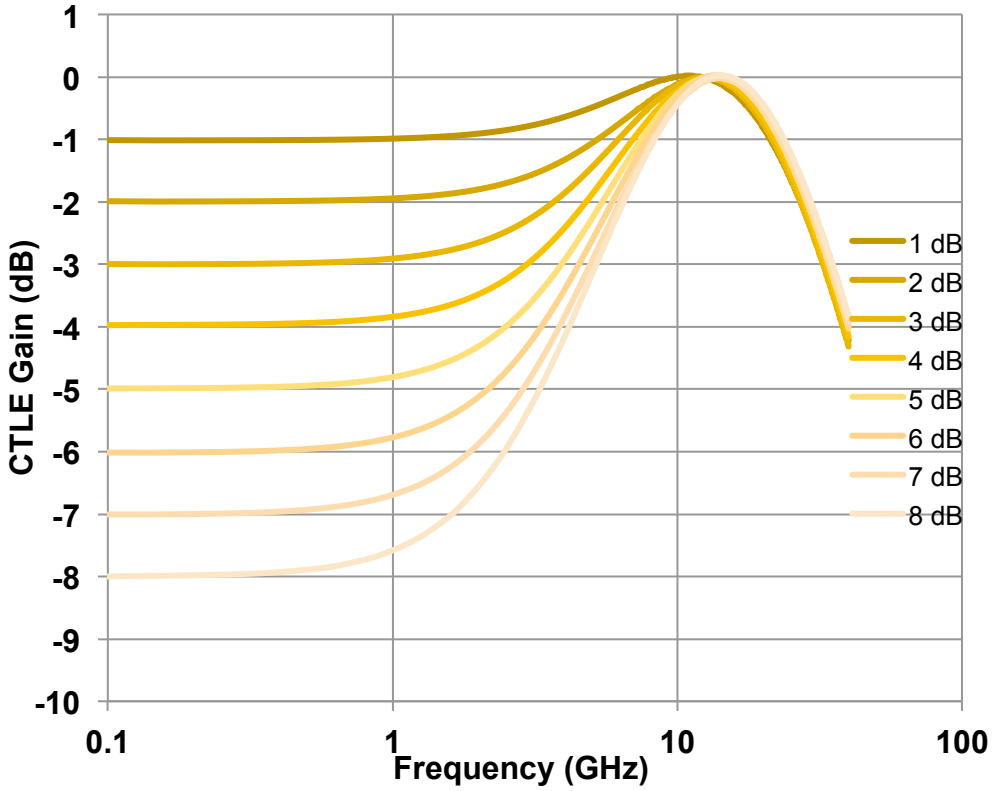


index	..._EQ.WidthAtBER)	...EQ.HeightAtBER)
0.000	2.089E-11	0.120

CTLE Response and Pole/Zeros

- CTLE response is defined by

$$Gain = G\frac{P1 \bullet P2}{Z}\frac{(Z - j*\omega)}{(P1 - j*\omega)(P2 - j*\omega)}$$



Gain	G	Z	P1	P2
1	0.89	7.1e9	1.86e10	1.41e10
2	0.795	7.1e9	1.86e10	1.41e10
3	0.795	7.1e9	1.56e10	1.41e10
4	0.633	4.98e9	1.56e10	1.41e10
5	0.563	4.35e9	1.56e10	1.41e10
6	0.5	3.82e9	1.56e10	1.41e10
7	0.446	3.4e9	1.56e10	1.41e10
8	0.398	3e9	1.56e10	1.41e10

The Differences between TP1a and Slicer

- TP1a is measured with metrology grade HCB and DC-blocks
- The signal at the slicer must pass through
  - Non-metrology grade module PCB
  - Broadband DC blocks (standard 0.1 uf will add additional penalty)
  - Mismatch between trace and the cap body
  - Package/Via/BGA
  - Non-ideality of real CTLE vs the reference CTLE
  - ESD diode
- With very good design practice there is about 0.1 UI non-EQJ* penalty and about 30% vertical eye penalty!

* Non-EQJ is the residual p-p jitter left after the reference CTLE at 1E-15

Simulation Comparison of Point B vs the Slicer all Results for 1E-15

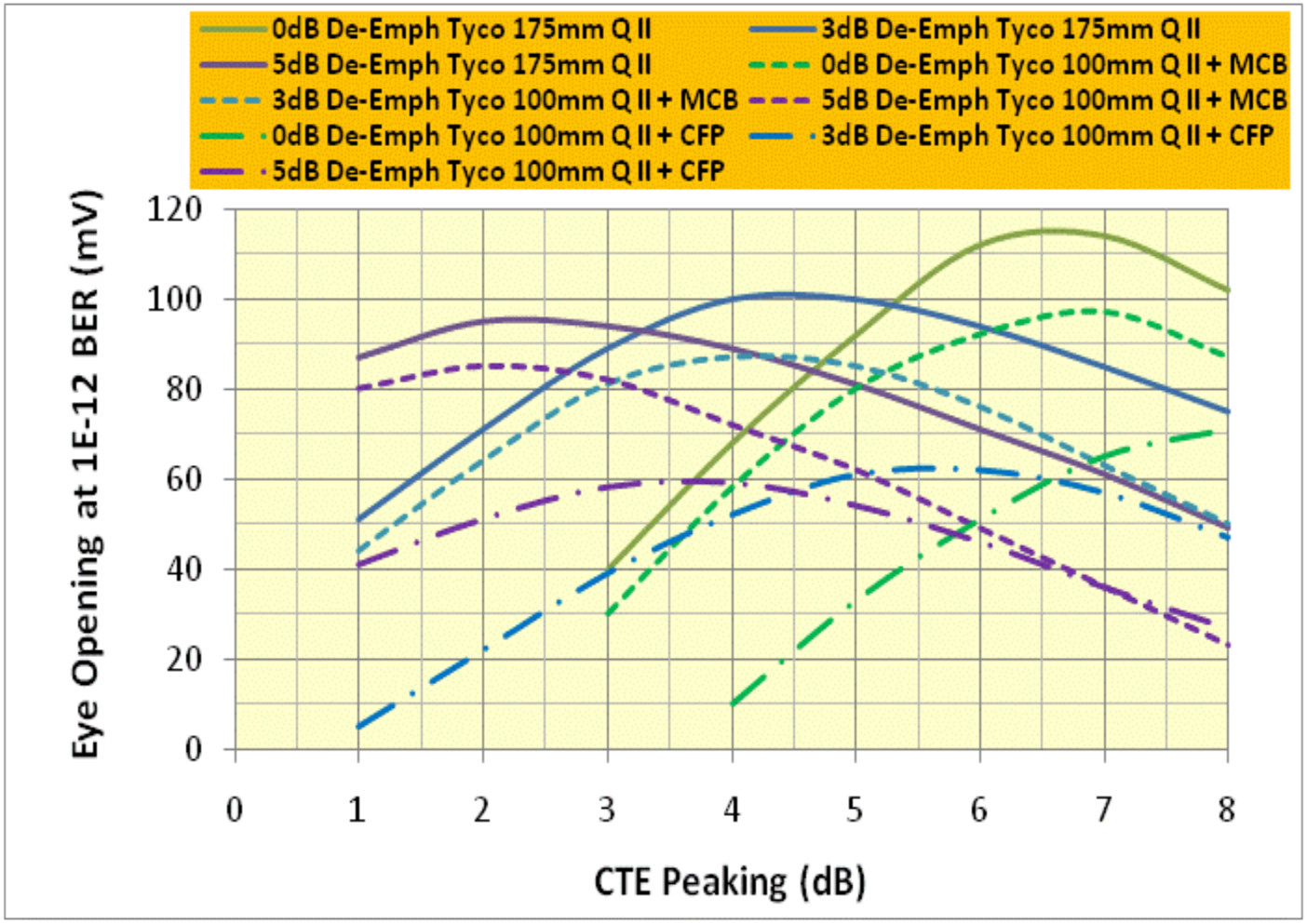
- The three channel consist of reference TE Quattro channel, high ILD channel, and high sqrt(f) channel

Channel	Loss @ 14GHz	ILD (RMS)	Eye H FFE2	Eye H * FFE2/ CTLE	Eye H * FFE3/ CTLE	Eye W FFE2	Eye W * FFE2/ CTLE	Eye W * FFE3/ CTLE
TE Quattro II 175 mm at Slicer	9.9 dB	0.045	62 mV	77 mV	87 mV	0.349 UI	0.390 UI	0.393 UI
TE Q II 4in + Microstrip at Slicer	9.8 dB	0.055	47 mV	71 mV	74.25 mV	0.331 UI	0.346 UI	0.385 UI
zSFP+ Channel at Slicer	11.2	0.029	25 mV	46.5 mV	54 mV	0.235 UI	0.319 UI	0.408 UI
TE Quattro II 175 mm at TP1a	9.9 dB	0.045	100 mV	106 mV	114 mV	0.505 UI	0.528 UI	0.529 UI
TE Q II 4in + Microstrip at TP1a	9.8dB	0.055	85 mV	97mV	106 mV	0.435 UI	0.485 UI	0.478 UI
zSFP+ Channel at point TP1a	11.2	0.029	33 mV	66 mV	86 mV	0.295 UI	0.385 UI	0.455 UI

* Most of the equalization is done by CTLE post 1 to 2 dB and Pre in the 1 to 1.5 dB

Varying Tx Pre-emphasis With Ideal CTLE: Eye Height at TP1a

- TX amplitude 800 mV, XTLAK 800 mV



Varying Tx Pre-emphasis With Ideal CTLE Eye Width at TP1a

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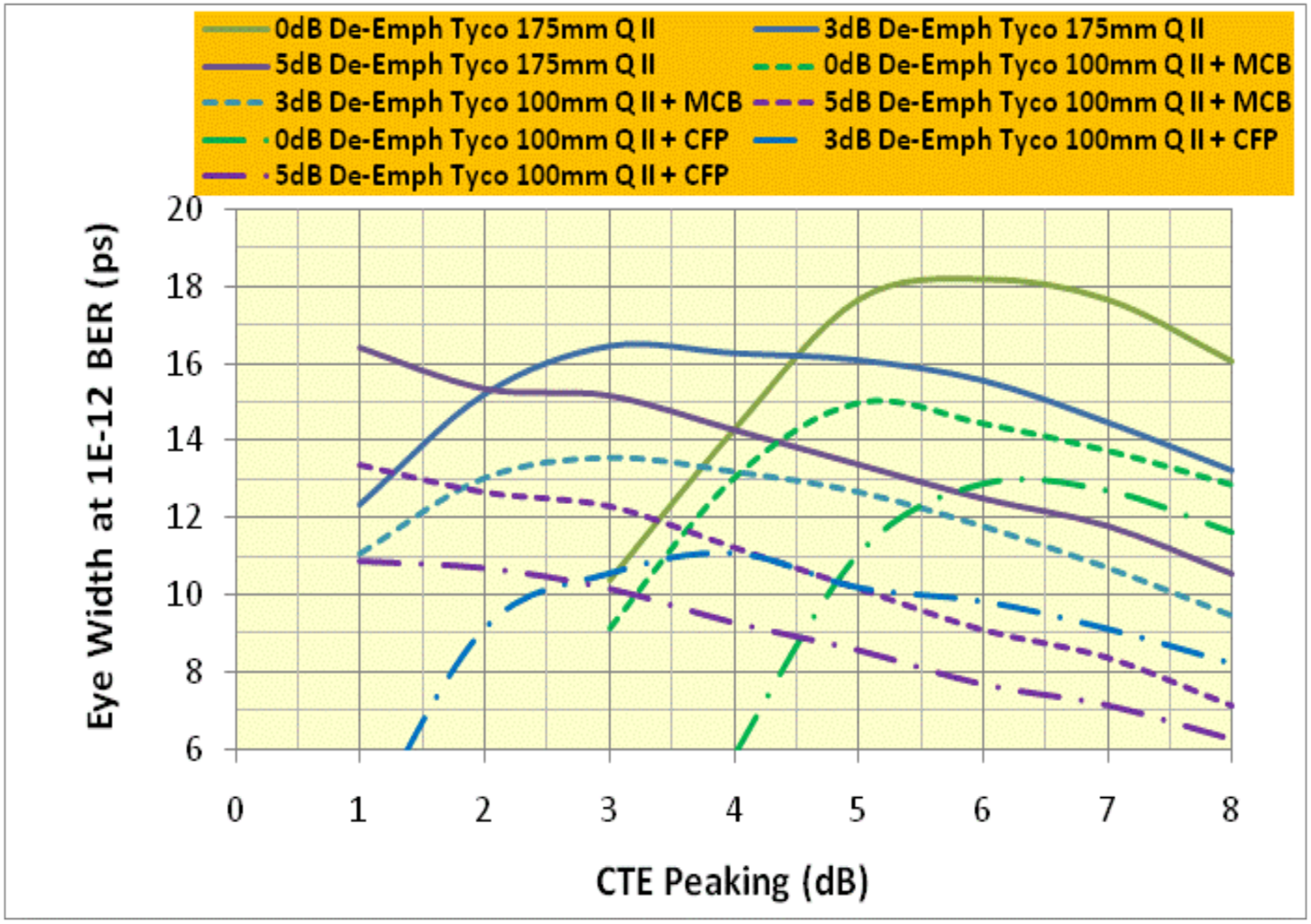
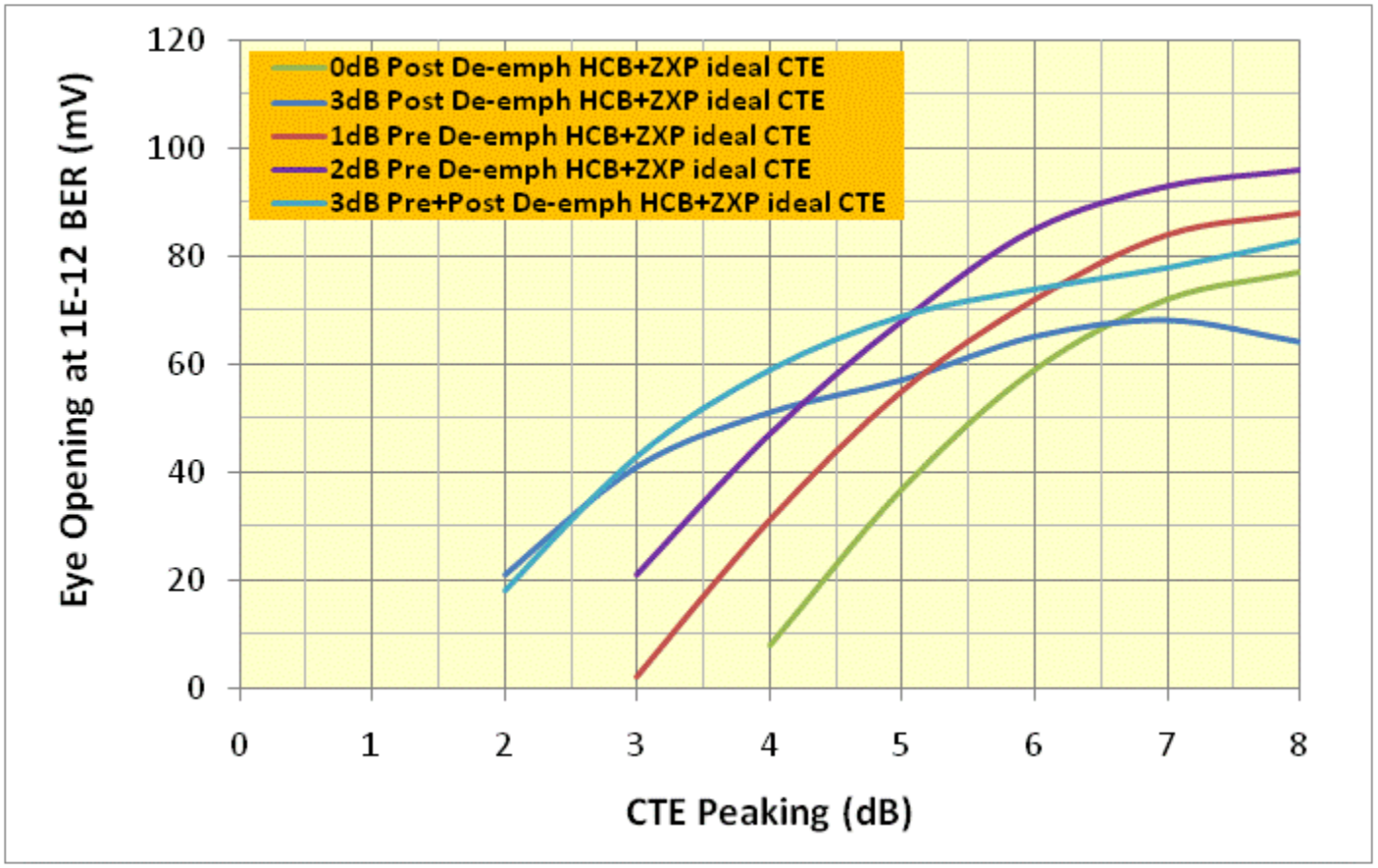


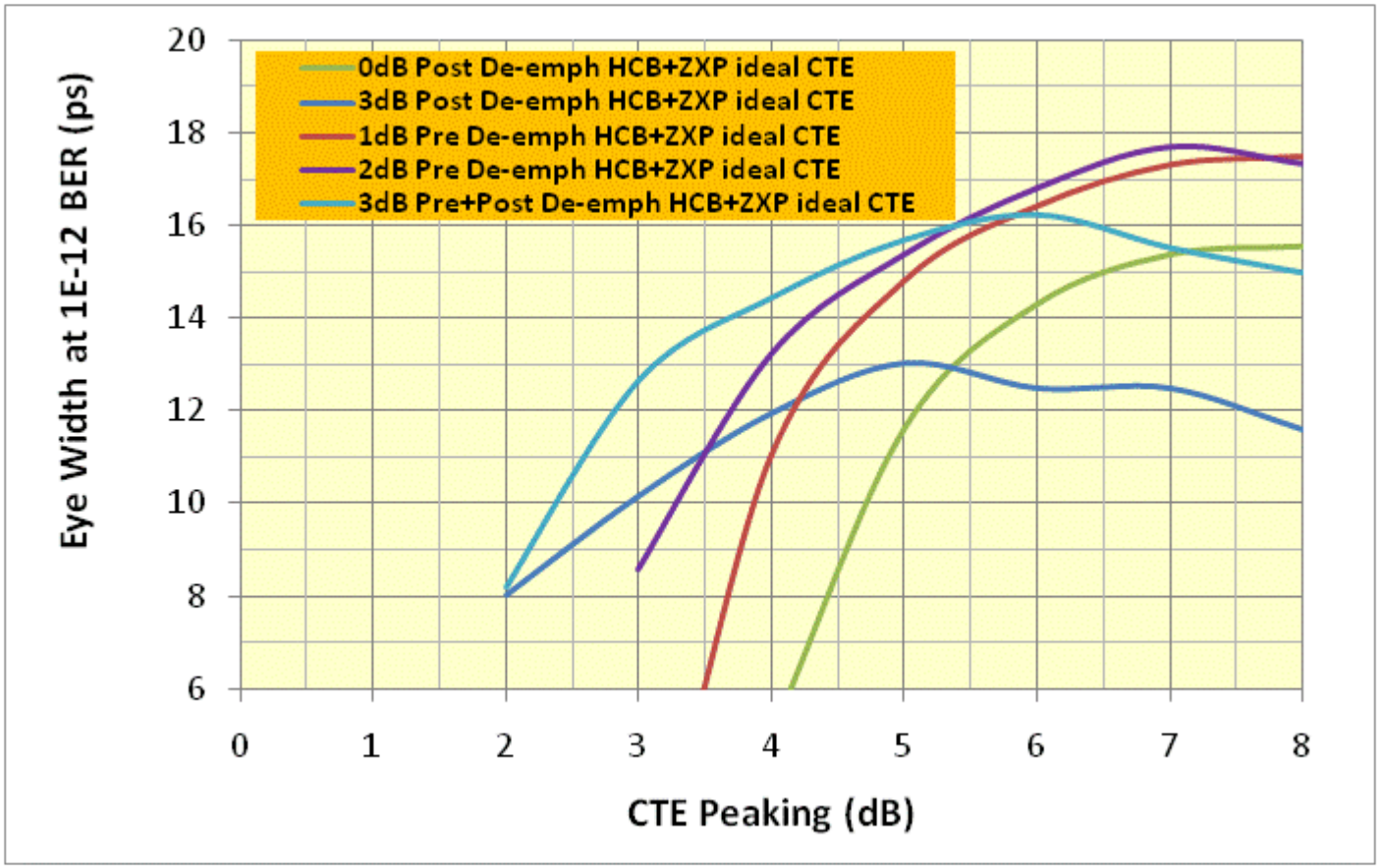
Varying Tx De-emphasis With Ideal CTLE: Eye Height on Channel with sqrt(f) TP1a

- TX amplitude 800 mV, XTLAK 800 mV, channel zSFP + Channel + 2HCB Cal
- 3dB Pre+Post de-emphasis uses same precursor tap value as 1dB precursor de-emphasis



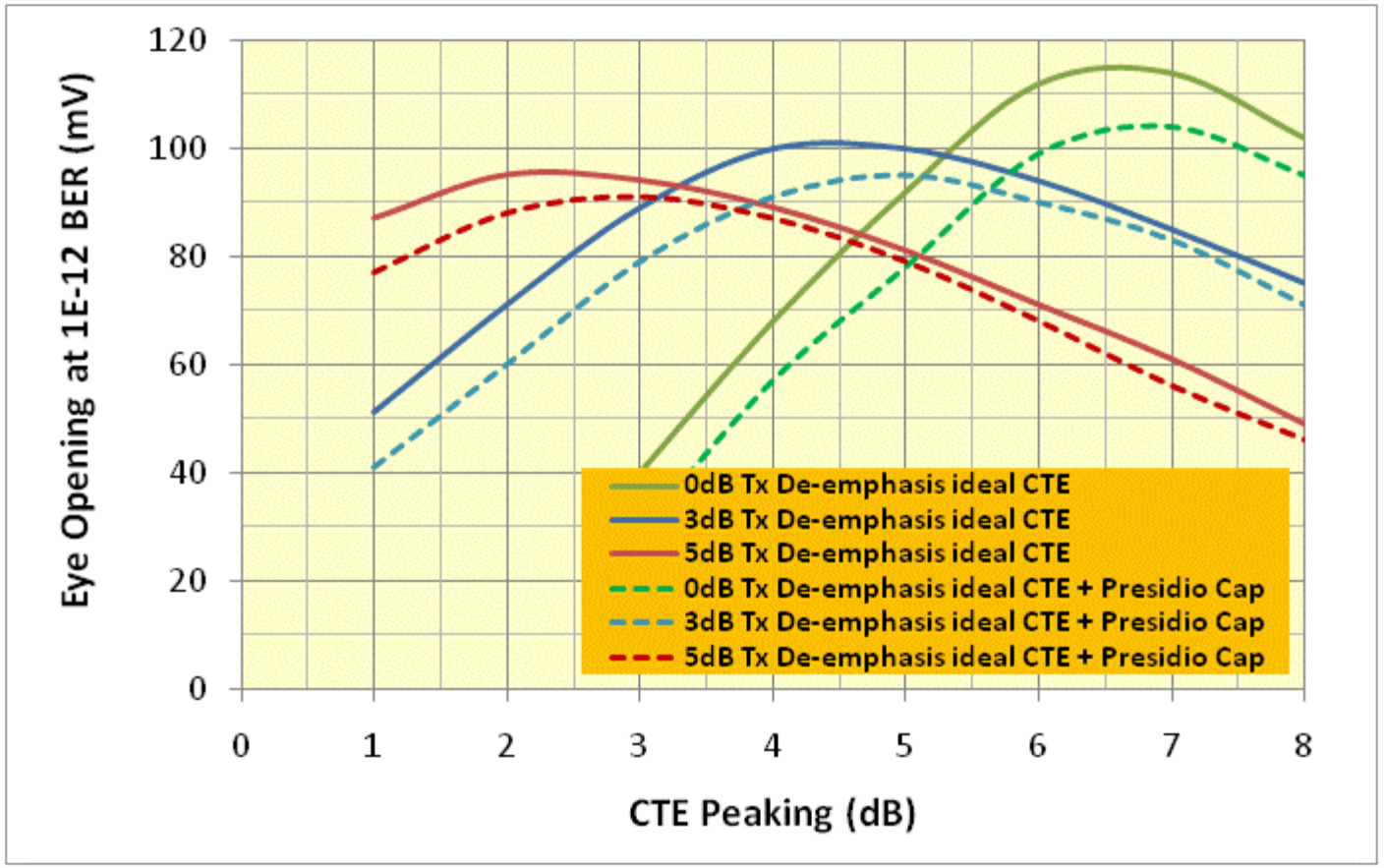
Varying Tx De-emphasis With Ideal CTE: Eye Width on Channel with sqrt(f)

- TX amplitude 800 mV, XTLAK 800 mV, channel zSFP + Channel + 2HCB Cal
- 3dB Pre+Post de-emphasis uses same precursor tap value as 1dB precursor de-emphasis



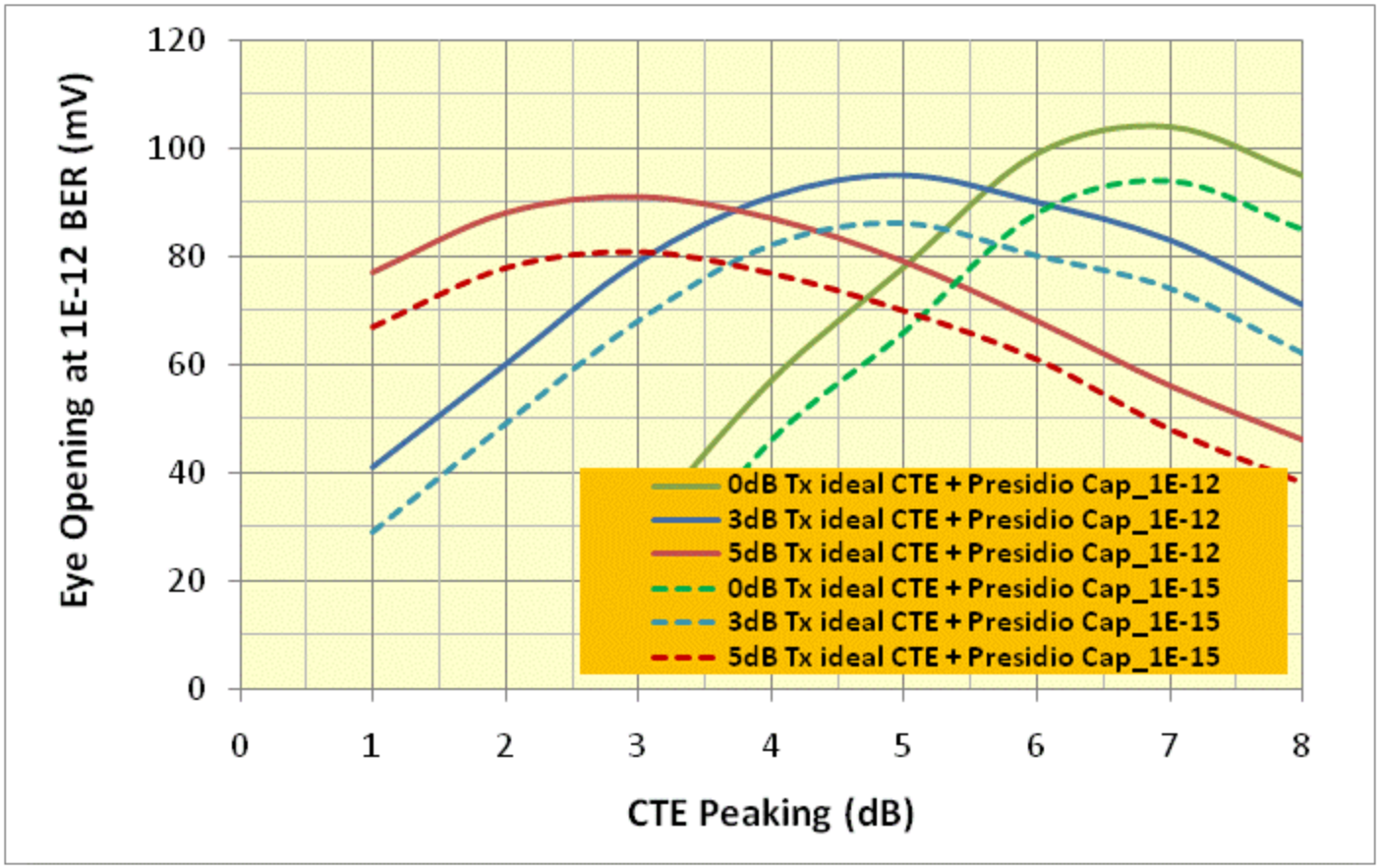
TE 175 mm Tx Pre-emphasis With & Without Presidio Cap: Eye Height

- TX amplitude 800 mV, XTLAK 800 mV



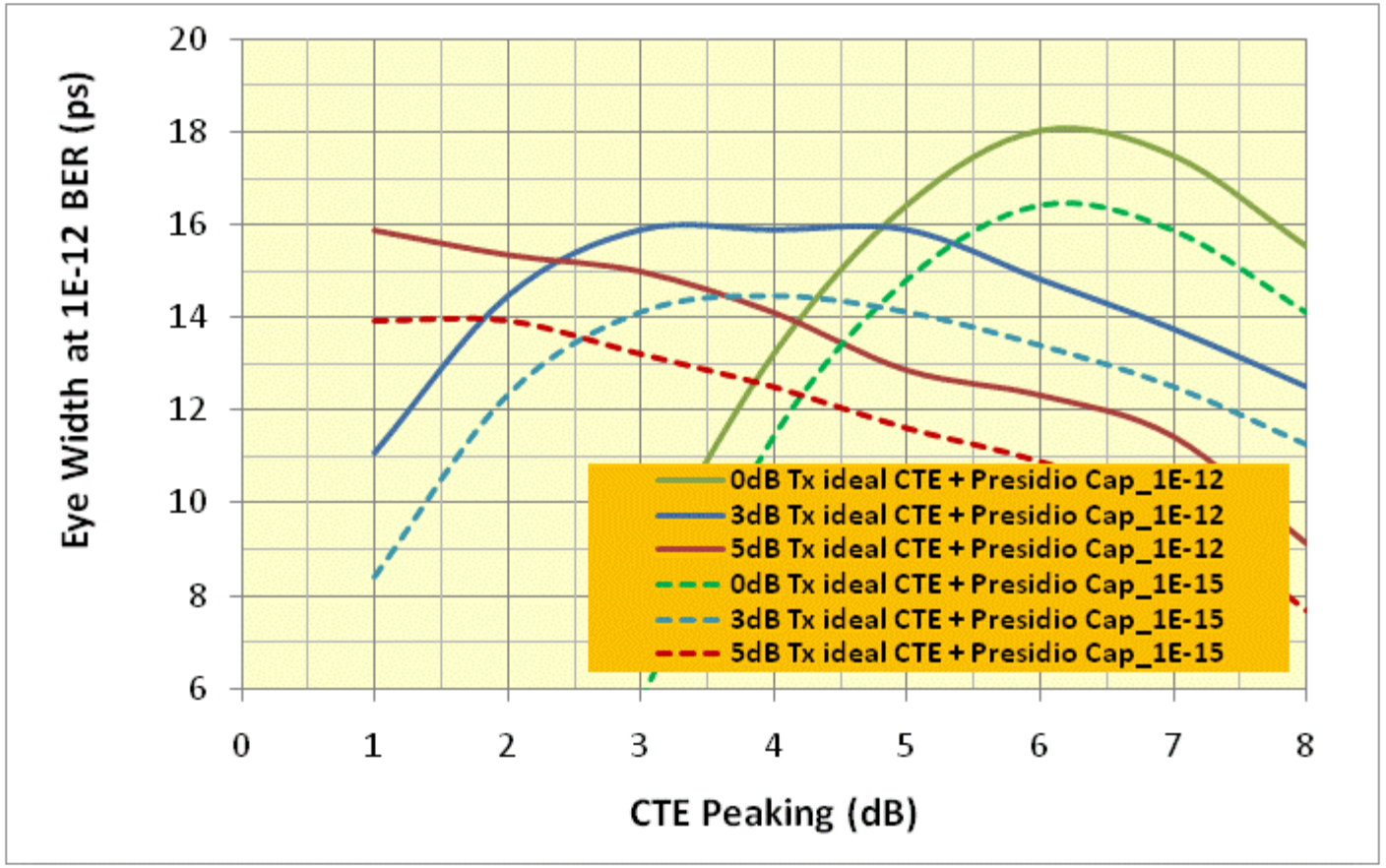
Tyco 175 mm Tx Pre-emphasis With Presidio Cap: Eye Height

- TX amplitude 800 mV, XTLAK 800 mV



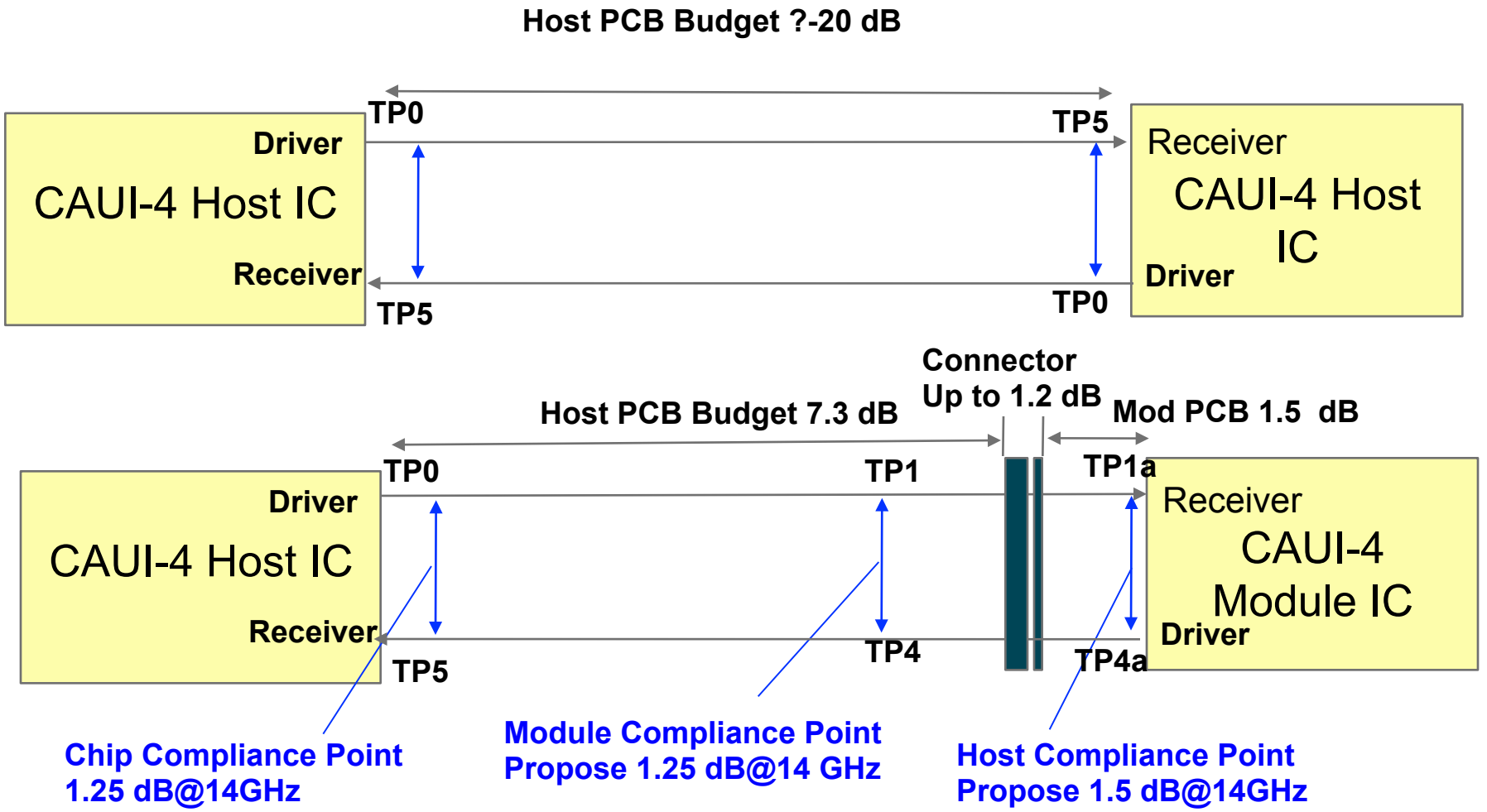
Tyco 175 mm Tx Pre-emphasis With Presidio Cap: Eye Width

- TX amplitude 800 mV, XTLAK 800 mV



CAUI-4 Architecture and Reference Points

- The bm group need to further study CAUI-4 chip to chip application
  - Considering all the constrains, the 10 dB is the best choice for the chip to module



Summary

- I highlighted during the July 2012 meeting the need to develop a common chip to chip and chip to module interface with loss of 20 dB
- After detail study over course of several conference call the take away is that 10 dB is the best choice for chip to module among number of other choice less attractive
- One could argue CAUI-4 with CTLE easily could have 12-13 dB loss budget Creating two port type
  - 12-13 dB is too little to create a different port type
  - Not enough support to add 1-2 tap DFE to the module CDR with ~35% power increase to support channel with 16-20 dB
  - With some of the next generation 28G connectors having ICN in excess of 5 mV RMS it is not so clear even 12-13 dB would be feasible
  - Higher loss budget chip to module should be left as engineered solution and perhaps some guideline could be provided in an informative annex
- In the bm group need to focus on the chip to chip application where loss budget is in 18-20 dB
  - Do we also create a 2nd chip to chip interface based on 10 dB?

Thank You