Changes to Clause 95 discussed in the MMF Ad Hoc

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95.7.2 100GBASE-SR4 receive optical specifications

Each lane of a 100GBASE-SR4 receiver shall meet the specifications in Table 95–7 per the definitions in 95.8.

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–11	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.6	dBm
Conditions of stressed receiver sensitivity test:[d]		
~~Vertical eye closure penalty (VECP),[d] lane under test~~	~~4.2~~	~~dB~~
TxVEC of stressed receiver conformance test signal, lane under test	5	dB
Stressed eye J2 Jitter,[d] lane under test	0.41	UI
Stressed eye J4 Jitter,[d] lane under test	0.55	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	
~~TxVEC of stressed eye conformance signal[d]~~	~~5~~	~~dB~~

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.
[d]~~Vertical eye closure penalty and stressed eye jitter are~~These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

95.7.3 100GBASE-SR4 illustrative link power budget

An illustrative power budget and penalties for 100GBASE-SR4 channels are shown in Table 95–8.

Table 95–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 5 or valid 100GBASE-SR4 signal	95.8.2
Average optical power	3, 5 or valid 100GBASE-SR4 signal	95.8.3
Optical modulation amplitude (OMA)	Square wave or 4	95.8.4
Transmitter vertical eye closure (TxVEC)	3 or 5	95.8.5
Extinction ratio	3, 5 or valid 100GBASE-SR4 signal	95.8.6
Transmitter optical waveform	3, 5 or valid 100GBASE-SR4 signal	95.8.7
Stressed receiver sensitivity	3, 5 or valid 100GBASE-SR4 signal	95.8.8
~~Vertical eye closure penalty calibration~~ TxVEC of stressed receiver conformance test signal calibration	~~3 or 5~~ 3, 5 or valid 100GBASE-SR4 signal	~~87.8.11~~95.8.8

95.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for an interface at the BER specified in 95.1.1. The interface BER is the average of the four BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (RS-FEC encoded scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three unstressed lanes, and the BER for that stressed lane alone must be found, e.g., by multiplying by four if the unstressed lanes have low BER. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane.

95.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 95–6 if measured per TIA/EIA-455-127-A or IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 95–10.

The method described in 95.8.5.1 and 95.8.5.2 is the reference measurement method. Other equivalent measurement methods may be used with suitable calibration.

95.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 95–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using one of the test patterns specified for extinction ratio in Table 95–10.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 95–10).

95.8.7 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86-4 with the Transmitter eye mask coordinates and hit ratio in Table 95–6. The transmitter optical waveform of a port transmitting the test pattern specified in Table 95–10 shall meet specifications according to the methods specified in 86.8.4.6.1 with the exceptions that:

— The clock recovery unit's high-frequency corner bandwidth is 10 MHz.
— The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691.

Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response, and for any excess reference receiver noise.

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined by 95.8.8.1 and 95.8.8.5, with the conformance test signal at TP3 as described in 95.8.8.2.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Pattern 3 or Pattern 5, or a valid 100GBASE-SR4 signal, is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.

95.8.8.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 95–5. The patterns used for the received compliance signal are specified in Table 95–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 95.8.8.2, and has sinusoidal jitter applied as specified in 95.8.8.5. A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The low-pass filter is used to create ISI ~~-induced vertical eye closure penalty (VECP)~~. The low-pass filter, when combined with the E/O converter, should have a frequency response that results in the appropriate level of ~~initial vertical eye closure~~ TxVEC before the sinusoidal terms are added.

The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the ~~VECP~~TxVEC, stressed eye J2 Jitter, and stressed eye J4 Jitter specifications

given in Table 95–7 are met simultaneously while also passing the stressed receiver eye mask in Table 95–7 according to the methods specified in 95.8.7 (the random noise effects such as RIN, or random clock jitter, do not need to be minimized).

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized.

The stressed receiver conformance signal verification is described in 95.8.8.4.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 95–7. Pattern 3 or Pattern 5, or a valid 100GBASE–SR4 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 100GBASE-SR4 the relevant BER is the interface BER at the PMD service interface. The interface BER is the average of the four BER of the receive lanes when stressed: see 95.8.1.1. If present, the RS-FEC sublayer can measure the lane symbol error ratio at its input. The lane BER can be assumed to be one tenth of the lane symbol error ratio. If each lane is stressed in turn, the PMD interface BER is the average of the BERs of all the lanes when stressed: see 95.8.1.1.

95.8.8.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver of the lane under test meets BER requirements with near worst-case waveforms at TP3.

The primary parameters of the stressed receiver conformance test signal are ~~vertical eye closure penalty (VECP)~~its TxVEC, stressed eye J2 Jitter and stressed eye J4 Jitter. ~~VECP is measured at the time center of the eye, half way between the normalized times of 0 and 1 on the unit interval (UI) scale as determined by the eye crossing means. VECP is given by Equation (87–1), and illustrated in Figure 87–4 (see 87.8.11.2).~~The TxVEC of the stressed receiver conformance test signal is measured according to 95.8.5, except that the combination of the O/E and the oscilloscope used to measure the waveform has a fourth-order Bessel-Thomson filter response with a bandwidth of 19.34 GHz. Stressed eye J2 Jitter and stressed eye J4 Jitter are defined in 95.8.8.3.

An example stressed receiver conformance test setup is shown in Figure 95–5, however any approach that modulates or creates the appropriate levels and frequencies of the ~~VECP~~ TxVEC and jitter components is acceptable.

The following steps describe a possible method for setting up and calibrating a stressed eye conformance signal when using a stressed receiver conformance test setup as shown in Figure 95–5:

1) Set the signaling rate of the test pattern generator to meet the requirements in Table 95–7.
2) With the sinusoidal interferers, sinusoidal jitter, and Gaussian noise generator turned off, set the extinction ratio of the E/O to approximately the minimum specified in Table 95–6.
3) The required values of ~~VECP~~TxVEC, J2 Jitter and J4 Jitter of the stressed receiver conformance signal are given in Table 95–7.

   With ~~the~~ sinusoidal amplitude interferer 1, sinusoidal ~~interferers~~amplitude interferer 2, sinusoidal jitter, and the Gaussian noise generator turned off, greater than two thirds of the dB value of the

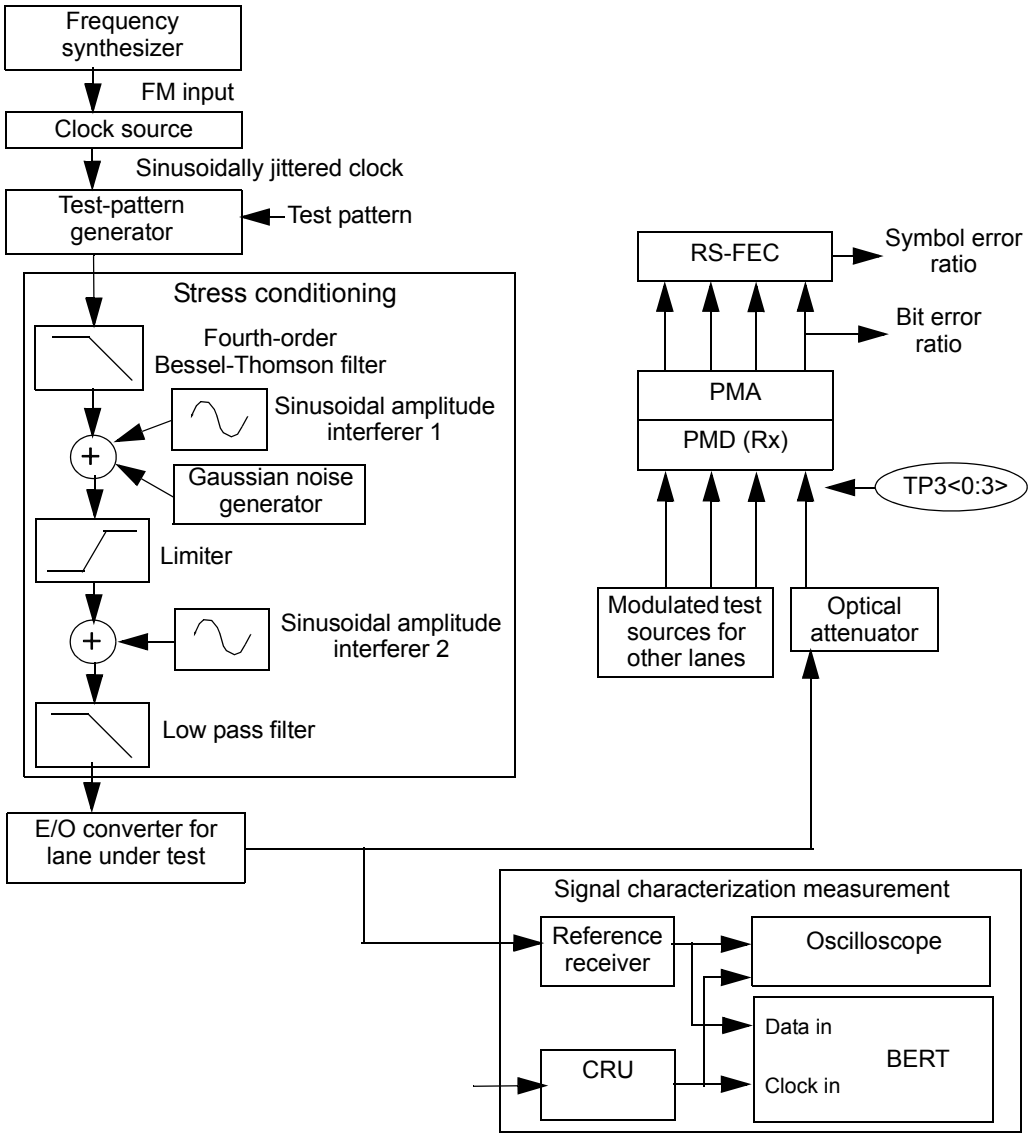

Figure 95–5—Stressed receiver conformance test block diagram

~~VECP~~ TxVEC should be created by the selection of the appropriate bandwidth for the low-pass filter. Any remaining ~~VECP~~ TxVEC must be created with a combination of sinusoidal ~~interferer 2 or~~ jitter, sinusoidal ~~jitter~~interference, and Gaussian noise.

The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The instantaneous bit shrinkage introduced by sinusoidal amplitude interferer 1 should be no more than 0.1 UI.

Sinusoidal jitter is added as specified in Table 95–11. When calibrating the conformance signal, the sinusoidal jitter frequency should be within the 10 MHz to 10 times LB as defined in Table 95–11. Sinusoidal jitter amplitude ~~below 10 MHz~~ may be calibrated by measuring the jitter on the oscilloscope, while transmitting the square wave pattern, and using a clean clock in place of the CRU to trigger the oscilloscope.

Iterate the adjustments of sinusoidal interferers and Gaussian noise generator and extinction ratio until the values of ~~VECP~~TxVEC, stressed eye J2 Jitter and stressed eye J4 Jitter meet the requirements in Table 95–7, the extinction ratio is approximately the minimum specified in Table 95–6, and sinusoidal jitter ~~above 10 MHz~~ is as specified in Table 95–11~~.~~

~~The TxVEC of the stressed eye conformance signal should not exceed the value given in Table 95–7, and is measured according to 95.8.5, except that the combination of the O/E and the oscilloscope used to measure the optical waveform has a fourth-order Bessel-Thomson filter response with a bandwidth of 19.34 GHz~~.

Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the "Stressed receiver sensitivity (OMA), each lane (max)" specified in Table 95–7, and the test sources for the other lanes is set to the "OMA of each aggressor lane" specified in Table 95–7.

95.8.8.3 J2 and J4 Jitter

J2 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. J2 Jitter is defined using a clock recovery unit as in 95.8.7. If measured using an oscilloscope, the histogram should include at least 10 000 hits, and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J2 is the time interval between the two points with a BER of 2.5×10^{-3}.

J4 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-4} of the jitter distribution. J4 Jitter is defined using a clock recovery unit as in 95.8.7. If measured using an oscilloscope, the histogram should include at least 1 000 000 hits, and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J4 is the time interval between the two points with a BER of 2.5×10^{-5}.

95.8.8.4 Stressed receiver conformance test signal verification

The stressed receiver conformance test signal can be verified using an optical reference receiver with an ideal fourth-order Bessel-Thomson response with a reference frequency f_r of 19.34 GHz. Use of G.691 tolerance filters may significantly degrade this calibration. The clock output from the clock source in Figure 95–5 ~~will be~~ is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye J2 Jitter and stressed eye J4 Jitter that includes the sinusoidal jitter component, a ~~separate~~ clock ~~source~~ recovery unit (~~clean clock~~ CRU of Figure 95–5) is required ~~that is synchronized to the source clock, but not modulated with the jitter source. However this can only be used when the clock source is modulated with frequencies within the band of 10 MHz to 10 times LB~~.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system will result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O/E, filters and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this standard, it is recommended that the implementor fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 95.8.8.2 and 95.8.8.5.

95.8.8.5 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 95–11.