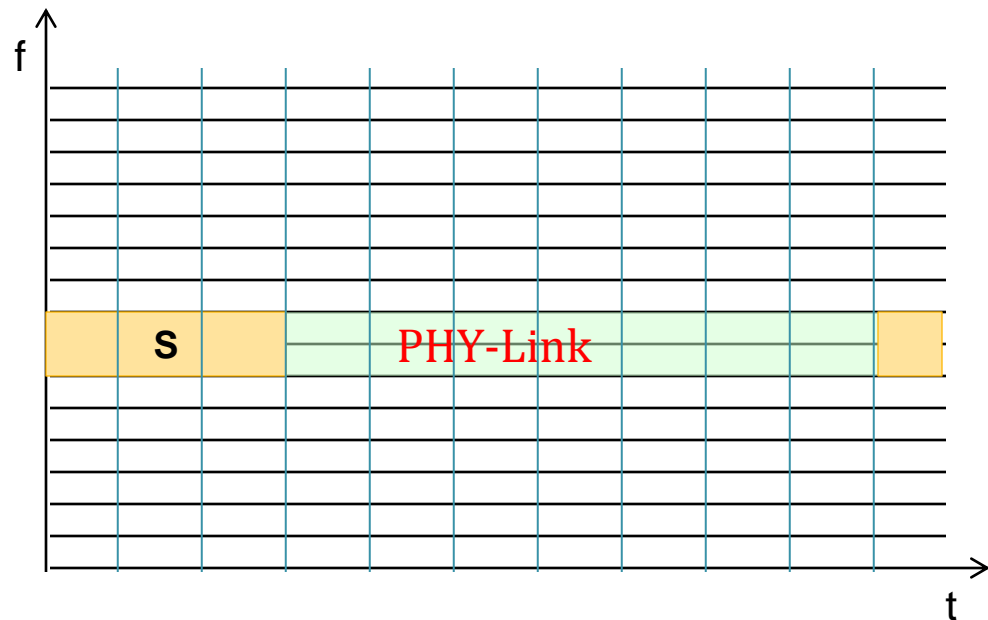




Downstream Synchronization Sequence: Vertical vs Horizontal

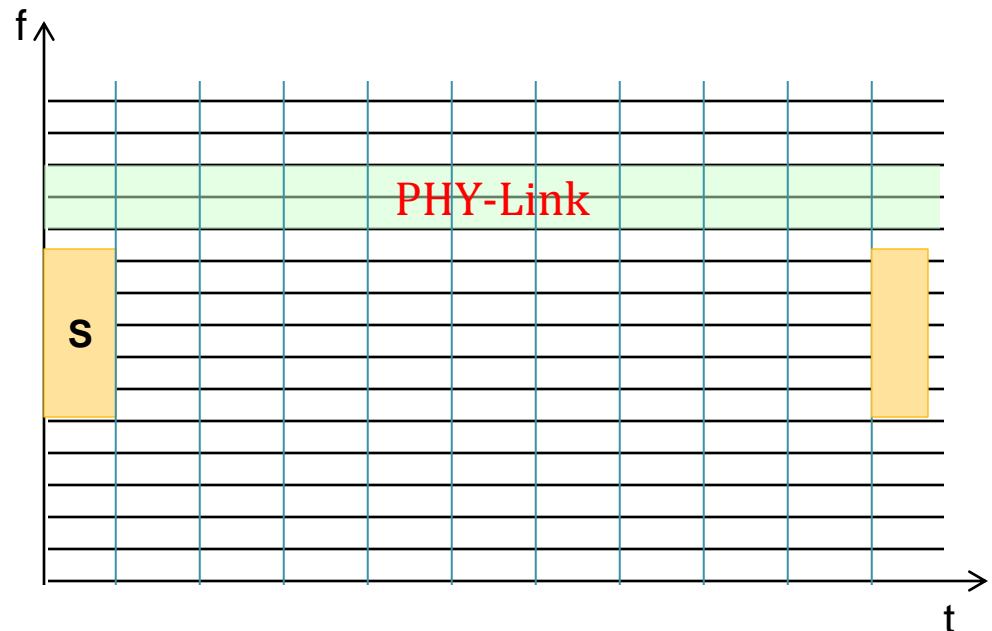
Horizontal Synchronization sequence (HSS)

- A Horizontal synchronization sequence (HSS) is a two dimensional preamble .
- The preamble occupies 8-64 sub-carriers in frequency domain and spans 25-8 OFDM symbols respectively in time domain. The preamble is repeated in every frame
- Proposed in [kilgar_02_1301.pdf](#)



Vertical Synchronization Sequence (VSS)

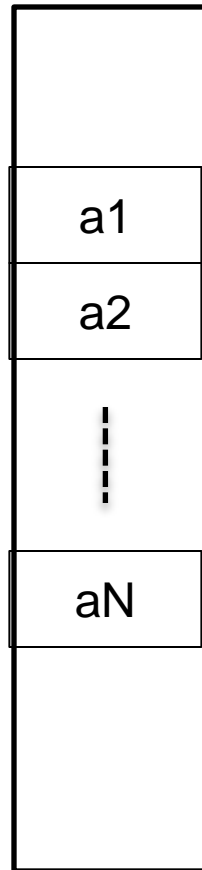
- The Vertical synchronization sequence (VSS) is one-dimensional in frequency domain
- It occupies 128-512 sub-carriers in the first OFDM symbol of every frame.
- Alternative proposal



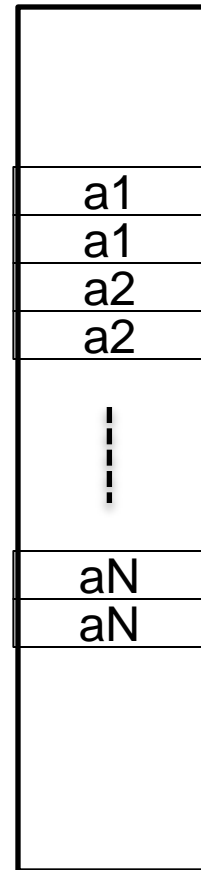
Proposed Synchronization sequence structure.

- The synchronization sequence occupies 128 sub-carriers of a single OFDM symbol.
- The synchronization sequence for 8K FFT case is derived by duplicating the synchronization sequence for the case of 4K FFT.
- The CNU can use a single correlator to achieve synchronization in just one shot.

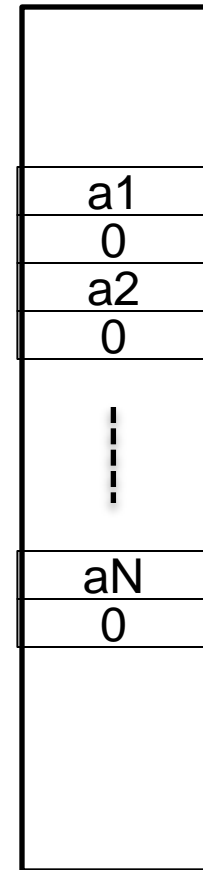
Synchronization sequences



4K FFT case

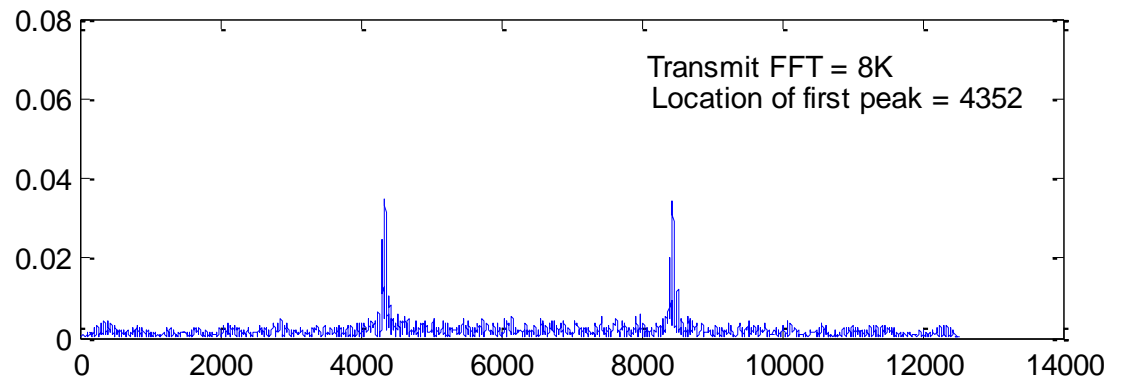
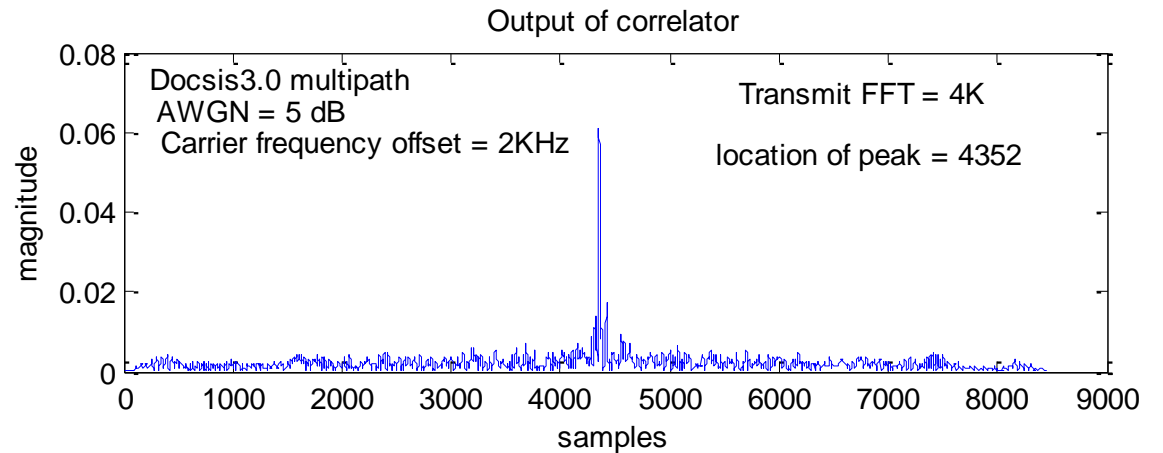


<OR>



8K FFT case

Simulation results



Reference synchronization sequence generated at CM is same for both cases.

Performance:

- Simulation Conditions:
 - 1) DOCSIS 3.0 Multipath Profile
 - 2) Carrier frequency offset (2, 50 & 52kHz)
 - 3) Number of iteration=5000;
 - 4) Synchronization length =127/255 sub-carriers for 4K/8K FFT

Results:

Detection = 99.99% for 10 dB AWGN (50 & 52kHz offset)

Detection = 99.52% for 5 dB AWGN (2kHz offset)

HSS “better than 99.9% detection at SNR as low as 10 dB”.

HSS VSS Comparison

- Compared to VSS, the HSS scheme has three fundamental problems:
 - 1) **Speed:** significantly slower (8-10 x)
 - 2) **Circuit Complexity:** significantly more gates (8-25 x)
 - 3) **Signal Processing:** significantly more processing required (80-250 x)
 - Can be mitigated somewhat with additional memory

Speed analysis

- HSS preamble is spread across some number (8 – 25) of successive OFDM symbols
- The distance between successive OFDM symbols depends upon two factors:
 - OFDM symbol duration (2 options; 25/50 us)
 - Cyclic Prefix length (5 options)
- During initial synchronization, both of these factors are unknown
- This requires the synchronization process to be repeated with 10 different hypothesis (5 possible CP lengths and 2 possible OFDM symbol lengths)
- In VSS the synchronization sequence is fully contained within a single OFDM symbol. And the synchronization can be achieved with just a single Hypothesis
- Can be mitigated by using more memory (329 Kbytes)

Circuit Complexity

- Synchronization process is a correlation operation (illustrated in following slides)
- The number of coefficients in the correlator is equal to the number of samples in the OFDM duration
 - (typically FFT size down sampled by some number such as $32 = 256$)
- HSS is spread across 8 to 25 OFDM symbols
 - Requires 8 to 25 independent correlators, each with a different set of coefficients.
 - Results in 8 to 25 times more gates (multipliers, adders, and memory elements)
- VSS is fully contained in a single OFDM symbol and requires only a single correlator.

Correlator structure

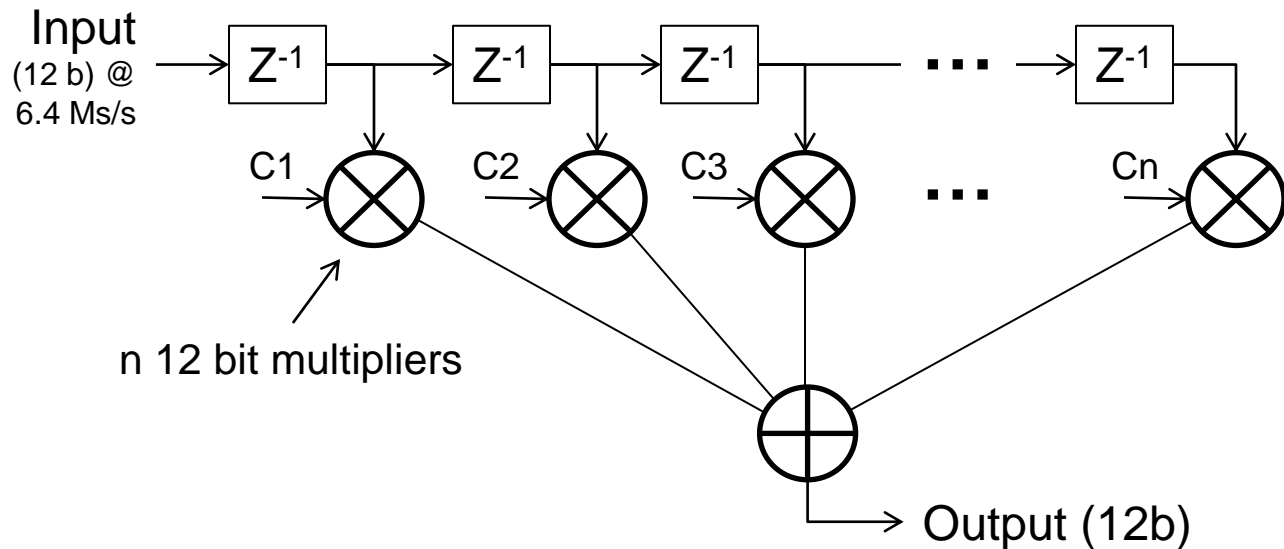
- n multipliers of M bits

Where:

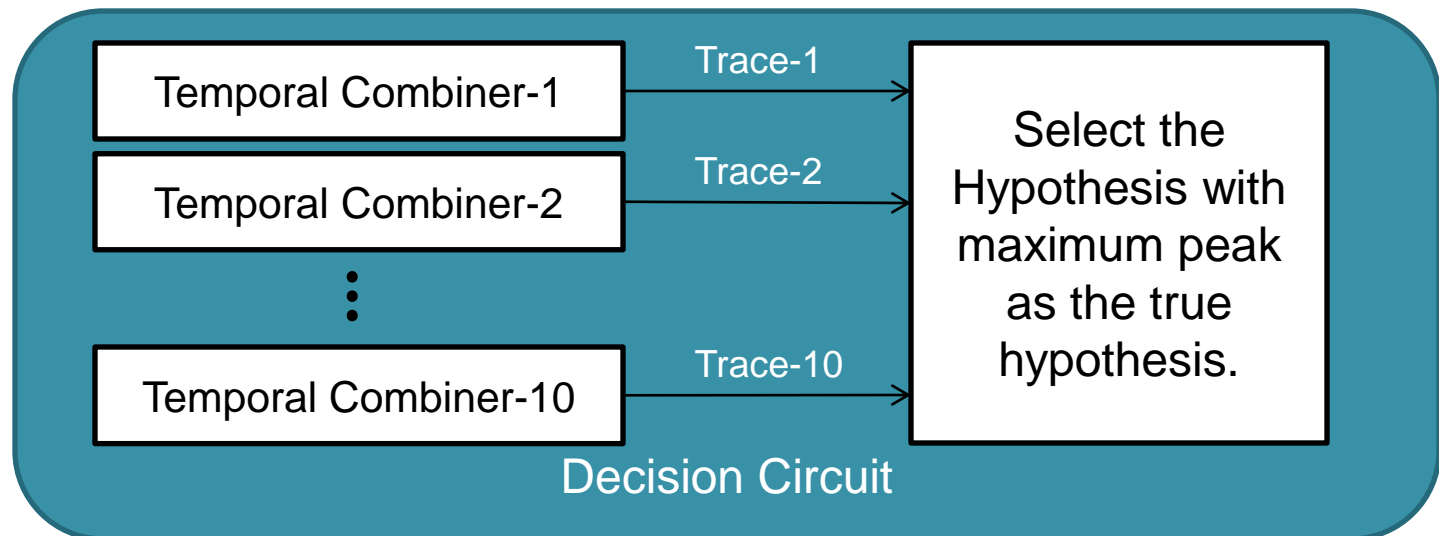
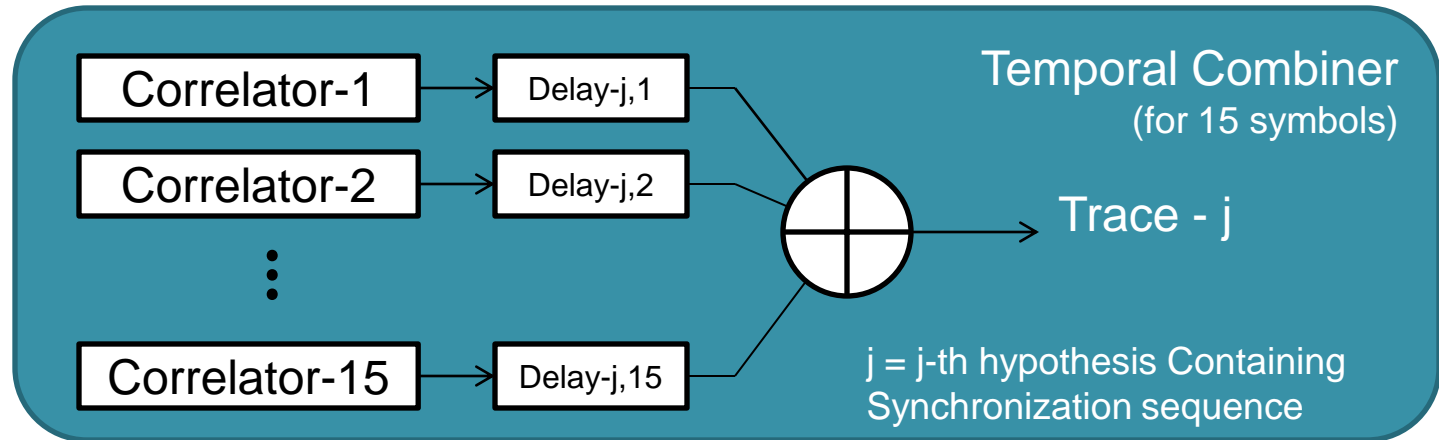
n = number of coefficients ($256 = 8192/32$)

M = ADC width (12 bits)

$C_1..C_n$ – known coefficients



Correlator structure



Signal processing

- For each hypothesis the HSS scheme requires 8 to 25 times more correlators.
- For 10 hypothesis the HSS scheme re-uses the above correlators 10 times
 - requires 80 to 250 times more digital signal processing.

Advantages of VSS

- Approximately 10 times faster than HSS
- Eight to twenty five (per number of symbols used in HSS) times less Gates (Silicon).
- PLC can be defined independent of the VSS.

Conclusions

- VSS scheme is significantly faster .
 - Initial frequency scanning time is only 0.5 seconds, instead of 5 seconds [see Appendix:A]
 - VSS circuit is 8-25 times less complex
 - VSS scheme take 80-250 times less digital signal processing
- <OR>
- 8-25 x processing with 329kB more memory



THANK YOU

Appendix:A: Initial synchronization time

- Assumptions:
 - Frame length = 3.2 milliseconds
 - Number of frequency scans = $1\text{GHz}/6\text{Mhz}=167$
 - Frequency scanning time = (Number of Hypothesis)*(frame length)* (Number of frequency scans)
- Frequency scanning time for proposed scheme = $1*3.2\text{E}-3*167 = 0.5344$ seconds
- Frequency scanning time for existing preamble structure = $10*3.2\text{E}-3*167 = 5.3$ seconds.

Can be mitigated using more memory

Number of multiplications

- For 8K FFT each matched filter uses 256 complex multiplications at 6.4 Msps
- The table below shows the number of multiplications needed for the case above

| Preamble in symbols | Number of Matched Filters (B) | Complex Multiplications $C = B * 256$ | Real Multiplications $D = 4 * C$ |
|---------------------|-------------------------------|--|-------------------------------------|
| 10 | 10 | 2,560 | 10,240 |
| 15 | 15 | 3,846 | 15,384 |
| 25 | 25 | 6,400 | 25,600 |