

Additional CI 45 Registers

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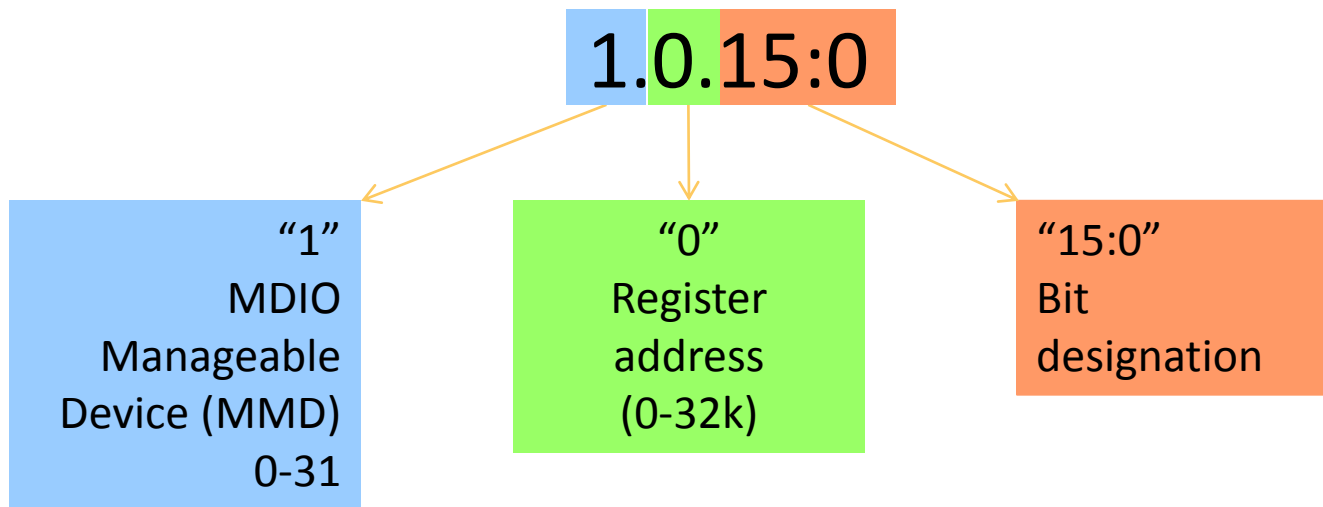
Version: V1.0(20140121)

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CI 45 Register references

- Management Data Input/Output (MDIO)



MMD's

- **MDIO Managed Device**
 - 32 possible
 - Defined in Table 45–1
- **Need to determine where we want EPoC registers located**
 - Existing MMD
 - New MMD
 - Some new some old
- **Propose taking MMD 12 for OFDM control & reporting**

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7	Auto-Negotiation
8	Separated PMA (1)
9	Separated PMA (2)
10	Separated PMA (3)
11	Separated PMA (4)
12 – 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

10GPASS-XR DS PHY-Link control

10GPASS-XR DS PHY-Link control register 1 bit definitions			
Bit(s)	Name	Description	R/W
1.a.15:12	Reserved	Ignore on read	RO
1.a.11:0	DS_PLC#1_Start	DS PHY-Link starting sub-carrier from 0 to 4095 in steps of 1 Sub-carriers or Sub-carrier pairs.	RW

DS PHY-Link search control

10GPASS-XR DS PHY-Link search control register 1 bit definitions

Bit(s)	Name	Description	R/W
1.b.15	Reserved	Ignore on read	RO
1.b.14	DS_PLC_Srch_Cntrl	1 = Start and a search 0 = Stop a search/search complete	RW
1.b.13	DS_PLC_Srch_Status	1 = Indicates a successful completed search 0 = Indicates an unsuccessful completed search	RO
1.b.12:0	DS_PLC_Srch_Freq_Start	Frequency at which to start looking for the PLC Channel . From 1 to 5000 MHz in 1 MHz steps	RW

10GPASS-XR DS PHY-Link search control register 2 bit definitions

1.c.15:8	Reserved	Ignore on read	RO
1.c.7:0	DS_PLC_Srch_Freq_Step	Step frequency to use for PLC search. From 1 to 256 MHz in 1 MHz steps	RW

10GPASS-XR DS PHY-Link search control register 3 bit definitions

1.d.15:13	Reserved	Ignore on read	RO
1.d.12:0	DS_PLC_Srch_Cnt	Number of grid steps in search range.	RW

US PHY-Link control register

10GPASS-XR US PHY-Link control register 1 bit definitions			
Bit(s)	Name	Description	R/W
1.e.15:12	Reserved	Ignore on read	RO
1.e.11:0	US_PLC#1_Start	US PHY-Link starting sub-carrier from 0 to 4095 in steps of 1 Sub-carriers or Sub-carrier pairs.	RW

DS OFDM channel center frequency

10GPASS-XR DS OFDM channel center frequency control registers bit definitions			
Bit(s)	Name	Description	R/W
1.f.15:0	DS_Center_Freq_Ch1	This specifies the center frequency of Subcarrier 0 of the first OFDM channel transmission. Since subcarrier 0 is always excluded, it will actually be below the allowed downstream spectrum band. This definition equates to a center frequency from 0 to 4.29 GHz in 65.54 kHz steps. Permissible lower bound TDB.	RW
1.f+1.15:0	DS_Center_Freq_Ch2	Channel 2	RW
1.f+n.15:0	DS_Center_Freq_Chn	Channel 3	RW

- Note D3.1 uses a 32 control value with 1 Hz resolution for this function. This accomplishes the same function with a coarser granularity.

DS Profile descriptor

10GPASS-XR DS Profile descriptor control registers bit definitions			
Bit(s)	Name	Description	R/W
12.0.15:12	DS ModType SC3	Modulation to be used for a Subcarrier 3 or Subcarrier pair 6/7,	RW
12.0.11:8	DS ModType SC2	Modulation to be used for a Subcarrier 2 or Subcarrier pair 4/5,	RW
12.0.7:4	DS ModType SC1	Modulation to be used for a Subcarrier 1 or Subcarrier pair 2/3,	RW
12.0.3:0	DS ModType SC0	Modulation to be used for a Subcarrier 0 or Subcarrier pair 0/1, Enumerate list (see below)	RW
12.1-1023	as above for Subcarrier 4-4096 (8/9 - 8191/8192)		

0=Null (nulled SC, Exclusion bands),
 1=BPSK,
 2=QPSK,
 3= 8-QAM (support optional),
 4=16-QAM (PHY-Link),
 5=32-QAM (support optional),
 6=64-QAM,
 7=128 QAM

8=256-QAM,
 9=512-QAM,
 10=1024-QAM,
 11=2048-QAM,
 12=4096-QAM,
 13=8192-QAM,
 14=16384-QAM (support optional),
 15=Cont. pilots

Thank you

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Motion

Move to accept as baseline material the MDIO Registers outlined in remain_3bn_06_0114.pdf slide 4, 5, 6, 7, 8 & 9 and incorporate into the draft.

Moved: Duane Remein

Second:

For:

Against:

Abstain:

Motion is Technical ($\geq 75\%$) Procedural ($> 50\%$)

Motion Passed/Failed